Turkish Journal of Electrical Engineering & Computer Sciences

http://journals.tubitak.gov.tr/elektrik/

Research Article

Turk J Elec Eng & Comp Sci
(2017) 25: 2686 – 2695

doi:10.3906/elk-1607-11

Compact electronically tunable quadrature oscillator using single voltage differencing gain amplifier (VDGA) and all grounded passive elements

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Received: 01.07.2016 • **Accepted/Published Online:** 13.10.2016 • **Final Version:** 30.07.2017

Abstract: This work deals with the design of a compact electronically tunable sinusoidal quadrature oscillator. The proposed quadrature oscillator is designed with a single voltage differencing gain amplifier (VDGA) and all the three grounded passive elements. Its oscillation condition and oscillation frequency can be tuned independently by means of the VDGA transconductance gains. The proposed oscillator also provides the explicit quadrature voltage outputs of almost equal magnitude and low active and passive sensitivity figures. The performance of the oscillator has been demonstrated by PSPICE simulations based on TSMC 0.35-μm CMOS technology.

Key words: Voltage differencing gain amplifier (VDGA), quadrature oscillator, electronically tunable, transconductor, voltage-mode circuits

1. Introduction

Sinusoidal quadrature oscillators, producing two identical sinusoidals with 90°-phase difference, constitute important useful blocks in many telecommunications, information, and instrumentation systems. For decades, various voltage-mode sinusoidal quadrature oscillators were constructed by various active devices, such as second-generation current conveyor (CCII) [1], differential voltage current conveyor (DVCC) [2], current differencing buffered amplifier (CDBA) [3–6], double current controlled current feedback amplifier (DCC-CFA) [7], current differencing transconductance amplifier (CDTA) [8], operational amplifier (OA) [9], current feedback operational amplifier (CFOA) [10], current follower transconductance amplifier (CFTA) [11], fully differential current conveyor (FDCCII) [12], voltage buffered/inverted amplifier (VDBA/VDIBA) [13], and fully balanced voltage differencing buffered amplifier (FB-VDBA) [14]. However, the previous works given in [1–11] require more than one active component for their circuit realizations. Most of them also employ a large number of external passive components [1–4,6,9,10,12,13]. In the most recent work [14], a very compact quadrature oscillator based on a single FB-VDBA employs only three passive elements. This configuration still includes a floating resistor, which is not suitable for integration. Moreover, its oscillation condition and oscillation frequency cannot be adjusted independently. A comparison study for the performance specifications of the previously available voltage-mode quadrature oscillators in [1–14] is summarized in Table 1.

Since the introduction of the recently defined tunable active building block, namely the voltage differencing gain amplifier (VDGA), this active device is successfully being used in designing analogue signal processing

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Table 1. Comparison of performance specifications of other previously reported voltage-mode quadrature oscillators.

Reference	No. of active elements	No. of R/C	All-grounded passive elements	Electronic tunability	Independent tunability	Technology	Supply voltages
[1]	CCII = 3	4/2	yes	no	yes	AD844	–
[2]	DVCC = 3	3/2	no	no	yes	TSMC 0.35 μm	+V = 2 V, –V = 1.9 V
[3]	CDBA = 2	3/3	no	no	yes	AD844	±12 V
[4]	CDBA = 2	4/2	no	no	yes	AD844	±12 V
[5]	CCCDBA =2	1/2	yes	yes	yes	TSMC 0.18 μm	±2 V
[6]	CDBA = 2	3/2	no	no	yes	AD844	±12 V
[7]	DCC-CFA = 2	3/2	no	yes	yes	CMOS ON-Semi C5 0.5 μm	–
[8]	CDTA = 2	1/2	yes	yes	yes	MIETEC 0.5 μm	±2.5 V
[9]	OA = 3	5/3, 3/5	no	no	yes	LF351	±10 V
[10]	CFOA = 2	3/2	no	no	yes	AD844	±12 V
[11]	GCFTA = 1, UGVF = 1	2/2	no	yes	yes	ALA400 bipolar array	±2 V
[12]	FDCCII = 1	3/2	yes	no	yes	TSMC 0.18 μm	±2.5 V
[13]	DO-VDBA = 2	1/2	no	yes	yes	TSMC 0.18 μm	±1.2 V
[14]	FB-VDBA = 1	1/2	no	yes	no	OPA860	±5 V
This work	VDGA = 1	1/2	yes	yes	yes	TSMC 0.35 μm	±1.5 V

–: Not mentioned,
GCFTA: Generalized current follower transconductance amplifier,
UGVF: Unity-gain voltage follower,
DO-VDBA: Dual output voltage differencing buffered amplifier

circuits [15–17]. This device was modified from the previously introduced VDTA and VDBA devices, in which its voltage at the terminal z (v_z) is simultaneously transferred to the current at the terminal x ($i_x = g_{mB}v_z$) and the voltage at the terminal w ($v_w = \beta v_z$) by adjustable transfer gains g_{mB} and β. Since the VDGA solution usually provides electronic tunability through its three separate transfer gains, it seems to be a versatile and flexible active element in the design of noninteractive electronic tuning circuits. In this paper, a compact tunable sinusoidal quadrature oscillator is realized with the VDGA. The oscillator circuit is constructed using a reduced number of components, i.e. one VDGA, one resistor, and two capacitors. All of the passive components are grounded, which is beneficial for the monolithic integration point of view. The realized oscillator exhibits the independent electronic controllability of the oscillation condition and the oscillation frequency by three separate biasing currents. The effects of the VDGA nonidealities on the performance of the oscillator are also analyzed. PSPICE simulation results using a 0.35-μm from TSMC CMOS technology are included, which validate the practical utility of the proposed circuit.

2. Description of the VDGA

The circuit symbol of the VDGA is shown in Figure 1. It should be noted that the VDGA device has a pair of high-impedance voltage inputs v_p and v_n, two high-impedance current outputs i_z and i_x, and a low-impedance voltage output v_w. Ideally, the difference between the input voltages v_p and v_n ($v_p - v_n$) is transformed into the current flowing of the terminal z (i_z) by the transconductance gain g_{mA}. The corresponding voltage drop at the terminal z (v_z) is converted to a current at the terminal x (i_x) by the transconductance g_{mB}. In addition,

the voltage v_z is also amplified with the voltage gain β, and then transferred to the output voltage at the terminal w (v_w). According to the above describing relations, the terminal characteristics of the VDGA can be described by the following matrix equation:

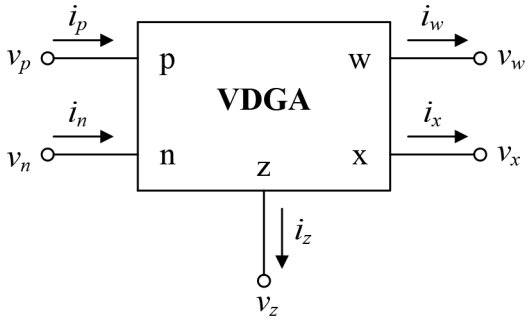

Figure 1. Circuit symbol of the VDGA.

$$\begin{bmatrix} i_p \\ i_n \\ i_z \\ i_x \\ v_w \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ g_{mA} & -g_{mA} & 0 & 0 \\ 0 & 0 & g_{mB} & 0 \\ 0 & 0 & \beta & 0 \end{bmatrix} \begin{bmatrix} v_p \\ v_n \\ v_z \\ v_x \end{bmatrix} \tag{1}$$

The CMOS realization of the VDGA by three tunable transconductors (M_{1A}–M_{9A}, M_{1B}–M_{9B}, and M_{1C}–M_{9C}) is shown in Figure 2 [15,16]. Each of them forms three independent tunable transconductance gains g_{mA}, g_{mB}, and g_{mC}. The value of g_{mk} ($k = A,\ B,\ C$) can be approximately determined by [18]

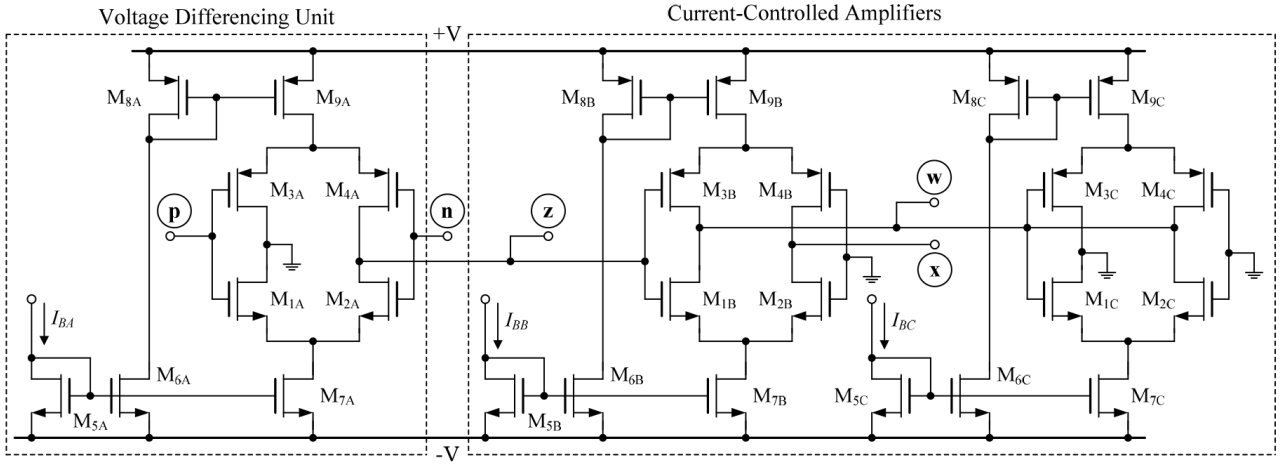

Figure 2. CMOS realization of the VDGA.

$$g_{mk} \cong \left(\frac{g_{1k}g_{2k}}{g_{1k}+g_{2k}}\right) + \left(\frac{g_{3k}g_{4k}}{g_{3k}+g_{4k}}\right), \tag{2}$$

where $g_{ik} = \sqrt{\frac{I_{Bk}\mu C_{ox}W_i}{2L_i}}$ is the transconductance parameter of the MOS transistor M_{ik} ($i = 1, 2, 3, 4$), I_{Bk} is the external DC bias current, μ is the free carrier mobility in the channel, C_{ox} is the gate-oxide capacitance

per unit area, and W_i and L_i are the channel width and length of the MOS M_{ik}, respectively. It is crucial to note from Eq. (2) that the transconductance g_{mk} can be tuned electronically by its bias current I_{Bk}.

From Figure 2, the transconductance cell M_{1A}–M_{4A} performs the differential-input voltage to current converter ($i_z = g_{mA}(v_p - v_n)$), while the transconductance cell M_{1B}–M_{4B} converts the voltage v_z to the output current i_x of the VDGA ($i_x = g_{mB}v_z$). In addition, the current-controlled voltage amplifier is formed from a pair of independent transconductance cells M_{1B}–M_{4B} and M_{1C}–M_{4C} for the voltage amplifying action ($v_w = \beta v_z$). The voltage transfer gain β of this stage is given by the following relation:

$$\beta = \frac{g_{mB}}{g_{mC}} \tag{3}$$

3. Proposed quadrature oscillator configuration

The configuration for the realization of the proposed sinusoidal quadrature oscillator using only one VDGA, one grounded resistor, and two grounded capacitors is shown in Figure 3. The proposed circuit employs a low-component count and all grounded passive components, thereby making it suitable for further integration and eliminating various parasitic impedance effects. Routine circuit analysis shows that the characteristic equation realized by this oscillator can be written as

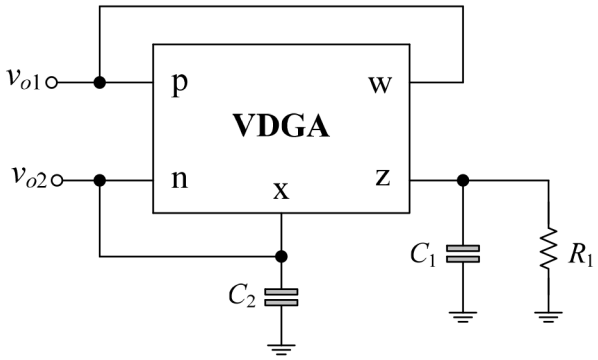

Figure 3. Proposed single VDGA-based sinusoidal quadrature oscillator.

$$s^2C_1C_2 + sC_2\left(\frac{1}{R_1} - \frac{g_{mA}g_{mB}}{g_{mC}}\right) + g_{mA}g_{mB} = 0. \tag{4}$$

This results in the oscillation condition and the oscillation frequency (ω_o) as, respectively,

$$g_{mC} = g_{mA}g_{mB}R_1, \tag{5}$$

and

$$\omega_o = 2\pi f_o = \sqrt{\frac{g_{mA}g_{mB}}{C_1C_2}}. \tag{6}$$

Eq. (5) indicates that the oscillation condition can be varied by controlling g_{mC} (I_{BC}) without affecting the ω_o. From Eq. (6), the ω_o can be tuned separately of the oscillation condition by g_{mA} and/or g_{mB} (I_{BA} and/or I_{BB}). Therefore, the proposed compact oscillator in Figure 3 exhibits an independent electronic adjustment of the oscillation condition and ω_o through the biasing currents of the VDGA.

For simplicity, assume the identical values of $g_{mo} = g_{mA} = g_{mB}$ ($I_{BO} = I_{BA} = I_{BB}$) and $C = C_1 = C_2$; then the parameter ω_o in Eq. (6) is modified to

$$f_o = \frac{g_{mo}}{2\pi C}. \tag{7}$$

This implies that the frequency of oscillation f_o can be tuned linearly and electronically by means of g_{mo} through adjusting the bias current I_{BO}.

Also from the configuration of Figure 3, the two marked output voltages v_{o1} and v_{o2} are related as

$$v_{o1} = \frac{j\omega C_2}{g_{mC}} v_{o2}, \tag{8}$$

which represents a 90° phase difference between the two voltages. This confirms that the voltages v_{o1} and v_{o2} are in quadrature.

In order to stabilize the output amplitude and to minimize the distortion inherent, an automatic gain control (AGC) circuit is necessary [7,19]. Since the VDGA element used in the proposed oscillator consists of a transconductance amplifier and voltage amplifier as output stages, the precise AGC circuit for the amplitude stabilization suggested in [7] can be utilized.

4. Nonideal transfer gain analysis and sensitivity study

In contrast to the ideal case, the practical VDGA can be characterized by considering the nonideal transfer gains. Therefore, the defining relation for the practical VDGA gets changed to

$$\begin{bmatrix} i_p \\ i_n \\ i_z \\ i_x \\ v_w \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \alpha_A g_{mA} & -\alpha_A g_{mA} & 0 & 0 \\ 0 & 0 & \alpha_B g_{mB} & 0 \\ 0 & 0 & \delta\beta & 0 \end{bmatrix} \begin{bmatrix} v_p \\ v_n \\ v_z \\ v_x \end{bmatrix}, \tag{9}$$

where α_k and δ refer to the transconductance inaccuracy factor and the nonideal voltage transfer gain, respectively. The effect of the VDGA nonidealities on the proposed circuit is analyzed using Eq. (9), and found to modify the oscillation condition and ω_o as follows:

$$g_{mC} = \delta\alpha_A g_{mA} g_{mB} R_1 \tag{10}$$

and

$$\omega_o = \sqrt{\frac{\alpha_A \alpha_B g_{mA} g_{mB}}{C_1 C_2}}. \tag{11}$$

Note from above expressions that the nonideal gains of the VDGA slightly modify the oscillation condition and ω_o of the oscillator. However, the small deviations in the oscillation condition and the ω_o-value can be simply compensated by predistorting the values of g_{mC}, and g_{mA} and/or g_{mB}, respectively.

From Eq. (11), the sensitivity analysis for the oscillator's ω_o is found to be

$$S_{\alpha_A}^{\omega_o} = S_{\alpha_B}^{\omega_o} = S_{g_{mA}}^{\omega_o} = S_{g_{mB}}^{\omega_o} = \frac{1}{2} \tag{12}$$

and

$$S_{C_1}^{\omega_o} = S_{C_2}^{\omega_o} = -\frac{1}{2} \tag{13}$$

From Eqs. (12) and (13), the magnitude of all ω_o-sensitivities with respect to active and passive components as well as to various nonideal gains is within 0.5, which is a low sensitivity figure.

5. Parasitic impedance effects

For a complete nonideal analysis, it is useful to determine the influence of the parasitic impedances of the VDGA on the performance of the proposed circuit in Figure 3. Considering the corresponding terminal parasitic impedance of the VDGA device, it can be realized that $(R_p//C_p)$, $(R_n//C_n)$, $(R_z//C_z)$, and $(R_x//C_x)$ are the equivalent impedances existing at the terminals p, n, z, and x, respectively, and R_w is the finite output resistance at the terminal w. Including these parasitic impedances, the nonideal small-signal model of the proposed oscillator given in Figure 3 can be represented in Figure 4. Thus, nonideal analysis for the circuit in Figure 4 gives respectively the following expressions for the oscillation condition and ω_o:

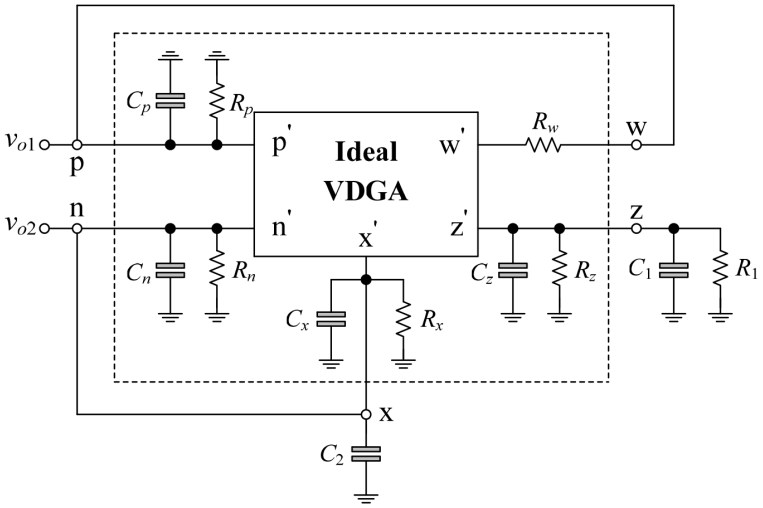

Figure 4. Nonideal small-signal model of the proposed quadrature oscillator in Figure 3.

$$g_{mC}\left(\frac{1}{R_1'} + \frac{C_1'}{R_2'C_2'}\right) = g_{mA}g_{mB} \tag{14}$$

and

$$\omega_o = \sqrt{\left(\frac{g_{mA}g_{mB}}{C_1C_2}\right)\left(1 - \frac{1}{g_{mC}R_2'}\right)}, \tag{15}$$

where $R_1' = (R_1//R_z)$, $R_2' = (R_n//R_x)$, $C_1' = (C_1//C_z)$, and $C_2' = (C_2//C_n//C_x)$. In practice, the values of external resistor R_1 and capacitors C_1 and C_2 are considered such that $(R_1 << R_z)$, $(C_1 >> C_z)$, and $(C_2 >> C_n, C_x)$. Consequently, it is obvious that $R_1' \cong R_1$, $C_1' \cong C_1$, and $C_2' \cong C_2$. It can be concluded from Eqs. (14) and (15) that the oscillation condition and ω_o of the proposed oscillator get altered by the parasitic impedances of the VDGA device. For example, if $g_{mA} = g_{mB} = g_{mC} = 200$ μA/V, $C_1 = C_2 = 10$ pF, $R_n = 450$ kΩ, and $R_x = 165$ kΩ, the percentage error in the ω_o is found to be 2.10%.

6. Performance simulations and discussions

The functionality of the proposed quadrature oscillator in Figure 3 has been evaluated with PSPICE simulation. The CMOS VDGA structure given in Figure 2 was simulated with the TSMC 0.35-μm CMOS process parameters. The dimensions of the CMOS transistors are listed in Table 2. The supply voltages used were +V = –V = 1.5 V.

Table 2. Dimensions of the CMOS transistors in Figure 2.

Transistors	W (μm)	L (μm)
M_{1k}–M_{2k}	16.1	0.7
M_{3k}–M_{4k}	28	0.7
M_{5k}	7	0.7
M_{6k}–M_{7k}	8.5	0.7
M_{8k}–M_{9k}	21	0.7

As example to obtain the oscillation frequency of f_o = 3.02 MHz, the proposed quadrature oscillator in Figure 3 was designed with the following component values: $g_{mA} = g_{mB} = g_{mC}$ = 0.19 mA/V ($I_{BA} = I_{BB} = I_{BC}$ = 10 μA), R_1 = 5.3 kΩ, and $C = C_1 = C_2$ = 10 pF. By performing transient simulations, the derived waveforms for quadrature outputs v_{o1} and v_{o2} are simultaneously given in Figure 5. From this graph, the quadrature phase difference was measured to be equal to 88°. In regard to the oscillation frequency, the simulated f_o was about 3 MHz, which is very close to the theoretically calculated value. The quadrature voltage property is further verified by the Lissajous figure (the x–y plot) of the two voltage outputs as shown in Figure 6. The simulated frequency spectrums for the quadrature output waveforms are also plotted in Figure 7, where the corresponding total harmonic distortion (THD) at quadrature outputs v_{o1} and v_{o2} were 0.888% and 0.618%, respectively. In addition to the simulation results, the total power consumption was found to be 0.73 mW.

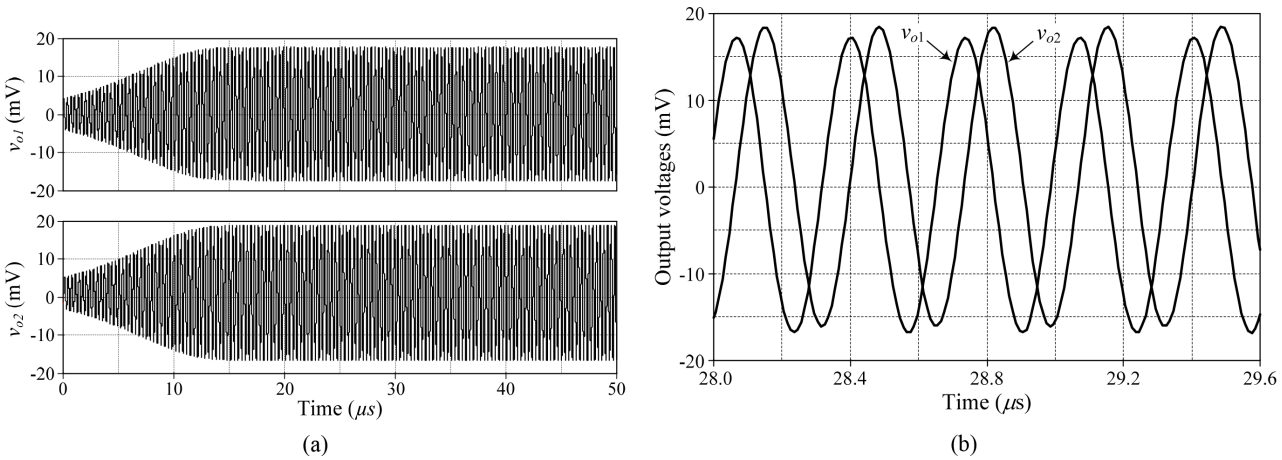

Figure 5. Simulated time-domain responses of quadrature outputs v_{o1} and v_{o2}: (a) initial state; (b) steady-state.

Next, the electronic control property of f_o without affecting the condition of oscillation is also performed for the above designed component values with a variable g_{mo}. The simulation result of noninteractive f_o tuning is given in Figure 8. The phase difference between the quadrature outputs v_{o1} and v_{o2} was further measured through simulations, and the percentage error in phase was also calculated. The results are plotted in Figure 9, which demonstrate quite small phase error deviated from 90°-phase shift.

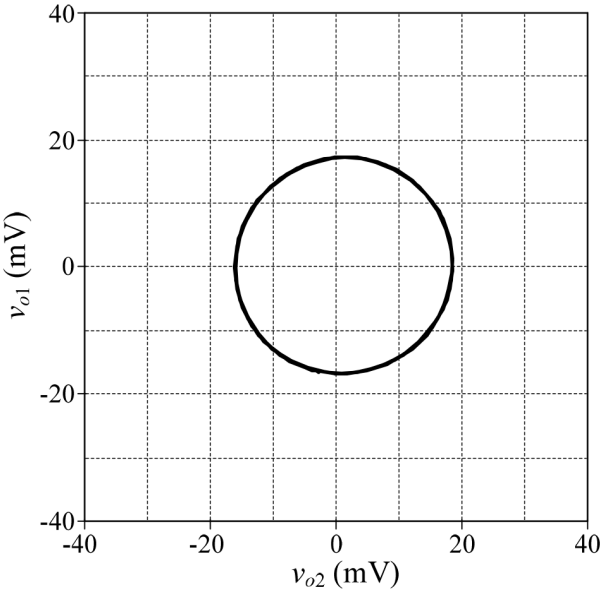

Figure 6. Lissajous curve for quadrature outputs v_{o1} and v_{o2} at f_o.

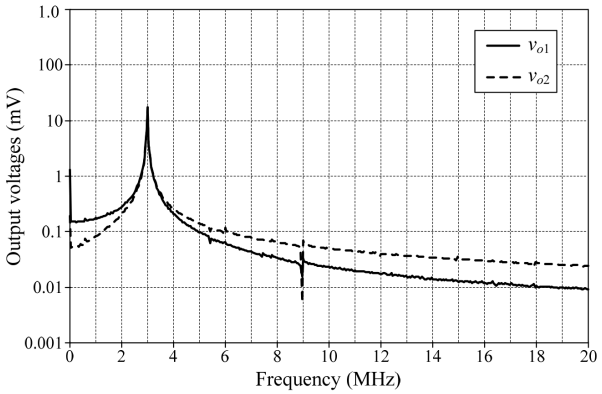

Figure 7. Simulated frequency spectrums of quadrature outputs v_{o1} and v_{o2}.

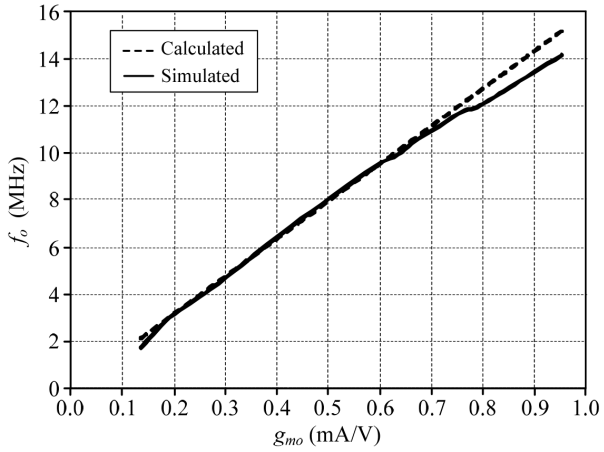

Figure 8. Electronic tuning of f_o with g_{mo}.

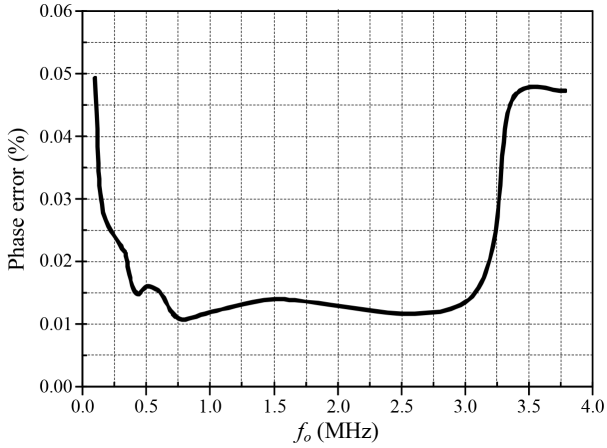

Figure 9. Phase error between v_{o1} and v_{o2} as a function of f_o.

Table 3 summarizes the measurement of the values of the percentage THD and output signal amplitudes for different supply voltage levels and two different oscillation frequencies. Obviously, the THD value increases when the supply voltage level increases. For example, for $\pm$V = 1 V and f_o = 302 kHz, the THD values at v_{o1} and v_{o2} are obtained as 0.204% and 0.123%, respectively. When the f_o-value is increased to 3.02 MHz, the THD values of output signals are also increased to 0.590% and 0.452%. It can also be observed that the v_{o2} output always has a higher amplitude compared with v_{o1} output for all supply voltage levels and oscillation frequencies.

The impact of the active and passive component variations on the oscillation frequency has been investigated by performing a Monte Carlo statistical analysis. After performing 100 runs, the derived histograms of the f_o for 5% Gaussian variations in transconductance and capacitor values are given in Figure 10.

Table 3. THD values and amplitude of output signals of Figure 3 for different power supply levels.

Supply voltages (V)		f_o = 302 kHz ($I_{BA} = I_{BB} = I_{BC}$ = 10 μA, C = 0.1 nF)				f_o = 3.02 MHz ($I_{BA} = I_{BB} = I_{BC}$ = 10 μA, C = 10 pF)			
+V	–V	THD (%)		Amplitude (mV_{p-p})		THD (%)		Amplitude (mV_{p-p})	
		v_{o1}	v_{o2}	v_{o1}	v_{o2}	v_{o1}	v_{o2}	v_{o1}	v_{o2}
+2.50	–2.50	3.493	2.51	21.625	22.263	1.749	1.115	20.867	21.446
+2.25	–2.25	1.705	1.240	20.81	21.353	1.093	1.602	18.996	19.397
+2.00	–2.00	1.233	1.446	19.920	20.364	1.093	1.602	18.996	19.397
+1.75	–1.75	1.583	1.498	19.043	19.397	0.546	0.509	18.050	18.360
+1.50	–1.50	0.724	0.567	18.084	18.347	0.888	0.618	16.870	17.313
+1.25	–1.25	0.560	0.261	16.446	17.002	0.995	0.732	14.430	15.565
+1.00	–1.00	0.204	0.123	14.596	14.683	0.590	0.452	7.709	7.766

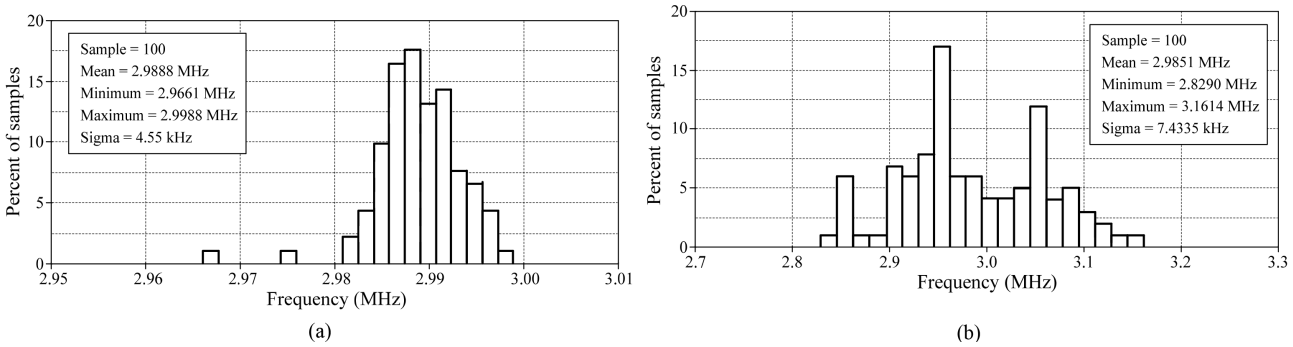

Figure 10. Monte Carlo analysis results for the fo: (a) 5% for variation in gmo-values; (b) 5% for variation in capacitor values.

7. Conclusions

This work presents a compact voltage-mode quadrature oscillator using one VDGA, one grounded resistor, and two grounded capacitors. The oscillation condition and the oscillation frequency of the proposed oscillator are independent and can be tuned electronically by separate bias currents. The effects of the VDGA nonidealities are investigated. Simulation results using the 0.35-μm CMOS real process parameters from TSMC are also provided to confirm the correct workability of the proposed quadrature oscillator.

Acknowledgements

This work was supported by Faculty of Engineering, Rajamangala University of Technology Isan, Khon Kaen Campus. The support in part by Faculty of Engineering, King Mongkut's Institute of Technology Ladkrabang (KMITL) is also gratefully acknowledged.

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