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An ultralow power, 0.003-mm^2 area, voltage to frequency-based smart temperature sensor for –55 °C to +125 °C with one-point calibration

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Abstract: With the scaling of transistor feature size and increased integration density, power density has increased, resulting in high chip temperature, thus degrading the performance and lifetime of the chip. In this work, an ultralow power smart temperature sensor employing a frequency locked loop technique is developed in 65 nm standard CMOS process. The circuit works on the principle of voltage to frequency conversion, exploiting the thermal dependency of threshold voltage (V_{th}) of MOS transistors in the subthreshold region. The sensor along with signal conditioning subcircuits has a low power consumption of 1.92 μW, while operating over –55 °C to +125 °C with a conversion rate of 10K samples/s. The output frequency corresponding to temperature has its temperature coefficient insensitive to process variation and therefore requires one-point calibration. Due to the simple signal conditioning circuitry, the sensor consumes an estimated area of 0.003 mm^2. Since the sensor has all its subcircuits working in the subthreshold region, it is suitable for low power applications.

Key words: Smart temperature sensor, dynamic thermal management, frequency locked loop, calibration, switched capacitor, voltage controlled oscillator

1. Introduction

The constant rise in performance demands of multiprocessor system-on-chips (MPSoCs) has led to more aggressive scaling techniques and increased transistor integration capacity. As a result, the power density and junction temperature gradient corresponding to ambient temperature of these SoCs is continuously increasing, as shown in Figure 1. These higher power densities and junction temperature variations degrade the reliability, lifetime, and performance, while increasing the timing issues, leakage power, gate delay, interconnect resistances, and cost of MPSoCs [1]. Chip failures of more than 50% happen due to thermal issues [2]. According to the International Technology Roadmap for Semiconductors (ITRS) estimates, the junction power density of high performance chips increases from 50 W/cm^2 at 100 nm to 100 W/cm^2 at 14 nm and for 3-D stacked integrated chips (ICs) it could be approximately 500 W/cm^2 [3]. Therefore, management of temperature has become an important concern in today's electronic system design. In this regard, different thermal management techniques, both on-chip as well as off-chip, were introduced that involve design of "smart" temperature sensors for online tracking of chip temperature. The design of high performance signal conditioning circuits for temperature sensors allow a wider deployment of on-chip sensors for better characterization of thermal activity at finer resolutions.

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In addition to low-cost and high performance, the power consumption of smart temperature sensors should be minimum for low battery-powered portable systems.

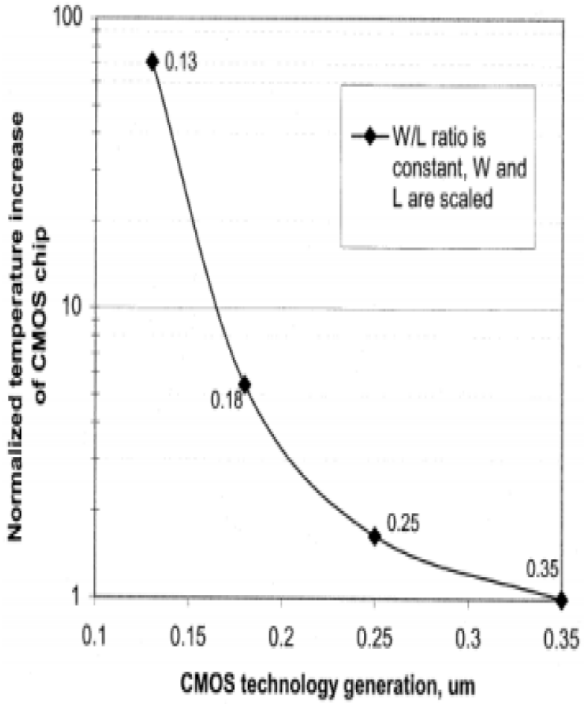

Figure 1. Normalized junction temperature increase in CMOS chip [3].

A variety of temperature sensors have been reported based on the thermal dependency of MOS transistors [4], resistors [5], bipolar transistors [6], and thermal delay lines [7]. The output of these sensors is usually analogue: temperature dependent current, voltage or frequency, operating in military range (–55 °C to +125 °C) with typical inaccuracy of ±2 °C. To improve the accuracy of these circuits, various readout circuits are used for calibration, which result in increased cost, area, and power consumption. The bipolar transistors were able to generate the sensing signal stably with greater sensitivity, but due to their demand of advanced calibration techniques and nonlinear dependency with temperature, they required bulky output interfaces. This resulted in trade-off between power dissipation, temperature inaccuracy, and sensor size. To overcome these issues, MOSFET-based time to digital converter temperature sensors were introduced [4]. These circuits generated frequency proportional to temperature, hence avoiding the use of expensive analogue to digital converters (ADCs) [8]. The MOSFET-based temperature sensors required two point calibration because of increased nonlinearity in their sensing signals, resulting in more power consumption, area, and cost. Furthermore, a temperature to frequency-based sensor working in the subthreshold region with single calibration was introduced in [9]. The control amplifier employed in [9] for a reference signal raised the stability issues over the temperature range due to the introduction of multiple poles, besides the area and power consumption. Moreover, the sensitivity and delay of switched capacitors (SCs) are not addressed, resulting in variations in capacitors, thus increasing the inaccuracy. To solve these problems, a temperature sensor is developed that operates with low power dissipation and requires one-point calibration. In this paper, a time domain-based CMOS smart temperature sensor is realized using 65 nm standard CMOS process. The sensor exploits the thermal dependency of threshold voltage of MOSFET transistors. The dependency of threshold voltage (V_{TH}) and

gain factor (β) of the MOS transistors on temperature is explained by Eq.(1) [8]. The variation in threshold voltage with temperature is depicted in Figure 2.

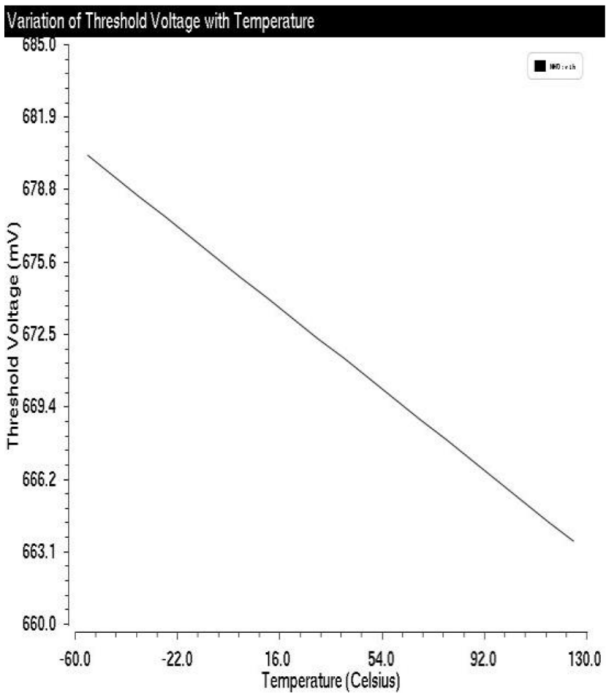

Figure 2. Variation of Vth for nMOS device with temperature.

$$\frac{\Delta I_{out}}{I_{out}} = \left(\frac{1}{\beta}.\frac{\partial \beta}{\partial T} + \frac{2}{V_{TH}}.\frac{\partial V_{TH}}{\partial T}\right) \tag{1}$$

where V_{TH} and β are technological parameters for n-channel transistors.

The main contributions of this work are as follows:

- Temperature to frequency-based smart temperature sensors using circuits in weak inversion region, designed for military applications (–55 °C to +125 °C).
- Low power consumption 1.92 μW at 10K samples/s and very compact area (0.003 mm^2) is achieved, resulting in improvement of greater than 72% of present implementations.
- Single calibration is required.
- Easy integration in any VLSI layout for dynamic thermal management (DTM) techniques.

The structure of this paper is as follows: section 2 explains the working principle of the sensor designed. Various effects of process, supply voltage, and temperature variations are discussed also. In section 3, the functionality of the developed prototype is validated using postlayout simulation results. A relative comparison with similar works is presented in section 4 and finally section 5 contains the conclusion.

2. Circuit description

2.1. Working principle

The functional block diagram of the temperature sensor is shown in Figure 3. It employs the frequency-loop technique to generate the desired proportional to absolute temperature (PTAT) frequency. The various blocks

of the temperature sensor are as follows: the PTAT current generator, current subtractor with an integrator, a voltage controlled oscillator (VCO), and a frequency to current converter. In this circuit, the feedback loop is implemented through an integrator, subtractor, frequency to current converter, and VCO. The overall circuit operates as follows: the output currents I_{PTAT} and I_{OUT} generated from the PTAT current source and frequency to current converter respectively are given to a subtractor. The integrator integrates the difference of I_{PTAT} and I_{OUT} to give the output voltage (V_{OUT}). This V_{OUT} is proportional to the difference between I_{PTAT} and I_{OUT} and is used for biasing the current starved VCO for providing oscillations of frequency f_{PTAT} proportional to V_{PTAT}.The frequency to current converter used in the feedback loop generates I_{OUT} from f_{PTAT}, which is again given to the subtractor. This feedback process continues and every time the V_{OUT} is readjusted and f_{PTAT} keeps on varying proportional to absolute temperature.

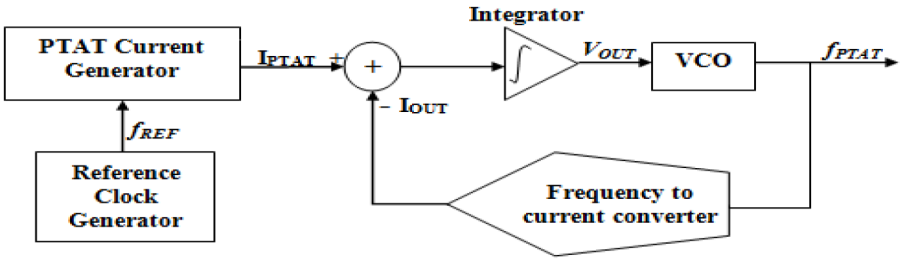

Figure 3. Functional block diagram of on-chip temperature sensor.

2.2. Complete circuit configuration

The complete circuit configuration of the temperature sensor is shown in Figure 4. Two cascaded inverters are used to get nonoverlapping clock signals of f_{PTAT}. These two signals drive the switched capacitors of the frequency to current converter. The PTAT switched capacitors are driven by the nonoverlapping signals of reference frequency f_{ref}. The aspect ratio of the inverters used in the current starved ring oscillator (CSRO) is 4:1 (i.e. $(W/L)_P = 8\,\mu m/0.44\,\mu m$, $(W/L)_N = 2\,\mu m/0.44\,\mu m$) and that of M_6 and M_5 of the PTAT generator is 5:1.

The circuit is divided into four stages: stage I is the frequency to current converter followed by the current subtractor and integrator in stage II. Stage III consists of the I_{PTAT} generator and stage IV includes the VCO. In order to reduce power consumption all the subcircuits are working in the subthreshold region. The details of these stages are given below.

2.2.1. Stage I: frequency to current conversion

The frequency-to-current converter is used to get the output current I_{OUT}, which is proportional to the output oscillation frequency f_{PTAT} obtained from the VCO. The switches of the SC resistor, with resistance $(C_1.f_{PTAT})^{-1}$, are driven by using the nonoverlapping pulses of f_{PTAT}. The output current (I_{OUT}) is given by

$$I_{OUT} = \frac{V_{ref}}{R_B} = C_1 f_{PTAT} V_{ref} \tag{2}$$

The I_{OUT} is fed back into the current subtractor using a current mirror. Due to the feedback operation, the PTAT current I_{PTAT} will be equal to the output current I_{OUT}, resulting in oscillations f_{PTAT}. The oscillation

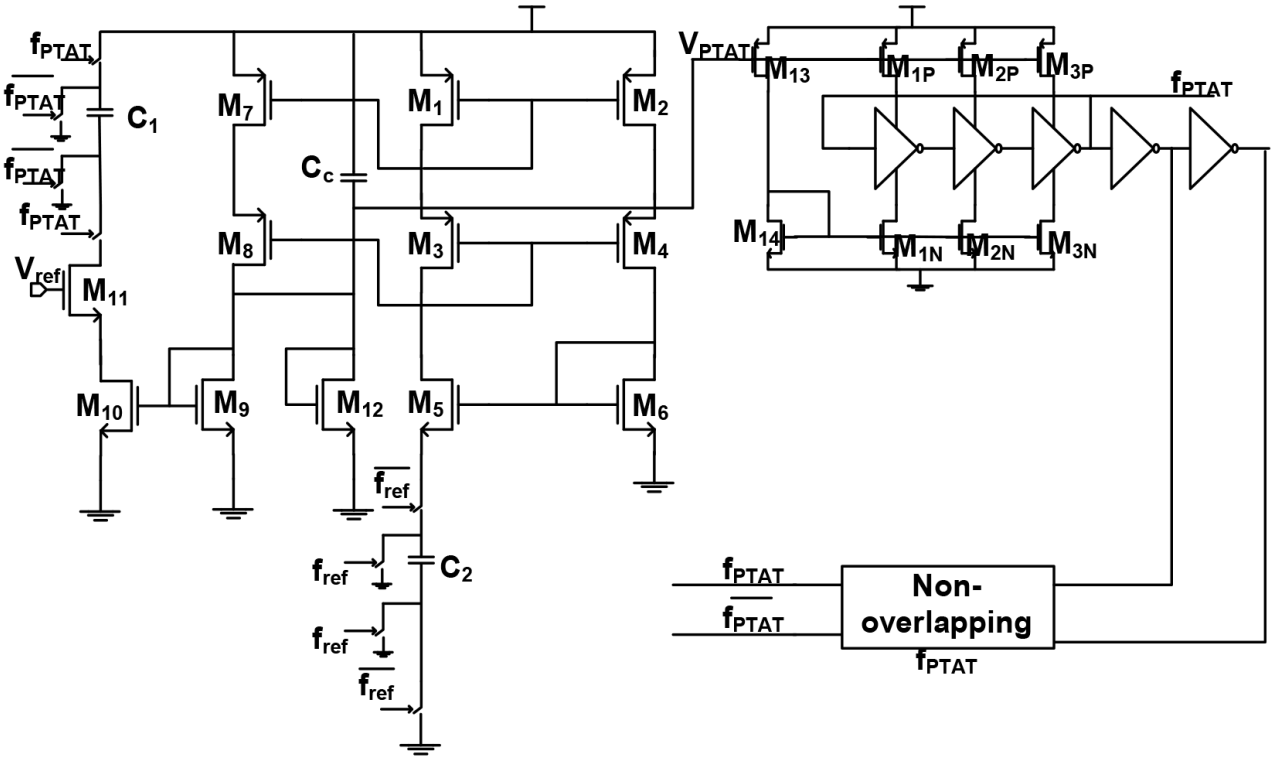

Figure 4. Entire circuit configuration of on-chip temperature sensor.

frequency f_{PTAT} is given by

$$f_{PTAT} = \frac{C_2}{C_1}\frac{f_{ref}}{V_{ref}}\frac{\eta K_B T}{q}\ln\left(\frac{K_2}{K_1}\right) \tag{3}$$

The external sources f_{ref} and V_{ref} used here can be clock reference generators or crystal oscillators and bandgap references, respectively. Since these external references are independent of temperature variations, the f_{PTAT} will exhibit PTAT characteristics. Due to the positive feedback, the stability of the PTAT circuit is assured as long as loop gain is less than unity, which is possible only if $\left(W/L\right)_5 \Big/ \left(W/L\right)_6 > 1$ [10]. The PTAT circuit can have another stable state, when the current flowing through it is zero. To guarantee this condition does not occur, it is necessary to add a startup circuit that only affects the operation when all currents are zero at startup.

2.2.2. Stage II: subtractor and integrator

The I_{PTAT} generated from the PTAT current generator and the output current I_{OUT} from the frequency to current converter are given to the current subtractor, which detects the difference between these two currents. In order to get the corresponding voltage, V_{OUT}, the difference current signal is given to the integrator for integration. Therefore, the resultant V_{OUT} from the integrator will be proportional to the difference of I_{PTAT} and I_{OUT}. The carefully designed capacitor C_C, shown in Figure 4, makes the feedback loop stable by forming a loop filter of frequency locked loop. The C_C also behaves as a startup circuit, reducing the startup time of the sensor. Transistor M_{12}, shown in Figure 4, is used to minimize the leakage current at high temperatures and to limit the startup current.

2.2.3. Stage III: PTAT current generator

The circuit configuration employed here as a PTAT current generator is the same as that described in [10], shown in Figure 5, where the circuit is used for biasing an operational amplifier to have stable transconductance, operating in a saturation region. In this work, this circuit is designed in the weak inversion region to generate an output current, where the resistor is realized using SCs [10]. The SC implemented here is parasitic insensitive and delay free whose switches (S_1 and S_4) are given the f_{ref}, whereas switches (S_2 and S_3) are given a nonoverlapping signal ($\bar{f_{ref}}$) of f_{ref}.

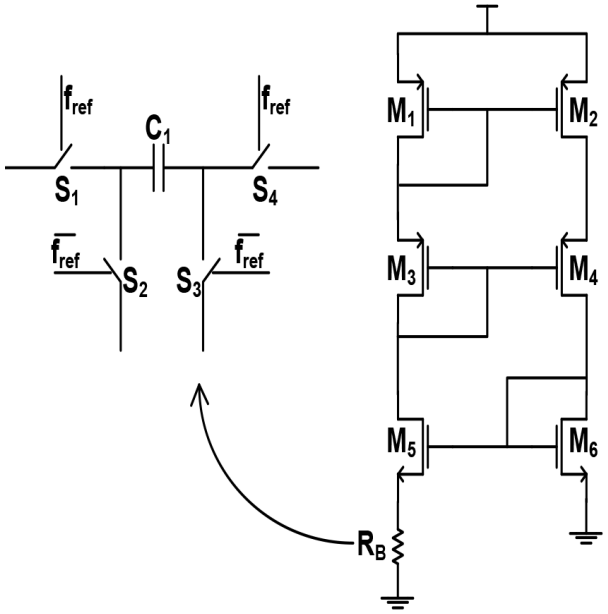

Figure 5. PTAT current generator.

In Figure 5, the geometrical ratios of M_1 and M_2 are equal; then $I_{D1} = I_{D2}$, and around the loop consisting of M_5, M_6, and R_B, we have

$$V_{GS6} = V_{GS5} + I_{PTAT}R_B \tag{4}$$

When a MOSFET is operating in the subthreshold region its drain current is an exponential function of the drain-source voltage V_{DS} and gate-source voltage V_{GS}, and is given by [10]

$$I_{DS} = I_{DO}\frac{W}{L}e^{-V_{BS}[(1/(\eta V_t))-(1/V_t)]}\left(1 - e^{\frac{-V_{DS}}{V_t}}\right)e^{(V_{GS}-V_T)/(\eta V_t)} \tag{5}$$

where V_T is the threshold voltage and $V_t = {}^{kT}/_{q}$, where k is the Boltzmann's constant (1.387×10^{-23} V. C/ °K), T is the temperature in degrees Kelvin, and q is the electronic charge (1.6×10^{-19} C). At room temperature $V_t = 26$ mV. The constants I_{DO} ($I_{DO} \approx 20\,nA$) and η ($\eta = 2$) are the process parameters. Under the assumption $V_{DS} > 3V_t$, Eq. (5) simplifies considerably to

$$I_{DS} = KI_{DO}e^{(V_{GS}-V_T)/(nV_t)} \tag{6}$$

and

$$I_{DO} \approx \frac{2K\left((\eta V_t)^2\right)}{e^2}, \tag{7}$$

where K is the aspect ratio.

2.2.4. Stage IV: voltage to frequency converter

Voltage to frequency (V/F) conversion is the most economical and simplest technique to obtain analogue-to-digital (A/D) conversion. Although V/F converters are slow when compared to A/D converters, they are quite appropriate for the majority of sensor applications. The output pulsed signals of V/F converters are less sensitive to a noisy environment than high resolution analogue signals. Ideally, the output frequency f_{OUT} of the V/F converter is directly proportional to the input voltage bias (V_{PTAT}), given by

$$\frac{f_{OUT}}{f_{FS}} = \frac{V_{ref}}{V_{FS}} \tag{8}$$

where f_{FS} and V_{FS} are the full-scale frequency and input voltage, respectively. For a given linear V/F converter, ratio f_{FS}/V_{FS}= G is constant and is called a conversion factor; therefore,

$$f_{OUT} = GV_{ref} \tag{9}$$

The V/F converter is realized by VCO, which employs a three-stage CSRO, operating in the subthreshold region of MOS transistors. The VCO generates frequency (f_{PTAT}), which is dependent on the V_{OUT}. The V/F converter is followed by two cascaded inverters to get nonoverlapping f_{PTAT} signals for the SCs, as shown in Figure 6. The I_{bias} controlled by the V_{OUT} defines the frequency of oscillations f_{PTAT} of the CSRO.

$$f_{PTAT} = \frac{I_{bias}}{2nAC_LV_{DD}} \tag{10}$$

where n is the number of stages (odd), C_L is the load capacitance, V_{DD} is the supply voltage, A is the delay fitting parameter, and I_{bias} is the bias current flowing through each inverter, and is given by

$$I_{bias} = I_o exp\left(\frac{V_{DD} - V_{OUT} - V_{TH}}{\eta V_T}\right) \tag{11}$$

2.3. Process and supply variation

Here the effect of process variation on the PTAT current generator, switched capacitors, and output frequency is analyzed. The process variation causes: 1) threshold voltage mismatch ($\Delta V_{TH} = V_{TH6} - V_{TH5}$) in the case of the PTAT current generator and, 2) variations in switched capacitors (C_1 and C_2). Using Eq. (4)

$$V_{GS6} = V_{GS5} + I_{PTAT}R_B \tag{12}$$

Since $I_5 = I_6$, therefore

$$V_{GS} = (\eta V_T)\, ln\left({}^{I_{DS}}/_{KI_{D0}}\right) + V_{TH} \tag{13}$$

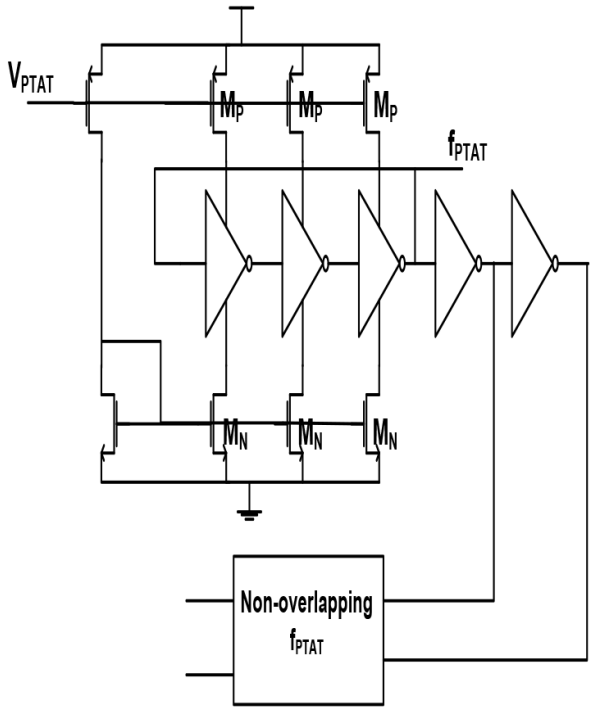

Figure 6. 3-stage current starved VCO.

Put this value in Eq. (12) and $R_B = (C_1 \cdot f_{ref})^{-1}$ we get

$$I_{PTAT} = \eta V_T \cdot ln\left(K_2/K_1\right) \cdot (C_1 \cdot f_{ref}) \tag{14}$$

Due to the threshold voltage mismatch, the variation in I_{PTAT} is

$$I_{PTAT\_var} = \eta V_T \cdot ln\left(K_2/K_1\right) \cdot (C_1 \cdot f_{ref}) + (C_1 \cdot f_{ref})\,\Delta V_{TH} \tag{15}$$

The additional term on the right side of Eq. (15) defines the threshold mismatch causing an offset in output current. The PTAT current generator can be stabilized using [10], in which the transconductance of transistors is matched with the conductance of resistors. Due to this, the transistor's transconductance will be independent of temperature and process as well as power supply voltage variations.

Following Eq. (12), the variation in output frequency due to process variation is given as

$$f_{PTAT} = \frac{C_2}{C_1}\frac{f_{ref}}{V_{ref}}\frac{\eta K_B T}{q}\ln\left(\frac{K_2}{K_1}\right) + \frac{C_2}{C_1}\frac{f_{ref}}{V_{ref}}\frac{\eta K_B T}{q}\Delta V_{TH} \tag{16}$$

The temperature coefficient (TC) of the output frequency is independent of process variation as the C_2/C_1 is insensitive to process variation. The delay of the CSRO is

$$t_p = \frac{2C_L V_T}{\mu C_{ox}\left(W/L\right)(V_{DD} - V_T)^2} + \frac{C_L}{\mu C_{ox}\left(W/L\right)(V_{DD} - V_T)} \cdot ln\left(\frac{1.5V_{DD} - 2V_T}{0.5V_{DD}}\right), \tag{17}$$

where V_T is the threshold voltage, C_L is the load capacitance, and $\mu C_{ox}\left(W/L\right)$ is the transconductance. As Eq. (14) can be differentiated over a wide sensing range, its corresponding Taylor series expansion explains the relationship between supply voltage and linearity. It can be seen that the higher order terms that add nonlinearities can be suppressed using larger supply voltages, thus resulting in high linearity.

3. Results and discussion

The sensor is realized using 65 nm CMOS standard process. The layout of the smart sensor is depicted in Figure 7. The estimated chip area (including V/F converter, integrator, VCO, and PTAT current generator) is 0.003 mm^2, excluding input/output pads. For the purpose of excitation and comparison, a reference voltage of 550 mV and frequency of 10 MHz are given using ideal sources. The variation in V_{PTAT} with temperature is shown in Figure 8. It is concluded that the slope of voltage, V_{PTAT}, curve is changing by 45% with increase in temperature.

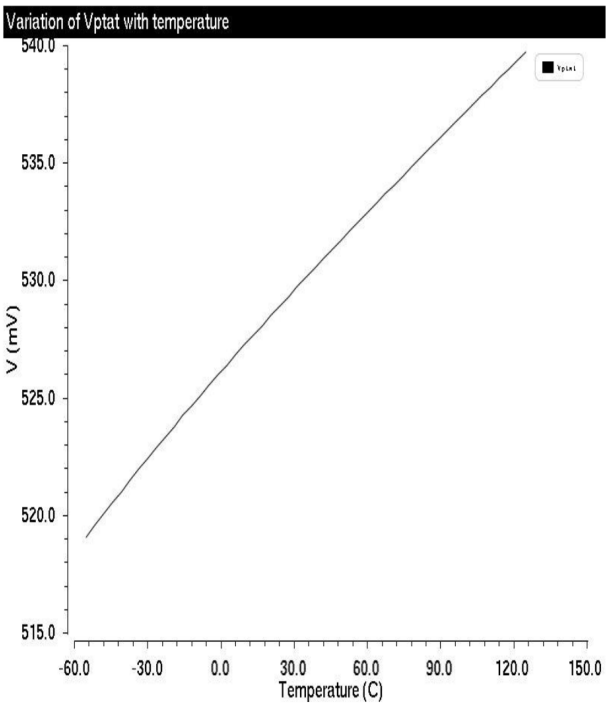

Figure 7. Layout of the proposed temperature sensor.

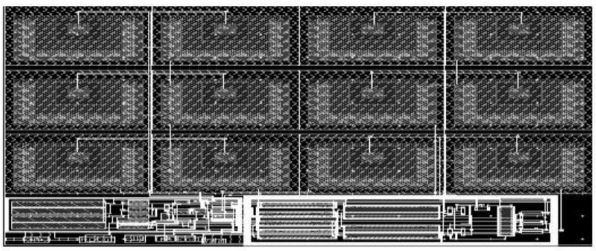

Figure 8. Variation in VPTAT with temperature.

The collective effects of process and environmental variations on the temperature to frequency-based sensor are observed at different process corners, namely typical–typical (TT), slow–slow (SS), fast–fast (FF), slow–fast (SF), and fast–slow (FS). The speed of each type of transistor, interconnect speed variations, and environmental variations are used to define process corners (TT, SS, FF, SF, FS), as shown in Figure 9. The variations in f_{PTAT} across all process corners are listed in Table 1. Under nominal conditions, the sensor generated a frequency of 801 KHz and 38.46 MHz at –55 °C to +125 °C, respectively. The effective resolution can be calculated using [11]

$$Resolution\ (^\circ) = \frac{X-Y}{Q-P}, \tag{18}$$

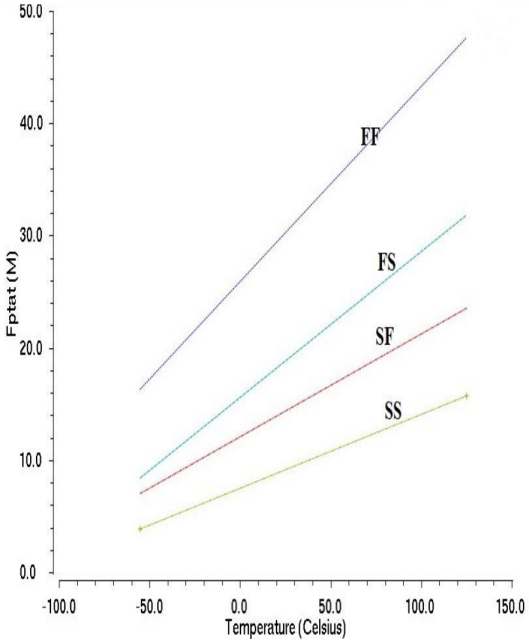

Figure 9. Temperature–frequency behavior at different process corners.

where P and Q are outputs at two temperatures Y and X, respectively. The effective resolution of the sensor under given conditions is 0.03 °.

Table 1. Process corner variation.

Temperature (°C)	Frequency (MHz)				
	FF	FS	SF	SS	TT
–55	16.3	8.3	7.0	3.8	0.80
27	30.4	19	14.5	9.2	10.1
125	47.6	31.8	23.5	15.7	38.4

3.1. Transient response

In order to verify the online temperature monitoring behavior of the sensor, the temperature and time are swept simultaneously from –55 to +125 °C and from 0 to 10 μs, respectively, and the variation in output frequency, f_{PTAT}, is observed. As shown in Figure 10, the f_{PTAT} increases with the increment in temperature after every clock cycle of 2 μs. Usually, the on-chip temperature keeps on increasing with time; however, due to some subcircuit failures, the chip temperature decreases. To illustrate this, after some increments in temperature a lower temperature is deliberately chosen at 6 μs to see the effect. As can be seen from Figure 10, the f_{PTAT} keeps on increasing up to 6 μs and then decreases. Therefore, the sensor can also be used to notify whether all subcircuits of SoCs are working properly or not. The runtime behavior of the sensor is summarized in Table 2.

3.2. Power consumption

The power consumption of the on-chip sensor should be as minimal as possible; otherwise it would lead to self-heating issues. Figure 11 shows the variation in power consumption with temperature. The power consumption varies from 154.9 nW to 8.8 μW for –55 °C to +125 °C, respectively. The power consumption exponentially increases with temperature.

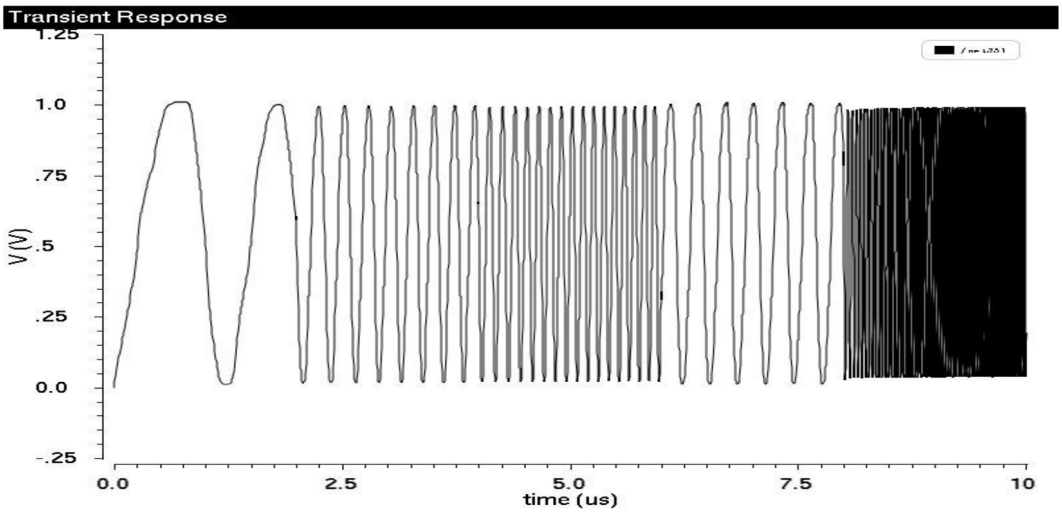

Figure 10. Transient response of temperature sensor.

Table 2. Runtime variation of frequency with temperature noted from Figure 10.

Time (μs)	Temperature (°C)	Frequency (MHz)
0–2	–55	0.81
2–4	0	5.67
4–6	27	10.1
6–8	–55	2.4
8–10	120	36.67

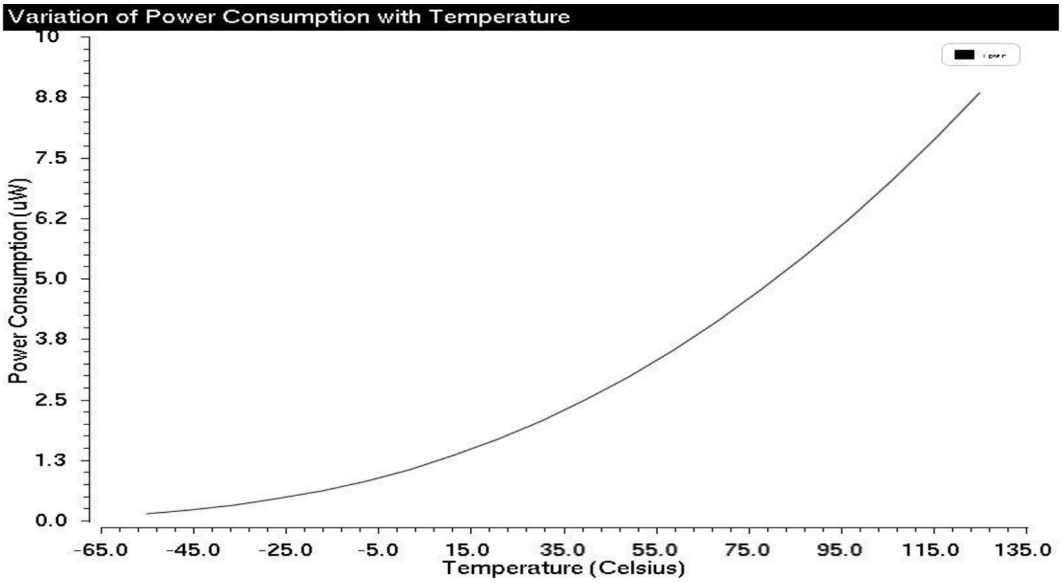

Figure 11. Variation in power consumption with temperature.

4. Comparison with previous works and discussion

The comparison of this work with previous smart temperature sensors is given in Table 3. The main advantages of the sensor, besides one-point calibration, are its small size and low power consumption. The sensor resulted

in an area of 0.003 mm^2 smaller than the prior topologies and the power consumption of 1.92 μW, surpassing the previous works by at least 72%. The reduction in sensor area and power consumption makes it highly resistant to spatial thermal gradients and self-thermal issues.

Table 3. Comparison with related works.

	This work*	[4]	[6]	[7]	[9]	[12]	[13]	[14]
Year	2015	2008	2010	2014	2011	2011	2013	2013
Sensor type	Sub. MOS	MOS	BJT	MOS	Sub. MOS	MOS	BJT	MOS
Temp. range (°C)	–55 to 125	0 to 100	–70 to 125	0 to 100	10 to 80	0 to 100	–55 to 125	0 to 110
CMOS tech. [nm]	65	180	65	45	350	220 /180	160	65
V_{DD} [V]	1	1	1.2	1	2.2–3	2.5	1.5–2	1
Resolution [°C]	0.03	0.3	0.03	0.097	0.2	0.133	0.005	0.94
Conv. rate [sample/s]	10K	100	2.2	N.A.	100	4.4K	100	469K
Calibration	1	2	1	1	1	1	1	1
Power consp. [μW]	1.92	0.2∼0.31	10	181.8	10–27	437.5	5.1	500
Area [mm^2]	0.003	0.05	0.1	0.001	0.08	N.A.	0.08	0.008

*Postlayout results

Since the results are based on the postlayout simulations carried in Cadence Virtuoso environment, the calibration issues present in the actual chip are not dealt with. In [12], an analytical approach for one-point calibration is explained. In [13], two techniques are reported: thermal and voltage calibration techniques. It was also concluded in [13] that voltage calibration is a good alternative to thermal calibration techniques.

5. Conclusions

In this paper, a tiny ultralow power MOSFET-based temperature sensor, working in the subthreshold region for a temperature range of –55 °C to +125 °C, was realized in 65 nm CMOS standard process. The sensor uses the frequency-locked loop technique for generating frequency proportional to absolute temperature. The use of simple signal conditioning circuitry instead of complex ADCs makes it compatible for most standard cell libraries. With the simple circuitry and subthreshold operation, the sensor succeeded in consuming an ultralow power of 1.92 μW with an area of 0.003 mm^2, thus outperforming at least 72% of the present topologies of temperature sensors. The sensor requires one-point calibration as it is insensitive to process variations. The minute size and low power consumption of the temperature sensor make it suitable for low power applications as well as runtime approaches of DTM applications.

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