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# A new sequential power flow algorithm for AC/DC systems including independent multiterminal DC subsystems

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**Abstract:** This paper presents a new algorithm based on the sequential method for power flow calculation in multiterminal AC/DC systems. The proposed approach differs from other similar studies in the literature by handling two main properties. Firstly, a real equivalent circuit model is considered for the under-load tap changer transformers (ULTCs) of DC converters for the first time in the literature. Hence, new DC equations are obtained. Thus, exact and accurate results can be obtained for practical applications using the proposed algorithm. Tap values adjustment effects of the ULTCs connected to DC converters are included into the Jacobian matrix instead of the bus admittance matrix in the sequential AC power flow algorithm, as well as other ULTCs in the AC system. For this aim, new equations for calculating power and Jacobian matrix elements are obtained. Secondly, more than one independent multiterminal DC subsystem in terms of DC connection is included in the study. DC power flow calculation is performed for each DC subsystem independently in the algorithm. Thus, modularity and flexibility are provided for including or removing any DC subsystems without needing to change the proposed algorithm. The proposed approach has been tested on a modified IEEE 20-bus AC/DC test system. The proposed AC/DC power flow algorithm was written and performed in MATLAB. The results show that the proposed approach is accurate and reliable in convergence.

**Key words:** Power flow, multiterminal, HVDC, AC/DC system, ULTC

## 1. Introduction

High-voltage direct current (HVDC) systems have been used in electrical power systems integrated to AC systems for a long time [1–5]. Many methods have been proposed for AC/DC power flow calculation in integrated AC/DC systems. These methods are separated into two main categories: the simultaneous method and the sequential method. In the simultaneous method, AC and DC equations are within each other and solved together [6–9]. In the sequential method, AC and DC equations are solved in separate power flow algorithms and convergence is provided by going forwards and backwards between these sequential algorithms. The sequential AC/DC power flow algorithm is structured by independent AC and DC power flow algorithms. The sequential AC/DC power flow algorithms continue to be executed until the sequential AC and DC power flow algorithms following each other converge independently [10–13].

In both the simultaneous and sequential methods mentioned above, the main issue is obtaining the appropriate tap values of the DC converters' ULTCs to maintain DC power balance [14]. Generally, the obtained values of the ULTCs are out of the tap limits [15]. Sometimes the tap values are obtained in the limits,

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but they can lead to imaginary values for the control angles (firing angle for rectifier or extinction/recovery angle for inverter) [16,17]. Previous studies have overcome these problems efficiently. However, in all of these studies, the ULTCs of the DC converters are assumed to be ideal. Furthermore, the obtained tap values are not discrete, and they are regulated to the nearest discrete real value [18]. Hence, the results obtained by the existing studies cannot be valid for practical applications.

On the other hand, most of the existing studies cannot meet the general solution of power flow when the integrated AC/DC system includes more than one independent DC subsystem. These studies are done in the case of only one two-terminal or multiterminal DC subsystem in the system. Liu et al. [18] proposed a sequential AC/DC power flow algorithm that can include more than one independent DC subsystem. DC equations have been considered nonlinear and solved through the Newton–Raphson method. So, it is clear that each addition of DC converter to the system causes a nonlinear increase in the Jacobian matrix and DC power flow convergence time.

In this paper, a new sequential AC/DC power flow algorithm is proposed for multiterminal AC/DC systems. The traditional Newton–Raphson method is used for the sequential AC power flow algorithm and a linear current-balancing method is used for the sequential DC power flow algorithm. The real equivalent circuits for the ULTCs [19,20] of the DC converters, as well as the other ULTCs in the AC system, are used in the proposed AC/DC power algorithm in order to be valid for practical applications. Thus, a new equivalent circuit model for DC converter stations and new DC equations for DC power flow are obtained. On the other hand, apart from similar studies in the literature, real discrete tap values are obtained directly and the calculations are done for these values. Hence, the proposed approach prevents calculation errors caused by the regulation of continuous tap values to discrete values. The tap-changing effects of DC converters' ULTCs during the sequential DC power flow algorithm affect the AC power flow directly as the bus admittance matrix structure is changed. To avoid the rebuilding of the bus admittance matrix caused by this situation, new AC power equations and new Jacobian matrix element calculation equations are obtained. Thus, the tap-changing effects are included into the Jacobian matrix and rebuilding the bus admittance matrix for each tap changing case is prevented, leading to fast convergence. A sequential DC power flow algorithm based on a current-balancing method is executed separately for each DC subsystem. Thus, modularity is achieved for the proposed AC/DC power flow algorithm for including or removing any DC subsystem without needing to change the proposed algorithm. The proposed approach has been tested on a modified IEEE 20-bus AC/DC test system by MATLAB to demonstrate its accuracy and reliability.

## 2. The proposed sequential AC/DC power flow algorithm

This section presents the proposed sequential AC/DC power flow algorithm. Sequential AC/DC power flow calculation is performed going forwards and backwards between the proposed sequential AC and DC power flow algorithms.

### 2.1. The illustration of the sequential AC power flow algorithm

This section presents the proposed sequential AC power flow algorithm used in this AC/DC power flow study. The proposed AC power flow algorithm is based on the Newton–Raphson method. In this study, real equivalent circuit models are considered for the DC converters' ULTCs as well as the other ULTCs used in the AC system. The ULTC's model and its equivalent circuit are given in Figure 1 [21].

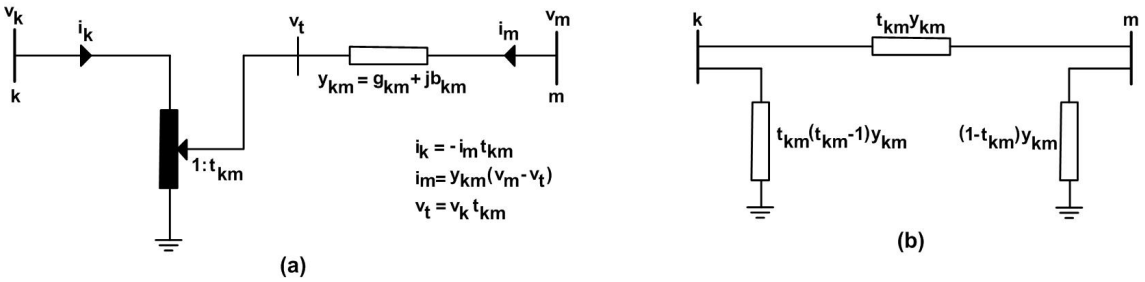


**Figure 1.** ULTC model a) representation of ULTC b) equivalent circuit of ULTC.

In Figure 1, $k$, $m$, $t_{km}$, and $y_{km}$ represent the bus that the ULTC's primary side is connected to, the bus that the ULTC's secondary side is connected to, the tap value of the ULTC, and the admittance of the ULTC's windings, respectively.

$$y_{km} = g_{km} + jb_{km} \tag{1}$$

As the tap values of the DC converters' ULTCs are changed in each sequential DC power flow iteration to achieve DC power balance in the study, the series and shunt admittance values of ULTCs change depending on the tap values (Figure 1). Thus, the bus admittance matrix of the AC system must be rebuilt for each new sequential AC power flow algorithm. To avoid rebuilding the AC bus admittance matrix for new ULTC tap values, only the ULTC's serial winding admittance $y_{km}$ is considered in the AC bus admittance matrix $y_{bus}$, and shunt admittances for bus $k$ and $m$ are considered zero. In these conditions, $p_k$, $q_k$, $p_m$, and $q_m$ (active power flowing from bus $k$ to other buses in the AC network, reactive power flowing from bus $k$ to other buses in the AC network, active power flowing from bus $m$ to other buses in the AC network, and reactive power flowing from bus $m$ to other buses in the AC network, respectively) can be given as follows:

$$\begin{aligned} p_k &= v_k \sum_{\substack{j=1 \\ j\neq k,m}}^{nb} v_j \left(g_{bus_{kj}} \cos\delta_{kj} + b_{bus_{kj}} \sin\delta_{kj}\right) + v_k v_m t_{km} \left(g_{bus_{km}} \cos\delta_{km} + b_{bus_{km}} \sin\delta_{km}\right) \\ &\quad + v_k^2 \left[g_{bus_{kk}} - \left(t_{km}^2 - 1\right) g_{bus_{km}}\right] \end{aligned} \tag{2}$$

$$\begin{aligned} q_k &= v_k \sum_{\substack{j=1 \\ j\neq k,m}}^{nb} v_j \left(g_{bus_{kj}} \sin\delta_{kj} - b_{bus_{kj}} \cos\delta_{kj}\right) + v_k v_m t_{km} \left(g_{bus_{km}} \sin\delta_{km} - b_{bus_{km}} \cos\delta_{km}\right) \\ &\quad + v_k^2 \left[-b_{bus_{kk}} + \left(t_{km}^2 - 1\right) b_{bus_{km}}\right] \end{aligned} \tag{3}$$

$$\begin{aligned} p_m &= v_m \sum_{\substack{j=1 \\ j\neq m,k}}^{nb} v_j \left(g_{bus_{mj}} \cos\delta_{mj} + b_{bus_{mj}} \sin\delta_{mj}\right) + v_m v_k t_{km} \left(g_{bus_{mk}} \cos\delta_{mk} + b_{bus_{mk}} \sin\delta_{mk}\right) \\ &\quad + v_m^2 g_{bus_{mm}} \end{aligned} \tag{4}$$

$$\begin{aligned} q_m &= v_m \sum_{\substack{j=1 \\ j\neq m,k}}^{nb} v_j \left(g_{bus_{mj}} \sin\delta_{mj} - b_{bus_{mj}} \cos\delta_{mj}\right) + v_m v_k t_{km} \left(g_{bus_{mk}} \sin\delta_{mk} - b_{bus_{mk}} \cos\delta_{mk}\right) \\ &\quad - v_m^2 b_{bus_{mm}} \end{aligned} \tag{5}$$

where $n_b$, $v_i$, $g_{bus_{ij}}$, $b_{bus_{ij}}$, and $\delta_{ij}$ represent the total number of buses in the AC system, the $i$th bus's voltage, the conductance value of $y_{bus}$'s $i$th and $j$th component, the susceptance values of $y_{bus}$'s $i$th and $j$th component, and the phase angle difference between $i$th and $j$th bus voltages, respectively.

The active and reactive powers flowing from the buses that are not connected to a ULTC (different from the buses k and m) to the other buses in the AC system are given as

$$p_i = v_i \sum_{j=1}^{nb} v_j \left( g_{bus_{ij}} \cos \delta_{ij} + b_{bus_{ij}} \sin \delta_{ij} \right) \tag{6}$$

$$q_i = v_i \sum_{j=1}^{nb} v_j \left( g_{bus_{ij}} \sin \delta_{ij} - b_{bus_{ij}} \cos \delta_{ij} \right) \tag{7}$$

The general bus representation for the AC/DC system used in this study is given in Figure 2.

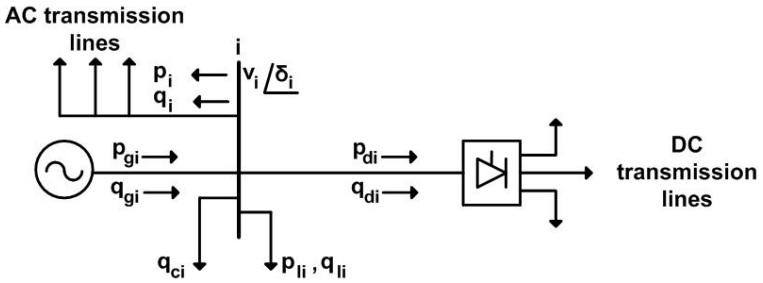


**Figure 2.** General bus representation for the AC/DC system.

In Figure 2, $p_{gi}$, $q_{gi}$, $p_{di}$, $q_{di}$, $p_{li}$, $q_{li}$, $q_{ci}$, $p_i$, and $q_i$ represent the active power of the $i$th bus's generator, the reactive power of the $i$th bus's generator, the active power of the DC converter connected to the $i$th bus, the reactive power of the DC converter connected to the $i$th bus, the active power of the $i$th bus's load, the reactive power of the $i$th bus's load, the reactive power of the shunt reactive power supply of the $i$th bus, the active power flowing from the $i$th bus to other buses in the AC system given by Eqs. (2,4,6), and reactive power flowing from the $i$th bus to other buses in the AC system given by Eqs. (3,5,7), respectively.

The active and reactive powers of the DC converters are considered constant loads in the sequential AC power flow algorithm for the buses where the DC converters are connected to them. The updated active and reactive powers of the DC converters at the end of the sequential DC power flow algorithm are sent to the sequential AC power flow algorithm. According to this approach, the power equations to be provided in the Newton–Raphson-based sequential AC power flow algorithm for the general bus representation given in Figure 2 are defined as

$$g_{pi} = p_i + p_{d_i} + p_{l_i} - p_{g_i} = 0 \quad (i = 2, \ldots n_b) \tag{8}$$

$$g_{qi} = q_i + q_d + q_{l_i} - q_{c_i} = 0 \quad (i = n_g + 1, \ldots n_b), \tag{9}$$

where $n_g$ represents the total number of generator buses in the system.

During the sequential AC power flow algorithm, the tap values of DC converters' ULTCs, which are changed in the sequential DC power flow algorithm, are considered control variables. Thus, the state and control variables for AC power flow algorithm are given as

$$x_{AC} = [\delta_2, \ldots, \delta_{nb}, v_{ng+1}, \ldots, v_{nb}] \tag{10}$$

$$u_{AC} = [p_{g2}, \ldots, p_{gng}, v_1, \ldots, v_{ng}, t_1 \ldots t_{nt}, t_{d_1} \ldots t_{d_{nd}}], \tag{11}$$

where $t$, $n_t$, $t_d$, and $n_{td}$ represent the tap value of the ULTC that is not connected to a DC converter, the total number of ULTCs that are not connected to DC converters, the tap value of the DC converter's ULTC, and the total number of DC converters' ULTCs, respectively.

### 2.2. The illustration of the sequential DC power flow algorithm

This section presents the proposed sequential DC power flow algorithm. HVDC links are separated to DC subsystems. DC subsystems are composed of the DC lines that are connected to each other. DC converters are considered as line commutating converters (LCC) that are multipulse thyristor-controlled rectifiers. LCCs can be operated in both rectifier and inverter mode by controlling the thyristor gate control angles [22]. The proposed power model for a multiterminal DC subsystem is given in Figure 3.

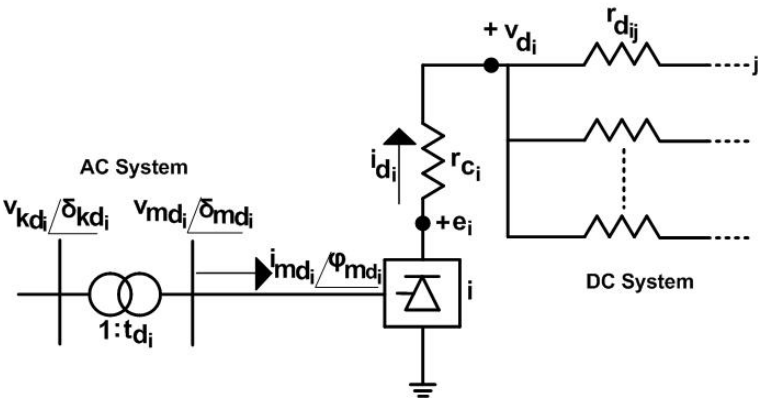


**Figure 3.** Proposed multiterminal DC subsystem power model.

$e_i$, $v_{d_i}$, $i_{d_i}$, $r_{c_i}$, $r_{d_{ij}}$, $t_{d_i}$, $v_{kd_i}$, $v_{md_i}$, $i_{md_i}$, $\delta_{kd_i}$, $\delta_{md_i}$, and $\phi_{md_i}$ represent the $i$th DC converter's open-circuit direct voltage, the $i$th DC converter's terminal direct voltage, the $i$th DC converter's direct current, the $i$th DC converter's commutation resistance, the DC line resistance between the $i$th and $j$th DC converters, the $i$th DC converter's ULTC tap value, the $i$th DC converter's ULTC primary alternative voltage, the $i$th DC converter's ULTC secondary alternative voltage, the alternative current flowing from the DC converter's ULTC secondary to the DC converter, the phase angle of the $i$th DC converter's ULTC primary alternative voltage, the phase angle of the $i$th DC converter's ULTC secondary alternative voltage, and the phase angle of the alternative current flowing from the $i$th DC converter's ULTC secondary to the DC converter, respectively.

The following equations and the sequential DC power flow algorithm are defined for the individual independent multiterminal DC subsystems demonstrated in Figure 3.

The DC converters' open-circuit direct voltages are defined as

$$e_i = v_{md_i} \cos\theta_i \quad (i = 1, \ldots, n_c) \tag{12}$$

where $n_c$ represents the total number of DC converters in the subsystem and $\theta_i$ is the thyristor gate control angle of the LCC-based DC converter, which defines $\alpha_{d_i}$ and $\gamma_{d_i}$ as the firing angle of the $i$th DC converter that operates in rectifier mode and the extinction/recovery angle of the $i$th DC converter that operates in inverter mode, respectively.

The DC converters' terminal direct voltages are defined as

$$v_{d_i} = e_i - r_{c_i} i_{d_i} \quad (i = 1, \ldots, n_c) \tag{13}$$

In Eq. (13), commutation resistance $r_{c_i}$ is positive for a DC converter that operates in rectifier mode and negative for a DC converter that operates in inverter mode.

Phase angle between the DC converter's ULTC secondary alternative voltage angle and the angle of the alternative current flowing from the DC converter's ULTC secondary to DC converter is defined as

$$\varphi_{md_i} = \delta_{md_i} - \phi_{md_i} \quad (i = 1, \ldots, n_c) \tag{14}$$

and can also be derived from

$$\varphi_{md_i} = \arccos\left(\frac{v_{d_i}}{v_{md_i}}\right) \quad (i = 1, \ldots, n_c) \tag{15}$$

The active and reactive powers of the DC converters can be given as

$$p_{d_i} = v_{d_i} i_{d_i} \quad (i = 1, \ldots, n_c) \tag{16}$$

$$q_{d_i} = |p_{d_i} \tan \varphi_{md_i}| \quad (i = 1, \ldots, n_c) \tag{17}$$

The multiterminal DC subsystem model is given in Figure 4.

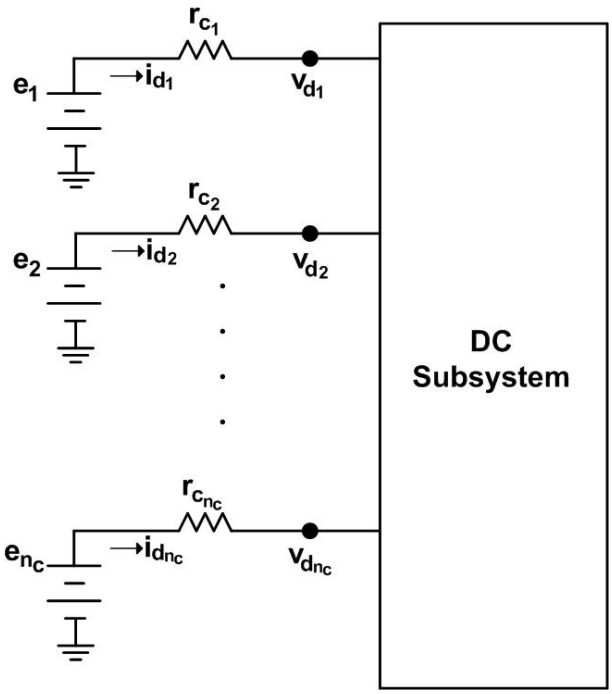


**Figure 4.** Multiterminal DC subsystem model.

In this model, commutation resistances are not included in the DC bus resistance matrix to avoid rebuilding the DC bus resistance matrix in each DC algorithm iteration. Otherwise, the DC bus resistance matrix is rebuilt in each algorithm iteration because the commutation resistance values change their sign in

each iteration when the converters are updated from rectifier mode to inverter mode, or vice versa. If the DC terminal direct voltages are considered source voltages, commutation resistances can be ignored in the DC bus resistance matrix. When considering the 1st DC converter a reference converter, the DC bus resistance matrix is derived as

$$r_{d_{bus}} = y_{d_{bus}}^{-1} = \begin{bmatrix} \left(\frac{1}{r_{d_{21}}} + \frac{1}{r_{d_{23}}} + \ldots + \frac{1}{r_{d_{2n_c}}}\right) & \left(-\frac{1}{r_{d_{23}}}\right) & . & \left(-\frac{1}{r_{d_{2n_c}}}\right) \\ \left(-\frac{1}{r_{d_{32}}}\right) & \left(\frac{1}{r_{d_{31}}} + \frac{1}{r_{d_{32}}} + \ldots + \frac{1}{r_{d_{3n_c}}}\right) & . & \left(-\frac{1}{r_{d_{3n_c}}}\right) \\ . & . & . & . \\ \left(-\frac{1}{r_{d_{n_c1}}}\right) & \left(-\frac{1}{r_{d_{n_c2}}}\right) & . & \left(\frac{1}{r_{d_{n_c1}}} + \frac{1}{r_{d_{n_c2}}} + \ldots + \frac{1}{r_{d_{n_cn_{c-1}}}}\right) \end{bmatrix}^{-1}, \tag{18}$$

where $y_{d_{bus}}$ indicates the DC bus admittance matrix that includes only the admittances of DC lines.

If the 1st DC converter's terminal direct voltage is considered the reference voltage, the DC converters' open-circuit direct voltages can be defined as

$$e_1 = v_{d_1} + r_{c_1} i_{d_1} \tag{19}$$

$$e_i = e_1 - r_{c_1} i_{d_1} + r_{c_i} i_{d_i} + \sum_{j=2}^{n_c} r_{dbus_{ij}} i_{d_j} \qquad (i = 2, ..., n_c) \tag{20}$$

According to the DC model given in Figure 4, in each DC subsystem the algebraic sum of the DC converters direct currents must be zero:

$$\sum_{i=1}^{n_c} i_{d_i} = 0 \tag{21}$$

The sequential DC power flow algorithm is performed by linear current-balancing method according to Eq. (21), considering the proposed multiterminal DC system equations given before. The sequential DC power flow algorithm can be given step-by-step for each DC subsystem, as below:

Step 1. Estimate the DC converters' terminal direct voltages as their nominal values.

$$v_{d_i}^{'} = v_{d_i}^{nom} \qquad (i = 1, ..., n_c) \tag{22}$$

Step 2. Estimate the DC converters' direct currents using the active powers of the DC converters obtained from the sequential AC power flow algorithm and the estimated DC converters' terminal direct voltages in step 1.

$$i_{d_i}^{'} = \frac{p_{d_i}}{v_{d_i}^{'}} \qquad (i = 1, ..., n_c) \tag{23}$$

Step 3. Calculate the real values of the DC converters' direct currents using the estimated values in step 2.

$$i_{di} = i_{di}^{'} - \frac{\left(\sum_{j=1}^{n_c} \frac{1}{\sigma_i}\right)^{-1} \cdot \sum_{j=1}^{n_c} i_{dj}^{'}}{\sigma_i} \qquad (i = 1, ..., n_c), \tag{24}$$

where $\sigma_i$ indicates the $i$th DC converter's weight coefficient selected according the system operation procedures and converter power rating. Eq. (24) defines the current balancing of the DC converters' direct currents

according to Eq. (21). Eq. (21) indicates the Kirchhoff current law (KCL) for the proposed DC subsystem model given in Figure 4. The estimated DC converters' direct currents derived by Eq. (23) in step 2 cannot provide the required equality given in Eq. (21). Thus, Eq. (24) balances these estimated currents to provide the KCL of Eq. (21) depending on the rates of the DC converters' active powers obtained from the AC power flow algorithm.

Step 4. Determine the commutation resistance with their signs using the real values of the DC converters' direct currents obtained in step 3.

$$r_{c_i} = \frac{|r_{c_i} i_{d_i}|}{i_{d_i}} \tag{25}$$

Step 5. Determine the open circuit direct voltages of the DC converters.

$$e_1 = v_{d_1} + r_{c_1} i_{d_1} \tag{26}$$

$$e_i = e_1 - r_{c_1} i_{d_1} + r_{c_i} i_{d_i} + \sum_{j=2}^{n_c} r_{dbus_{ij}} i_{d_j} \qquad (i = 2, ..., n_c) \tag{27}$$

Step 6. Determine the terminal direct voltages of the DC converters other than the 1st DC converter.

$$v_{d_i} = e_i - r_{c_i} i_{d_i} \qquad (i = 2, ..., n_c) \tag{28}$$

Step 7. Update the open-circuit direct voltages of the DC converters as

$$e_i = \begin{cases} e_i - e^{\min}_{difference}, e_p > v^{nom}_{d_i} \\ e_i + e^{\min}_{difference}, e_p < v^{nom}_{d_i} \end{cases} \qquad (i = 1, ..., n_c), \tag{29}$$

where $e^{\min}_{difference}$ indicates the minimum component of the vector given below:

$$[e_{difference}] = \left[ \left| e_1 - v^{nom}_{d_1} \right|, \left| e_2 - v^{nom}_{d_2} \right|, ....., \left| e_{n_c} - v^{nom}_{d_{n_c}} \right| \right] \tag{30}$$

and $p$ indicates the subscript where $e^{\min}_{difference}$ is the $p$th component of vector $e_{difference}$.

Step 8. Update the terminal direct voltages of the DC converters using the updated open-circuit direct voltages of the DC converters in step 7.

$$v_{d_i} = e_i - r_{c_i} i_{d_i} \qquad (i = 1, ..., n_c) \tag{31}$$

Step 9. Compare the terminal direct voltages of the DC converters used in step 1 and obtained in step 8.

$$v_{d_i} - v^{'}_{d_i} \leq \varepsilon_{DA} \qquad (i = 1, ..., n_c), \tag{32}$$

where $\varepsilon_{DA}$ indicates the error tolerance selected for the sequential DC power flow algorithm. If the inequality given in Eq. (32) is provided, go to step 10, else go to step 2 with the terminal direct voltages of the DC converters obtained in step 8 and use them as estimated terminal direct voltages.

Step 10. Determine the firing or extinction/recovery angles for the DC converters.

$$\theta_i = \arccos\left(\frac{e_i}{v_{md_i}}\right) \qquad (i = 1, ..., n_c) \tag{33}$$

Step 11. Update the tap values of the DC converters' ULTCs according to the firing or extinction/recovery angles for the DC converters obtained in step 10.

$$t_{d_i} = \begin{cases} t_{d_i} + t_{d_i}^{gear}, Im\left(\left|\arccos\left(\theta_i\right)\right|\right) > 0 \ \ \& \ \ t_{d_i} \neq t_{d_i}^{\max} \\ t_{d_i} + t_{d_i}^{gear}, Im\left(\left|\arccos\left(\theta_i\right)\right|\right) = 0 \ \ \& \ \ p_{d_i} > 0 \ \ \& \ \ \theta_i < \alpha_i^{\min} \ \ \& \ \ t_{d_i} \neq t_{d_i}^{\max} \\ t_{d_i} + t_{d_i}^{gear}, Im\left(\left|\arccos\left(\theta_i\right)\right|\right) = 0 \ \ \& \ \ p_{d_i} < 0 \ \ \& \ \ \theta_i < \gamma_i^{\min} \ \ \& \ \ t_{d_i} \neq t_{d_i}^{\max} \end{cases} \qquad (i = 1, ..., n_c), \tag{34}$$

where $t_{d_i}^{gear}$, $t_{d_i}^{\max}$, $\alpha_i^{\min}$, and $\gamma_i^{\min}$ represent the tap variation of the $i$th DC converter's ULTC for one gear change, the maximum tap value of the $i$th DC converter's ULTC, the minimum firing angle of the $i$th DC converter for rectifier mode, and the minimum extinction/recovery angle of the $i$th DC converter for inverter mode, respectively. As seen in Figure 3, the tap value of DC converter's ULTC determines the input AC voltage amplitude $(v_{md_i})$. It is clear from Eq. (12) that if $v_{md_i}$ is not high enough, $\theta_i$ is forced into imaginary or under-limit values. To avoid obtaining imaginary or under-limit values, $v_{md_i}$ must be increased by increasing the DC converter's ULTC tap value $(t_{d_i})$.

Step 12. Update the firing or extinction/recovery angles for the DC converters.

$$\theta_i = \begin{cases} \alpha_i^{\min}, Im\left(\left|\arccos\left(\theta_i\right)\right|\right) > 0 \ \ \& \ \ p_{d_i} > 0 \\ \gamma_i^{\min}, Im\left(\left|\arccos\left(\theta_i\right)\right|\right) > 0 \ \ \& \ \ p_{d_i} < 0 \end{cases} \qquad (i = 1, ..., n_c) \tag{35}$$

Step 13. Update the active and reactive powers of the DC converters.

$$p_{d_i} = v_{d_i} i_{d_i} \qquad (i = 1, ..., n_c) \tag{36}$$

$$\varphi_{md_i} = \arccos\left(\frac{v_{d_i}}{v_{md_i}}\right) \qquad (i = 1, ..., n_c) \tag{37}$$

$$q_{d_i} = \left|p_{d_i} \tan \varphi_{md_i}\right| \qquad (i = 1, ..., n_c) \tag{38}$$

Step 14. The sequential DC power flow algorithm is accomplished.

Eq. (35) increases the DC converters' ULTC tap values when only the control angles are forced to be imaginary. As will be given in Section 2.3, the proposed AC/DC power flow algorithm starts considering the initials of the DC converters' ULTC tap values to be in their minimum values. On the other hand, in each DC power flow algorithm iteration, the active and reactive power values of DC converters are updated by Eqs. (36) and (37). Thus, the exceeding problem of the maximum values of the DC converters' ULTC tap values is prevented. Hence, the proposed AC/DC power flow algorithm can find a suitable solution between the minimum and maximum values of the DC converters' ULTC tap values.

### 2.3. The illustration of the proposed sequential AC/DC power flow algorithm

In this section, the proposed sequential AC/DC power flow algorithm is given through the sequential AC and DC power flow algorithms given in Sections 2.1 and 2.2. The proposed sequential DC power flow algorithm is performed separately for each DC subsystem. The proposed AC/DC power flow algorithm is given in detail in Figure 5.

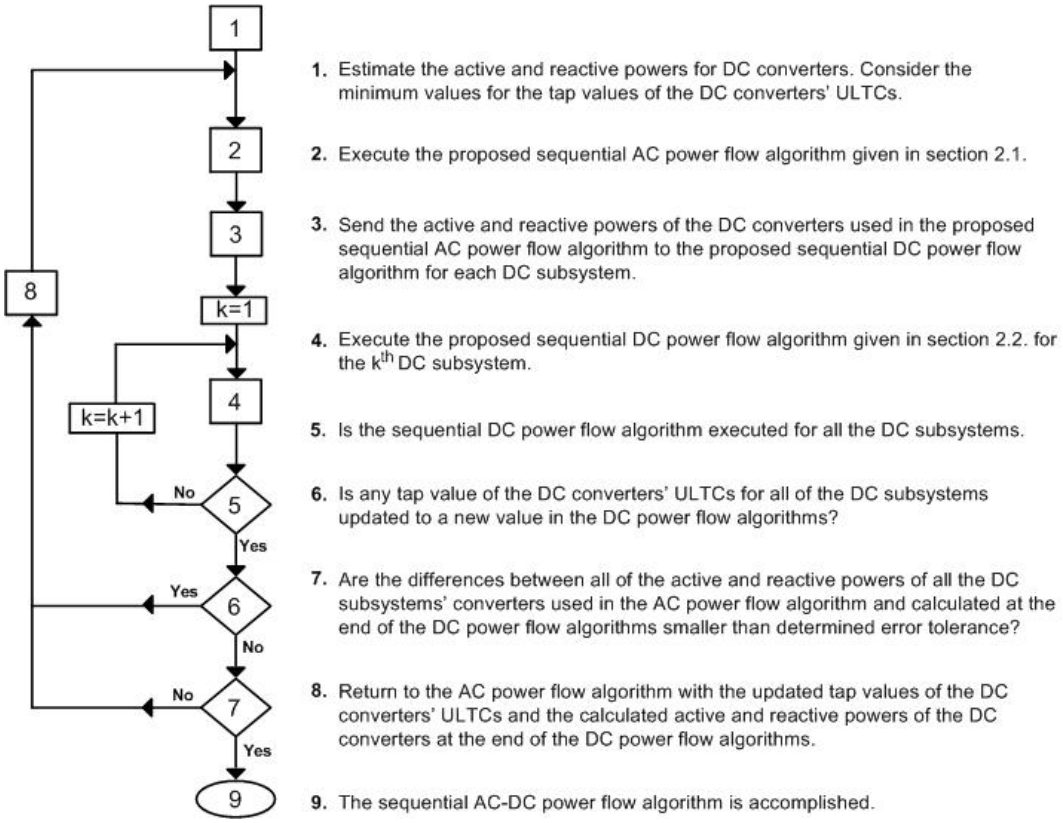


**Figure 5.** Proposed AC/DC power flow algorithm.

## 3. Results

The proposed AC/DC power flow algorithm is tested on the modified IEEE 20-bus AC/DC test system given in Figure 6 to prove the proposed approach's accuracy and efficiency. All of the results given in this section were obtained using MATLAB.

The modified IEEE 20-bus AC-DC test system is the remodified form of the modified IEEE 14-bus AC/DC test system used in [23,24] (Figure 6). The modified IEEE 14-bus AC/DC test system includes only one multiterminal DC system in its original form. To test the proposed approach for the AC/DC systems, including the independent DC subsystems, one more DC subsystem is included in the modified IEEE 14-bus AC/DC test system between buses 10, 11, and 14. As the real equivalent circuit model of the DC converters' ULTCs are considered in the proposed study, the total bus number is increased for each converter (Figure 6). To compare the results of the proposed approach with the approaches that ignore the real equivalent circuit model of the DC converters' ULTCs, the approaches in [23,24] are modified for AC/DC power flow of the test system in Figure 6. It is clear that the total bus number is again 14 for the remodified IEEE 14-bus AC/DC test system in the remodified studies of [23,24], as the real equivalent circuit models of the DC converters' ULTCs are ignored in those modified studies. It must be noted that comparisons of the results between the proposed approach and the mentioned approaches is only done to show the results of considering the real equivalent circuit of DC converters' ULTCs. It is clear that a healthy comparison for the efficiency and fastness of the power flow algorithms cannot be done because the studied system will always be different in the algorithms due to the aforementioned considerations of the real equivalent circuit of DC converters' ULTCs. The DC data

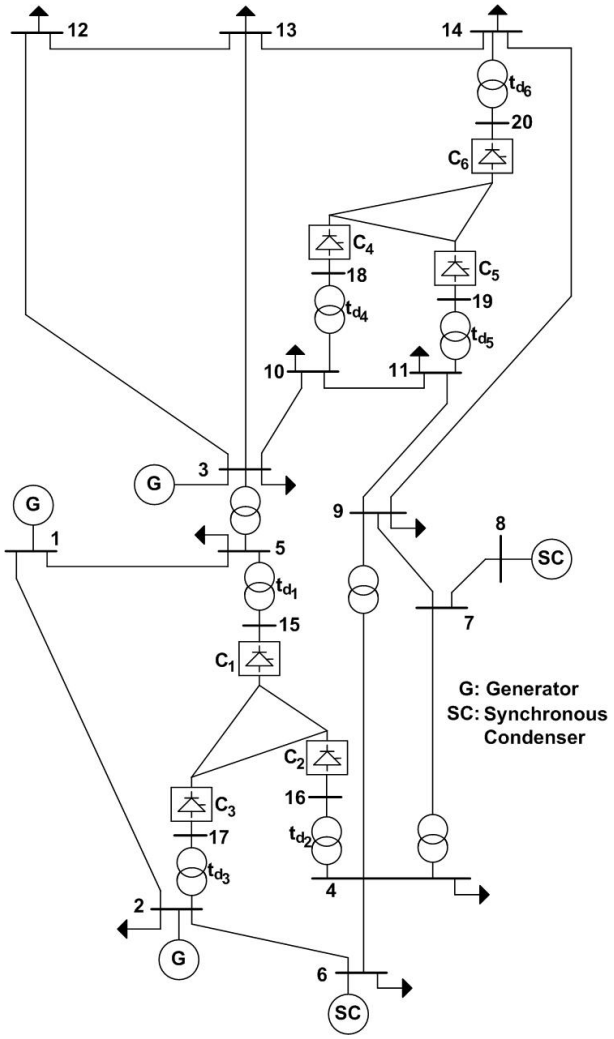


**Figure 6.** The modified IEEE 20-bus AC/DC test system.

of the test system are given in Tables 1–3. The DC converters are connected to buses 5, 4, 2, 10, 11, and 14 instead of the buses 15, 16, 17, 18, 19, and 20, respectively, in [23,24] (Table 3).

The results of applying the proposed AC/DC power flow algorithm to the test system is given and compared with the results of [23,24], which ignore the real equivalent circuits of the DC converters' ULTCs (Table 4).

As explained previously, results are undefined for the buses 15, 16, 17, 18, 19, and 20 in the compared studies because of ignoring the DC converters' ULTCs in the compared studies (Table 4). As seen in Table 4, all of the tap values of the DC converters' ULTCs are obtained as real discrete values for the given ULTCs' parameters in the proposed approach. However, the tap values obtained for some of the DC converters are far from the real discrete values of the ULTCs in the compared studies. In practical applications, these values must be rounded to the nearest discrete values for the compared studies. In this situation, the obtained firing or extinction/recovery angles of the compared studies cannot meet the power equations. On the other hand, the obtained firing angles for the compared studies cannot provide power balance, even if the tap values of

**Table 1.** Commutation resistance data and ULTC parameters of the DC system.

| DC subsystem | Terminal | $r_c$ (p.u.)$\mathrm{r_c}$ | ULTC parameters | | | |
|---|---|---|---|---|---|---|
| | | | $t_d^{\min}$ | $t_d^{\max}$ | $t_d^{gear}$ | Serial reactance × (p.u.) |
| 1 | Converter 1 ($C_1$) | 0.025680 | 0.9 | 1.1 | 0.05 | 0.20912 |
| | Converter 2 ($C_2$) | 0.028246 | 0.9 | 1.1 | 0.05 | 0.20912 |
| | Converter 3 ($C_3$) | 0.015329 | 0.9 | 1.1 | 0.05 | 0.20912 |
| 2 | Converter 4 ($C_4$) | 0.023711 | 0.9 | 1.1 | 0.05 | 0.11001 |
| | Converter 5 ($C_5$) | 0.024137 | 0.9 | 1.1 | 0.05 | 0.11001 |
| | Converter 6 ($C_6$) | 0.022456 | 0.9 | 1.1 | 0.05 | 0.11001 |

**Table 2.** Firing and extinction/recovery angle parameters of the DC system.

| Terminal | Firing or extinction/recovery angles (degrees) | |
|---|---|---|
| | $\alpha_i^{\min}$ | $\gamma_i^{\min}$ |
| Converter 1 ($C_1$) | 6.00 | 16.26 |
| Converter 2 ($C_2$) | 6.00 | 16.26 |
| Converter 3 ($C_3$) | 6.00 | 16.26 |
| Converter 4 ($C_4$) | 6.00 | 16.26 |
| Converter 5 ($C_5$) | 6.00 | 16.26 |
| Converter 6 ($C_6$) | 6.00 | 16.26 |

**Table 3.** Line resistance data of the DC system.

| Line resistance | | $r_d$ (p.u.) |
|---|---|---|
| From bus | To bus | |
| 15 (5, for [23,24]) | 16 (4, for [23,24]) | 0.0134 |
| 15 (5, for [23,24]) | 17 (2, for [23,24]) | 0.0570 |
| 16 (4, for [23,24]) | 17 (2, for [23,24]) | 0.0581 |
| 18 (10, for [23,24]) | 19 (11, for [23,24]) | 0.0242 |
| 18 (10, for [23,24]) | 20 (14, for [23,24]) | 0.0458 |
| 19 (11, for [23,24]) | 20(14, for [23,24]) | 0.0317 |

the ULTCs are obtained in real discrete values, because the serial and shunt admittances depending on the tap values of the DC converters' ULTCs are ignored in these studies. This neglect is impossible in practical applications, as proven by the differences between all the variables' results for the proposed approach and the compared algorithms. Thus, the results in Table 4 show that the proposed AC/DC power flow approach given in this paper provides an exact, accurate, and reliable solution for a power flow solution in power systems including HVDC systems.

The convergence results in iteration number and time are given in Table 5 for the proposed AC/DC power flow algorithm and compared studies.

The proposed approach has converged in more iteration numbers and in greater convergence time according the compared studies (Table 5). However, it must be noted that the compared studies neglect

**Table 4.** Comparative results of the proposed approach and similar studies.

| Variable | Result (p.u./deg.) | | | Variable | Result (p.u./deg.) | | | Variable | Result (p.u./deg.) | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | Proposed approach | [23] | [24] | | Proposed approach | [23] | [24] | | Proposed approach | [23] | [24] |
| $v_1^*$ | 1.0200 | 1.0200 | 1.0200 | $\delta_1$ | 0 | 0 | 0 | $q_{d_3}$ | 0.0735 | 0.0753 | 0.0789 |
| $v_2^*$ | 1.0700 | 1.0700 | 1.0700 | $\delta_2$ | 0.663 | 0.773 | 0.782 | $\varphi_{md_1}$ | 16.3441 | - | - |
| $v_3^*$ | 1.0850 | 1.0850 | 1.0850 | $\delta_3$ | –19.27 | –17.94 | –17.68 | $\varphi_{md_2}$ | 19.0742 | - | - |
| $v_4$ | 0.9740 | 1.0534 | 1.0535 | $\delta_4$ | –2.576 | –3.523 | –3.670 | $\varphi_{md_3}$ | 20.4645 | - | - |
| $v_5$ | 0.9750 | 1.0038 | 1.0056 | $\delta_5$ | –39.36 | –37.44 | –37.00 | $\theta_{d_1}$ | 13.5898 | 6.0000 | 6.0000 |
| $v_6^*$ | 1.0349 | 1.0349 | 1.0349 | $\delta_6$ | –3.030 | –2.577 | –2.647 | $\theta_{d_2}$ | 17.5903 | 16.2600 | 16.2600 |
| $v_7$ | 0.9981 | 1.0324 | 1.0321 | $\delta_7$ | –5.524 | –5.972 | –6.029 | $\theta_{d_3}$ | 19.9847 | 20.4487 | 20.3779 |
| $v_8^*$ | 0.9981 | 0.9981 | 0.9981 | $\delta_8$ | –5.524 | –5.972 | –6.029 | $t_{d_1}$ $(t_{5-15})$ | 1.10 | 1.0221 | 1.0205 |
| $v_9$ | 1.0118 | 1.0436 | 1.0429 | $\delta_9$ | –7.017 | –7.272 | –7.283 | $t_{d_2}$ $(t_{4-16})$ | 1.10 | 1.00 | 1.0000 |
| $v_{10}$ | 0.9917 | 1.0280 | 1.0266 | $\delta_{10}$ | –10.37 | –10.42 | –10.43 | $t_{d_3}$ $(t_{2-17})$ | 1.00 | 1.00 | 1.0000 |
| $v_{11}$ | 1.0304 | 1.0542 | 1.0537 | $\delta_{11}$ | –13.68 | –13.14 | –12.95 | $v_{d_4}$ | 1.0002 | 1.0123 | 1.0117 |
| $v_{12}$ | 1.0611 | 1.0649 | 1.0649 | $\delta_{12}$ | –19.08 | –17.82 | –17.56 | $v_{d_5}$ | 0.9943 | 1.0065 | 1.0056 |
| $v_{13}$ | 1.0553 | 1.0621 | 1.0622 | $\delta_{13}$ | –17.93 | –16.83 | –16.58 | $v_{d_6}$ | 0.9930 | 1.0052 | 1.0043 |
| $v_{14}$ | 1.0079 | 1.0360 | 1.0360 | $\delta_{14}$ | –10.86 | –10.65 | –10.46 | $i_{d_4}$ | 0.3999 | 0.3952 | 0.4151 |
| $v_{15}$ | 1.0382 | - | - | $\delta_{15}$ | –44.75 | - | - | $i_{d_5}$ | –0.2011 | –0.1987 | –0.2088 |
| $v_{16}$ | 1.0491 | - | - | $\delta_{16}$ | 0.623 | - | - | $i_{d_6}$ | –0.1988 | –0.1964 | –0.2063 |
| $v_{17}$ | 1.0547 | - | - | $\delta_{17}$ | 2.754 | - | - | $p_{d_4}$ | 0.4000 | 0.4000 | 0.4200 |
| $v_{18}$ | 1.0741 | - | - | $\delta_{18}$ | –12.52 | - | - | $p_{d_5}$ | –0.2000 | –0.2000 | –0.2100 |
| $v_{19}$ | 1.1230 | - | - | $\delta_{19}$ | –12.69 | - | - | $p_{d_6}$ | –0.1974 | –0.1975 | –0.2072 |
| $v_{20}$ | 1.0992 | - | - | $\delta_{20}$ | –9.845 | - | - | $q_{d_4}$ | 0.1565 | 0.0709 | 0.0757 |
| $t_{3-5}^*$ | 1.00 | 1.00 | 1.00 | $v_{d_1}$ | 0.9963 | 1.0076 | 1.0081 | $q_{d_5}$ | 0.1050 | 0.0624 | 0.0657 |
| $t_{4-7}^*$ | 1.00 | 1.00 | 1.00 | $v_{d_2}$ | 0.9915 | 1.0028 | 1.0035 | $q_{d_6}$ | 0.0937 | 0.0598 | 0.0628 |
| $t_{4-9}^*$ | 1.00 | 1.00 | 1.00 | $v_{d_3}$ | 0.9882 | 0.9996 | 0.9999 | $\varphi_{md_4}$ | 21.3721 | - | - |
| $p_{g1}$ | 0.1031 | 0.0754 | 0.0741 | $i_{d_1}$ | 0.5019 | 0.4962 | 0.4861 | $\varphi_{md_5}$ | 27.6969 | - | - |
| $p_{g2}^*$ | 0.6500 | 0.6500 | 0.6500 | $i_{d_2}$ | –0.3026 | –0.299 | –0.279 | $\varphi_{md_6}$ | 25.3907 | - | - |
| $p_{g3}^*$ | 1.2000 | 1.2000 | 1.2000 | $i_{d_3}$ | –0.199 | –0.197 | –0.207 | $\theta_{d_4}$ | 19.8144 | 6.0000 | 6.0000 |
| $q_{g1}$ | –1.3060 | –1.438 | –1.433 | $p_{d_1}$ | 0.500 | 0.5000 | 0.4900 | $\theta_{d_5}$ | 27.0667 | 16.2600 | 16.2600 |
| $q_{g2}$ | 0.3929 | 0.3819 | 0.3834 | $p_{d_2}$ | –0.300 | –0.300 | –0.280 | $\theta_{d_6}$ | 25.0179 | 16.2600 | 16.2600 |
| $q_{g3}$ | 1.6506 | 1.3086 | 1.2941 | $p_{d_3}$ | –0.196 | –0.197 | –0.207 | $t_{d_4}$ $(t_{10-18})$ | 1.10 | 1.00 | 1.0014 |
| $q_{sc6}$ | –0.5251 | –0.477 | –0.478 | $q_{d_1}$ | 0.1466 | 0.0959 | 0.0933 | $t_{d_5}$ $(t_{11-19})$ | 1.10 | 1.00 | 1.0000 |
| $q_{sc8}$ | 0.0292 | –0.194 | –0.192 | $q_{d_2}$ | 0.1037 | 0.0965 | 0.0895 | $t_{d_6}$ $(t_{14-20})$ | 1.10 | 1.0137 | 1.0130 |

*indicates the control variables

**Table 5.** Convergence results of the proposed approach and similar studies.

| Convergence results | Proposed approach | [23] | [24] |
|---|---|---|---|
| Iteration number | 6ac3dc(1)3dc(2)5ac 3dc(1)3dc(2)5ac3dc(1) 3dc(2)4ac3dc(1)3dc(2) 3ac3dc(1)3dc(2)3ac 3dc(1)3dc(2)3ac3dc(1) 3dc(2)2ac3dc(1)3dc(2) 2ac3dc(1)3dc(2)2ac 3dc(1)3dc(2)2ac3dc(1) 3dc(2)2ac3dc(1)3dc(2) 2ac3dc(1)3dc(2)2ac 3dc(1)3dc(2)2ac3dc(1) 3dc(2) | 5ac4dc(1)3dc(2)5ac 3dc(1)3dc(2)2ac3dc(1) 4dc(2)2ac3dc(1)4dc(2) | 5ac4dc(1)3dc(2)5ac 3dc(1)3dc(2)2ac3dc(1) 3dc(2)2ac3dc(1)3dc(2) |
| Time (sec.) | 0.8675 | 0.3795 | 0.3718 |
| (ac: sequential AC power flow algorithm iteration, dc(1): sequential DC power flow algorithm iteration for DC subsystem 1, dc(2): sequential DC power flow algorithm iteration for DC subsystem 2) | | | |

the real equivalent circuit models of the DC converters' ULTCS. Nevertheless, the accuracy and reliability of the proposed approach in practical applications are more effective and important than the convergence time.

The proposed AC/DC power flow algorithm is applied to the same test system for different AC operating points to show the proposed approach's efficiency and accuracy. The results for different cases are given in Table 6. The results demonstrate that the proposed approach is capable of solving system AC/DC power flow in a robust manner for different system conditions.

**Table 6.** The results of the proposed approach for different cases.

| Variable | Case 1 | Case 2 | Case 3 | Variable | Case 1 | Case 2 | Case 3 | Variable | Case 1 | Case 2 | Case 3 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $v_1^*$ | 1.080 | 1.0510 | 1.030 | $\delta_1$ | 0 | 0 | 0 | $q_{d_3}$ | 0.0660 | 0.1512 | 0.1487 |
| $v_2^*$ | 1.060 | 1.0420 | 1.070 | $\delta_2$ | 1.763 | 1.574 | –0.297 | $\varphi_{md_1}$ | 15.4102 | 23.2140 | 14.8343 |
| $v_3^*$ | 1.045 | 1.0640 | 1.020 | $\delta_3$ | –11.633 | –3.667 | –37.95 | $\varphi_{md_2}$ | 20.7575 | 16.7241 | 11.6894 |
| $v_4$ | 1.074 | 1.0982 | 1.030 | $\delta_4$ | –3.638 | –8.817 | –13.94 | $\varphi_{md_3}$ | 18.3941 | 20.5647 | 18.5094 |
| $v_5$ | 1.005 | 1.0100 | 1.040 | $\delta_5$ | –27.354 | –13.79 | –53.41 | $\theta_{d_1}$ | 13.7163 | 22.4165 | 14.8343 |
| $v_6^*$ | 1.086 | 1.0910 | 1.0659 | $\delta_6$ | –2.837 | –5.678 | –9.230 | $\theta_{d_2}$ | 20.3238 | 12.9069 | 11.6894 |
| $v_7$ | 1.111 | 1.0612 | 1.0749 | $\delta_7$ | –4.884 | –6.604 | –15.58 | $\theta_{d_3}$ | 17.8550 | 19.5876 | 18.5094 |
| $v_8^*$ | 1.111 | 1.0612 | 1.0749 | $\delta_8$ | –4.884 | –6.604 | –15.58 | $t_{d_1}$ $(t_{5-15})$ | 1.05 | 1.10 | 1.00 |
| $v_9$ | 1.102 | 1.0423 | 1.0448 | $\delta_9$ | –5.554 | –5.378 | –16.52 | $t_{d_2}$ $(t_{4-16})$ | 1.00 | 1.00 | 1.00 |
| $v_{10}$ | 1.085 | 1.0253 | 1.0243 | $\delta_{10}$ | –6.172 | –6.384 | –20.36 | $t_{d_3}$ $(t_{2-17})$ | 1.00 | 1.05 | 1.00 |
| $v_{11}$ | 1.063 | 1.0319 | 1.0113 | $\delta_{11}$ | –8.068 | –5.705 | –28.09 | $v_{d_4}$ | 0.9976 | 0.9997 | 0.9983 |
| $v_{12}$ | 1.029 | 1.0478 | 0.9982 | $\delta_{12}$ | –12.236 | –4.178 | –37.44 | $v_{d_5}$ | 0.9976 | 0.9980 | 0.9964 |
| $v_{13}$ | 1.027 | 1.0442 | 0.9977 | $\delta_{13}$ | –12.031 | –3.877 | –35.95 | $v_{d_6}$ | 1.0023 | 0.9919 | 0.9987 |
| $v_{14}$ | 1.017 | 1.0268 | 0.9829 | $\delta_{14}$ | –10.939 | –2.237 | –26.47 | $i_{d_4}$ | –0.1002 | 0.2401 | 0.0701 |
| $v_{15}$ | 1.036 | 1.0912 | 1.0297 | $\delta_{15}$ | –30.641 | –11.51 | –55.42 | $i_{d_5}$ | –0.1504 | 0.1202 | –0.1505 |
| $v_{16}$ | 1.066 | 1.0526 | 1.0170 | $\delta_{16}$ | –2.592 | –15.46 | –17.03 | $i_{d_6}$ | 0.2506 | –0.3603 | 0.0804 |
| $v_{17}$ | 1.046 | 1.0614 | 1.0362 | $\delta_{17}$ | 3.907 | 5.735 | 4.507 | $p_{d_4}$ | –0.1000 | 0.2400 | 0.0700 |
| $v_{18}$ | 1.081 | 1.0197 | 1.0226 | $\delta_{18}$ | –5.636 | –7.831 | –20.78 | $p_{d_5}$ | –0.1500 | 0.1200 | –0.1500 |
| $v_{19}$ | 1.058 | 1.0286 | 1.0563 | $\delta_{19}$ | –7.228 | –6.418 | –27.25 | $p_{d_6}$ | 0.2512 | –0.3574 | 0.0803 |
| $v_{20}$ | 1.059 | 1.0632 | 1.0299 | $\delta_{20}$ | –12.338 | –0.272 | –26.94 | $q_{d_4}$ | 0.0419 | 0.0483 | 0.0155 |
| $t_{3-5}^*$ | 1.00 | 0.95 | 1.00 | $v_{d_1}$ | 0.9996 | 1.0029 | 0.9954 | $q_{d_5}$ | 0.0531 | 0.0300 | 0.0528 |
| $t_{4-7}^*$ | 1.05 | 1.00 | 1.10 | $v_{d_2}$ | 0.9972 | 1.0081 | 0.9959 | $q_{d_6}$ | 0.0858 | 0.1380 | 0.0202 |
| $t_{4-9}^*$ | 1.10 | 0.90 | 1.00 | $v_{d_3}$ | 0.9926 | 0.9938 | 0.9826 | $\varphi_{md_4}$ | 22.7237 | 11.3827 | 12.5139 |
| $p_{g1}$ | 0.0419 | 0.0394 | 1.2074 | $i_{d_1}$ | 0.3001 | –0.229 | 0.1808 | $\varphi_{md_5}$ | 19.4780 | 14.0233 | 19.3779 |
| $p_{g2}^*$ | 0.6500 | 0.6500 | 0.5500 | $i_{d_2}$ | –0.1003 | 0.6349 | 0.2711 | $\varphi_{md_6}$ | 18.8546 | 21.1063 | 14.1295 |
| $p_{g3}^*$ | 1.2000 | 1.200 | 0.4200 | $i_{d_3}$ | –0.1999 | –0.405 | –0.452 | $\theta_{d_4}$ | 22.3955 | 9.6284 | 12.0765 |
| $q_{g1}$ | –0.279 | –0.308 | –1.388 | $p_{d_1}$ | 0.3000 | –0.230 | 0.1800 | $\theta_{d_5}$ | 18.8798 | 13.3397 | 18.7749 |
| $q_{g2}$ | –1.1809 | –0.989 | 0.2068 | $p_{d_2}$ | –0.1000 | 0.6400 | 0.2700 | $\theta_{d_6}$ | 17.8887 | 19.8603 | 13.7118 |
| $q_{g3}$ | 0.1829 | 0.801 | 0.9268 | $p_{d_3}$ | –0.1984 | –0.403 | –0.444 | $t_{d_4}$ $(t_{10-18})$ | 1.00 | 1.00 | 1.00 |
| $q_{sc6}$ | 0.0660 | 0.353 | 0.1900 | $q_{d_1}$ | 0.0827 | 0.0986 | 0.0477 | $t_{d_5}$ $(t_{11-19})$ | 1.00 | 1.00 | 1.05 |
| $q_{sc8}$ | 0.5384 | –0.225 | 0.2893 | $q_{d_2}$ | 0.0379 | 0.1923 | 0.0559 | $t_{d_6}$ $(t_{14-20})$ | 1.05 | 1.05 | 1.05 |

*indicates the control variables

## 4. Conclusion

This paper presents a novel power flow solution based on sequential algorithms for AC/DC systems that include independent multiterminal DC subsystems. Real equivalent circuits of DC converters' ULTCs are considered in this study for the first time in the literature. For this aim, a novel DC power flow model is developed. Tap-changing and admittance effects of the DC converters' ULTCs are included in the sequential AC power flow algorithm. To avoid the rebuilding of the AC bus admittance matrix caused by the tap changing of the DC converters' ULTCs in the sequential DC power flow algorithm, tap-changing effects are included in the Jacobian matrix through the newly obtained AC power equations. Hence, a faster convergence is achieved. The sequential DC power flow algorithm is performed using the linear current-balancing method, and thus

the convergence of the algorithm is accelerated. The sequential DC power flow algorithm is performed for each DC subsystem separately. Thus, modularity and flexibility are provided for including or removing any DC subsystems without needing to change the proposed AC/DC power flow algorithm. Comparative results have shown that the proposed approach provides accurate and reliable results for practical applications, while previous studies ignore the real equivalent circuits for the ULTCs of the DC converters and are not able to meet accuracy and reliability criteria.

## References


[1] Chen L, Pan H, Deng C, Zheng F, Li Z, Guo F. Study on the application of a flux-coupling-type superconducting fault current limiter for decreasing HVDC commutation failure. Can J Elect Comput E 2015; 38: 10-19.

[2] Zhao X, Li K. Droop setting design for multi-terminal HVDC grids considering voltage deviation impacts. Electr Pow Syst Res 2015; 123: 67-75.

[3] Gavriluta C, Candela I, Citro C, Luna A, Rodriguez P. Design considerations for primary control in multi-terminal VSC-HVDC grids. Electr Pow Syst Res 2015; 122: 33-41.

[4] Watanabe C, Itou Y, Sasaki H, Murata Y, Suizu M, Sakamaki M, Watanabe M, Katakai S. Practical application of +/– 250 kV DC-XLPE cable for Hokkaido-Honshu HVDC link. Electr Eng Jpn 2015; 191: 18-31.

[5] Moon JW, Park JW, Kang DW, Kim JM. A control method of HVDC-modular multilevel converter based on arm current under the unbalanced voltage condition. IEEE T Power Deliver 1995; 30: 529-536.

[6] Smed T, Andersson G, Sheble GB, Grigsby LL. A new approach to AC/DC power flow. IEEE T Power Syst 1991; 6: 1238-1244.

[7] Arrillaga J, Harker BJ, Turner KS. Clarifying an ambiguity in recent AC-DC load flow formulation. IEE Proc-C 1980; 12: 324-325.

[8] Arifoglu U. Load flow based on Newton's method using Norton equivalent circuit for AC-DC multiterminal systems. Eur T Electr Power 1999; 9: 167-174.

[9] Marsafawy MM, Mathur RM. A new fast technique for load flow solution of integrated multiterminal DC-AC systems. IEEE T Power Ap Syst 1980; 99: 246-255.

[10] Messalti S, Belkhiat S, Saadate S. A new approach for load flow analysis of integrated AC-DC power systems using sequential modified Gauss–Seidel methods. Eur T Electr Power 2012; 22: 421-432.

[11] De Silva JR, Arnold CP. A simple improvement to sequential AC/DC power flow algorithms. Int J Elec Power 1990; 12: 219-221.

[12] Reeve J, Fahmy G, Stott B. Versatile load flow method for multiterminal HVDC systems. IEEE T Power Ap Syst 1977; 96: 925-933.

[13] Sato H, Arrillaga J. Improved load flow techniques for integrated AC-DC systems. IET Proc 1969; 116: 525-532.

[14] Yalcin F. A new approach for optimal power flow calculation in AC–DC system including FACTS devices. PhD, Sakarya University, Sakarya, Turkey, 2013.

[15] Zhang BM, Chen SS, Yan Z. Advanced Power System Network Analysis. 2nd ed. Beijing, China: Tsinghua University Press, 2001.

[16] Arrillage J, Watson NA. Computer Modelling of Electrical Power Systems. 2nd ed. Chichester, West Sussex, UK: Wiley, 2007.

[17] Parbha K. Power System Stability and Control. New York, NY, USA: McGraw-Hill, 1993.

[18] Liu C, Zhang B, Hou Y, Wu FF, Liu Y. An improved approach for AC-DC power flow calculation with multi-infeed DC systems. IEEE T Power Syst 2011; 26: 862-869.

[19] Fan J, Bo Z. Modelling of on-load tap-changer transformer with variable impedance and its applications. In: Proceedings of the IEEE 1998 International Conference on Energy Management and Power Delivery; 3–5 March 1998; New York, NY, USA: IEEE. pp. 491-494.

[20] Jimenez JC, Nwankpa CO. Analysis of reconfigurable tap changing transformer model through analog emulation. In: Proceedings of the IEEE 2009 International Symposium on Circuits and System; 24–27 May 2009; Taipei, Taiwan. New York, NY, USA: IEEE. pp. 1989-1992.

[21] Yalcin F, Arifoglu U. Inserting the tap values of the tap changer transformers into the Jacobian matrix as control variables. Sau J Sci 2013; 17: 337-348.

[22] Sellick, RL, Åkerberg, M. Comparison of HVDC light (VSC) and HVDC classic (LCC) site aspects, for a 500 MW 400 kV HVDC transmission scheme. In: Proceedings of the 10th IET International Conference on AC and DC Power Transmission; 4–5 December 2012; Birmingham, UK: IET. pp. 1-6.

[23] Ong CM, Hamzei-Nejad A. A general purpose multiterminal DC load flow. IEEE T Power Ap Syst 1981; PAS-100: 3166-3174.

[24] Arifoglu U. The power flow algorithm for balanced and unbalanced bipolar multiterminal AC-DC systems. Electr Pow Syst Res 2003; 64: 239-246.