Turkish Journal of Electrical Engineering & Computer Sciences

http://journals.tubitak.gov.tr/elektrik/

Research Article

Turk J Elec Eng & Comp Sci
(2017) 25: 3578 – 3590

doi:10.3906/elk-1512-86

Improved resettable integrator control for a bridgeless interleaved AC/DC converter

Kanimozhi GUNASEKARAN*, Sreedevi VELLITHIRUTHI THAZHATHU
School of Electrical Engineering, VIT University, Vandalur - Kelambakkam, Chennai, Tamilnadu, India

Received: 10.12.2015 • **Accepted/Published Online:** 12.06.2017 • **Final Version:** 05.10.2017

Abstract: Plug-in hybrid electric vehicles (PHEVs) consist of a front-end boost rectifier, which incorporates a power factor correction (PFC) circuit for battery charging. Bridgeless interleaved (BLIL) PFC boost converter topology is proved as a standard PFC converter as it has high efficiency, reduced input current ripple, and reduced electromagnetic interference (EMI). This paper proposes a digital nonlinear control technique that employs a resettable integrator to shape the input current of the converter in phase with the input voltage to achieve high input power factor. This control approach rejects power source and load perturbations better than linear feedback control methods. This is accomplished by summing up the sensed input current of a BLIL converter with a fictitious current synthesized with the input voltage. In this work, a BLIL converter is analyzed for its input power factor improvement, voltage stress across the devices, and dynamic response under variable supply and load conditions using simulation. The hardware is tested for a 300 W BLIL boost converter to validate the simulated results. The performance of the proposed controller is compared with that of conventional average current mode control. The experiment and simulation results prove that the resettable integrator controller shows a better performance than the conventional controller.

Key words: AC/DC PFC converter, bridgeless interleaved, control techniques, PI control, integrator control, power factor correction

1. Introduction

A plug-in hybrid electric vehicle (PHEV) has a battery storage system, which can be recharged by connecting a plug to an external electric power supply. The front-end AC/DC PFC boost converter [1] is the main component of the charger system. The front-end converter rectifies the input AC voltage and transfers it to a regulated intermediate DC link bus. The DC bus follows an isolated DC/DC stage that converts the bus voltage to a boosted regulated DC voltage for charging batteries. Bridgeless interleaved (BLIL) PFC boost converter topology [2] is proved as a standard PFC converter as it has high efficiency, reduced input current ripple, and lower electromagnetic interference (EMI).

A BLIL converter in an open loop suffers from poor output voltage regulation, reduced efficiency for wider load range, poor power quality in terms of power factor, and input current ripples. The above problems can be reduced by implementing various current control techniques [3] for the converters. Linear current control techniques such as average current mode control [4,5], peak current mode control [6], and hysteresis current mode control [7,8] are reported in the literature. However, linear control techniques cannot perform optimally over the whole operating range as it results in sluggish response and instability for variable load and supply

*Correspondence: gkanimozhi2312@gmail.com

conditions. Therefore, for the precise approach nonlinear control techniques are used, which gives fast transient response with less overshoot or undershoot. Nonlinear techniques such as Lyapunov control [9], differential flatness control [10,11], and one cycle control [12] exhibit inherent immunity to system variations. However, the controller based on Lyapunov or flatness theory controls the input power by utilizing large bandwidth in a power control loop and necessitates a specific load profile. This also results in the complex programming of the battery charging curve in the DSP processor with increased memory allocation. A controller based on one cycle technique is simple and robust to implement and it has been proven efficient for AC/DC bidirectional converters [13], active power filters [14], and grid-connected inverters [15]. A control strategy based on the application of one cycle control technique under hybrid PWM is applied for a three-phase three-level neutral point clamped voltage source converter [16] and with a dynamic second-order voltage estimation technique for a single-phase PFC rectifier [17]. Better control is reported due to the modified scheme.

In this paper, an improved resettable integrator is proposed for input power factor correction together with voltage regulation for a BLIL boost converter. A fictitious current is synthesized with the input voltage and it is summed up with the sensed current in the improved resettable integrator approach. This resulting current is compared with a saw-tooth waveform to generate the gating pulses to the switches of the converter. This approach is applicable for constant frequency converters and it rejects power source and load perturbations better than conventional linear feedback control. The major advantage of the proposed technique is that it eliminates the input side harmonics as well as traces the transients. This control technique can be implemented in various converter topologies for leading edge and trailing edge modulation. In this work, the converter is analyzed for leading edge modulation and the output signal is integrated until it reaches the reference signal. The improved resettable integrator scheme is compared with conventional average current control in improving the power factor and dynamic characteristics of the converter. The average current mode control is termed as a traditional PI control in the paper.

The principle of operation of bridgeless interleaved boost converter is discussed in Section 2. Section 3 describes the analytical modeling of the converter and the design of the improved resettable integrator controller is dealt with in Section 4. Simulation results and comparison with conventional PI control are provided in Section 5 and Section 6 discusses the hardware results, followed by the conclusion in Section 7.

2. Principle of operation of the bridgeless interleaved PFC boost converter (BLIL)

The topology of the bridgeless interleaved boost converter [18,19] is shown in Figure 1. It is a modification of interleaved boost converter [20]. The power circuit consists of four inductors ($L1, L2, L3$, and $L4$), four MOSFETS ($Q1$ to$Q4$), four diodes ($D1$ to $D4$), and a DC link capacitor (C_{01}). As the name implies, the input diode bridge rectifier is eliminated and in addition it consists of two MOSFETs and two fast diodes. It reduces the input current ripple compared to the interleaved boost converter. Each phase of the circuit is connected to two interleaving inductors, which reduce the current stress on the device and in turn filter components. The working of the circuit is explained for a duty cycle less than 50%, i.e. in discontinuous conduction mode. The modes of operation for a positive half cycle of input voltage are described below.

2.1. Mode 1

During mode 1, the gating pulses are given to switches $Q1 - Q2$ and the energy is stored in inductors $L1$ and $L2$. Let Δi_{L1} and Δi_{L3} be the ripple current through inductors $L1/L2$ and $L3/L4$, respectively. The ripple

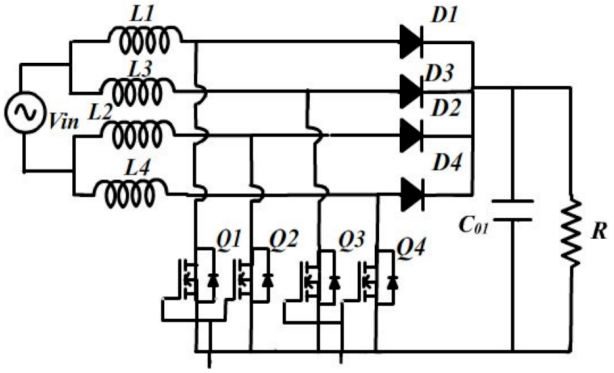

Figure 1. Bridgeless interleaved PFC boost converter.

current through series inductances $L1$ and $L2$ is given as

$$\Delta i_{L1} = \frac{1}{L1 + L2} V_{in} \delta T_s \tag{1}$$

The energy in inductors $L3$ and $L4$ is released through the diode $D3$, load, and body diode of $Q4$ to the supply as shown in Figure 2a. The ripple current through inductors $L3$ and $L4$ is

$$\Delta i_{L3} = \frac{1}{L3 + L4} (V_o - V_{in}) \delta T_s \tag{2}$$

The input current ripple ΔIin will be the sum of currents through inductors $L1/L2$ and $L3/L4$ and is given as

$$\Delta Iin = \frac{1}{L1 + L3} V_o (1 - \delta) T_s, \tag{3}$$

where δ is the duty cycle, T_s is the time period, V_o is the output voltage, and V_{in} is the input voltage of the converter.

2.2. Mode 2

The circuit operation in mode 2 is shown in Figure 2b. The switches $Q3$ and $Q4$ are turned ON and the input current flows through inductor $L3$, switches $Q3 - Q4$, and inductor $L4$. The energy is stored in inductors $L3 / L4$.The ripple current through the inductors $L3 / L4$ is given as

$$\Delta i_{L3} = \frac{1}{L3 + L4} V_{in} \delta T_s \tag{4}$$

The stored energy in inductor $L1$ and $L2$ during mode 1 is released through $D1$, load, and body diode of $Q2$. The resulting ripple current is

$$\Delta i_{L1} = \frac{1}{L1 + L2} (V_o - V_{in}) \delta T_s \tag{5}$$

The input current ripple ΔIin is expressed as

$$\Delta Iin = \frac{2}{L1 + L3} V_{in} (\delta - \frac{1}{2}) T_s \tag{6}$$

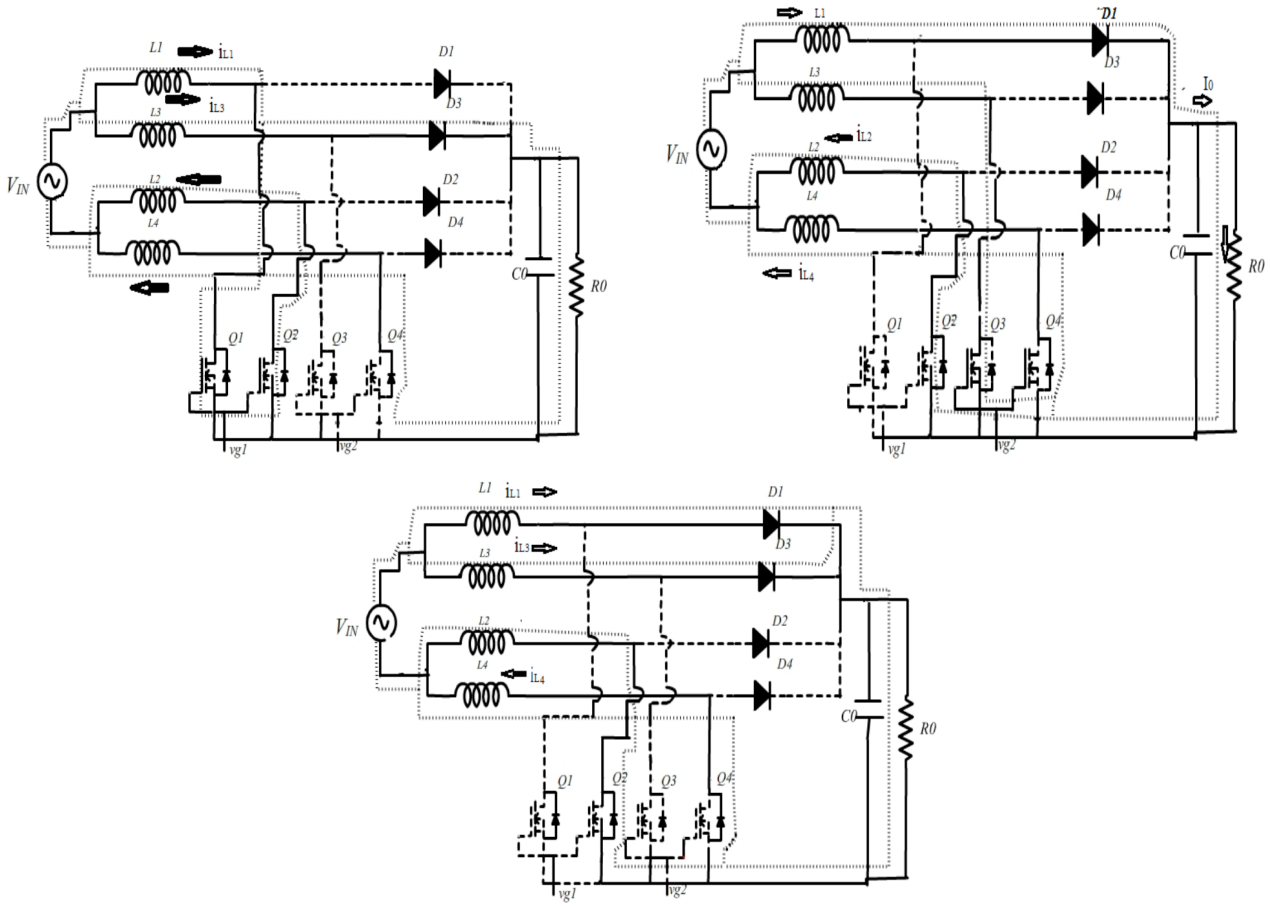

Figure 2. a) Mode 1: Switches $Q1$ and $Q2$ are ON. b)Mode 2: Switches $Q3$ and $Q4$ are ON. c) Mode 3: Body diodes of $Q2$ and $Q4$ are conducting.

2.3. Mode 3

The gating pulses to all the switches are removed. In this mode, the body diodes of switches $Q2$ and $Q4$ are conducting, as shown in Figure 2c. The input current takes the path from supply - $L1 - D1$ - load - $D4 - L4$ and $L3 - D3$ - load - $D2 - L2$.The current through series inductances $L1/L2$ and $L3/L4$ is given as

$$\Delta i_{L1} = \frac{1}{L1 + L2}(V_o - V_{in})(\frac{1}{2} - \delta)T_s \tag{7}$$

$$\Delta i_{L3} = \frac{1}{L3 + L4}(V_o - V_{in})(\frac{1}{2} - \delta)T_s \tag{8}$$

The input ripple current ΔIin is given as

$$\Delta Iin = \frac{1}{L1 + L3}V_o(1 - \delta)T_s \tag{9}$$

The circuit operation is the same during a negative half cycle of the input voltage.

3. Analytical modeling of the converter

The various components of the converter are selected based on the analytical modeling of the converter. The selection of the semiconductor devices is based on the analytical equations for rms and average value of current stress of the switches and derived on the following assumptions: (a) The converter is operating in continuous conduction mode (CCM), (b) the input voltage is sinusoidal and it operates with unity power factor, and (c) the output voltage is ripple free. For the typical boost converter, MOSFET duty cycle $\delta_Q(\theta)$ is given as

$$\delta_Q(\theta) = 1 - \frac{|vin(\theta)|}{V_o} = 1 - \frac{V_p \left|\sin\theta\right|}{V_o}, \tag{10}$$

where V_p is the peak value of input voltage. Assuming the inductor current to be sinusoidal and it is given as

$$i_L = Ip \left|\sin(\theta)\right|, \tag{11}$$

where Ip is the peak value of the input current. The instantaneous MOSFET current $i_Q(\theta)$ and its RMS value of current i_{Q-rms} can be given as

$$i_Q(\theta) = I_p \left|\sin(\theta)\right| .\delta_{Q-rms} \tag{12}$$

$$i_{Q-rms} = [\frac{1}{\pi}\int_0^{\pi} [I_p \left|\sin(\theta)\right| (1 - \frac{V_p \left|\sin(\theta)\right|}{V_0})]^2]^{1/2} d\theta \tag{13}$$

The diode duty cycle $\delta_D(\theta)$ can be given as

$$\delta_D(\theta) = 1 - \delta_Q(\theta) = \frac{V_p \left|\sin\theta\right|}{V_o} \tag{14}$$

The instantaneous value of current through the diode and its RMS value can be given as

$$i_D(\theta) = I_p \left|\sin(\theta)\right| \frac{V_p \left|\sin\theta\right|}{V_o} \tag{15}$$

$$i_{D-rms} = [\frac{1}{\pi}\int_0^{\pi} [I_p \left|\sin(\theta)\right| (\frac{V_p \left|\sin(\theta)\right|}{V_0})]^2]^{1/2} d\theta \tag{16}$$

The input ripple current ΔI_{rp} through the inductor is assumed to be half of the peak of the inductor current (I_p).

$$\Delta I_{rp} = \frac{1}{2} I_p \tag{17}$$

The inductor value can be obtained from inductor current ripple as follows:

$$\Delta I_L = \frac{V_p \sqrt{2} D}{f_s L/2}, \tag{18}$$

where L is the inductor value connected to each phase. The output capacitor current has both high frequency and low frequency components and are given as

$$I_{c-rms(low)} = \frac{I_0}{\sqrt{2}} = \frac{\sqrt{2}}{2}\frac{P_o}{V_o} \text{ and } I_{c-rms(high)} = \frac{Pin}{V_o}\sqrt{\frac{16V_o}{6\pi V_p} - \frac{P_o^2}{P_{in}^2}} \tag{19}$$

The output capacitor value is calculated from

$$C_0 = \frac{2P_o/f}{V_o^2 - (V_o - \Delta Vc)^2}, \tag{20}$$

where ΔV_C is the output capacitor ripple voltage. The gain of the converter is given by the expression

$$G = \frac{Vo}{Vin} = 1/(1-D) \tag{21}$$

and hence the voltage stress Vst across the semiconductor devices is expressed as

$$Vst = GVin = Vo \tag{22}$$

4. Design of an improved resettable integrator controller

In this section, the basic operation of a switch in one cycle control technique [21,22] is explained. The switch operates according to the switch function $k(t)$ at a frequency $f_o = \frac{1}{T_s}$, where $k(t) = 1\ 0 < \quad t < T_{on}$

$$0Ton < t < T_s \tag{23}$$

T_{on} being the switch ON time. The input signal $x(t)$ is chopped by the switch and transferred to the output and the output variable is given as $y(t)$. The switching frequency of the converter f_o is much greater than the frequency of the input signal $x(t)$ or the reference signal $V_r(t)$ and hence both the parameters can be taken as constant. Now $y(t)$ is given as

$$\begin{aligned} y(t) &= \tfrac{1}{T_s} \int_0^{T_{on}} x(t)dt \\ &= \tfrac{1}{T_s} x(t) \int_0^{T_{on}} dt = x(t)\delta(t) \end{aligned} \tag{24}$$

Duty ratio is modulated in such a way that integration of the switched variable is equal to the integration of the reference signal $V_r(t)$ as stated in Eq. (6).

$$\begin{aligned} &\int_0^{T_S} x(t)dt = \int_0^{T_S} V_r(t)dt \\ &y(t) = \tfrac{1}{T_S} \int_0^{T_S} x(t)dt \\ &= \tfrac{1}{T_S} \int_0^{T_S} V_r(t)dt = V_r(t) \end{aligned} \tag{25}$$

Hence the switched variable average is instantaneously controlled within one cycle. The block diagram of the improved resettable integrator controller is shown in Figure 3. The output voltage V_{sen} is obtained from a voltage sensor and is fed as input to the voltage error amplifier $(C1)$. The error voltage $V_c(t)$ is given to a classic PI controller to produce a voltage $Vm(t)$. The controlled signal $Vm(t)$ is integrated by resettable integrator and a ramp voltage of variable magnitude is generated for every switching cycle. The resulting voltage is given to the noninverting terminal of the comparator $C2$. The logic used to generate switching signals is shown in Figure 4. For the raising edge of the clock pulses, the switches $Q1$ and $Q2$ are turned ON and the

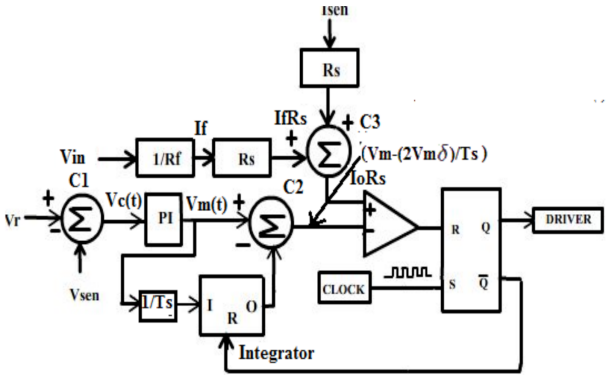

Figure 3. Block diagram of improved resettable integrator control technique.

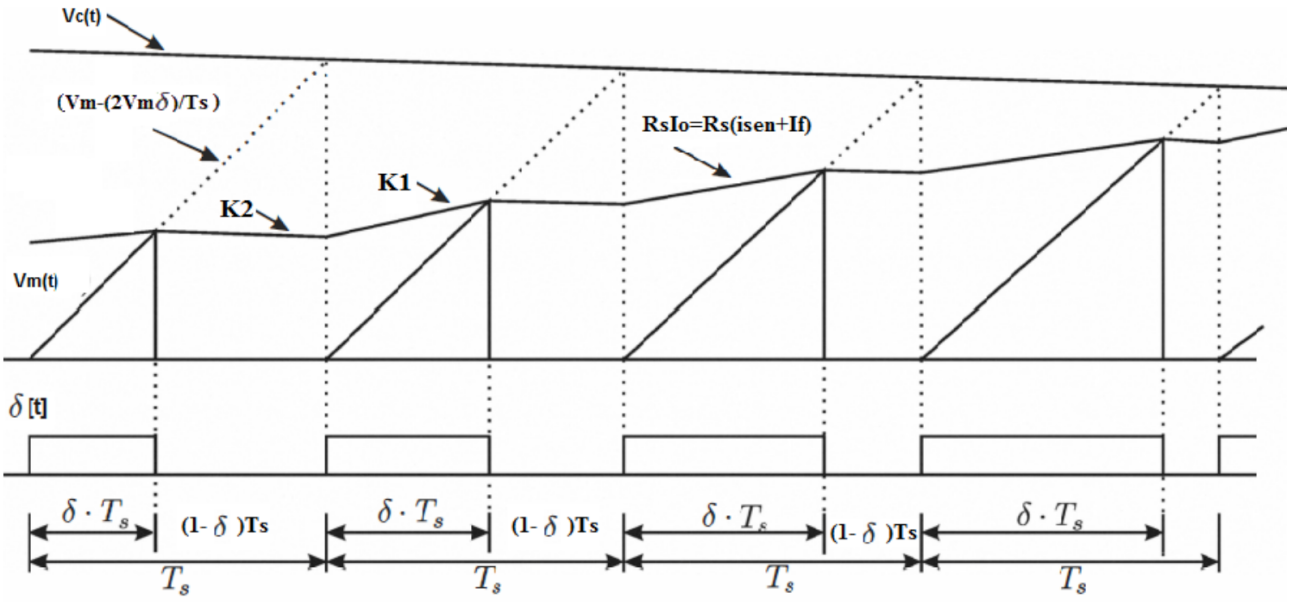

Figure 4. Control logic of improved resettable integrator for pulse generation.

current through the inductors $L1$ and $L2$ increases. The equation for the rising edge slope $K1$ of the inductor current $I_{sen}(t)$ is given as

$$K1 = \frac{Rs(Vin + Vo)}{L}, \tag{26}$$

where Rs is the gain of the current sensor and L is the sum of $L1$ and $L2$. The turn off time of the switches $Q3$ and $Q4$ is decided by the comparator output $C2$. The falling slope $K2$ of the sensed inductor current is given as

$$K2 = \frac{Rs(Vin - Vo)}{L} \tag{27}$$

A fictitious current If proportional to the input voltage is synthesized by multiplying sensed source voltage Vin by a gain of $1/Rf$. It is summed up with $IsenRs$ to get the resulting signal $IoRs$. The signal $IoRs$ is compared $(C3)$ with saw-tooth waveform to obtain the switching pulses. Now the control equation of the

controller is given as

$$Rs(Isen + If) = Vm(1 - 2d) \tag{28}$$

The peak value of the input current is given as

$$Isen = \frac{VmVin}{VoRs} \tag{29}$$

Hence the current equation for the proposed controller is given as

$$Isen + If = \frac{(VmVin)}{VoRs} \tag{30}$$

$$\text{(or) } \frac{Vin}{Re} + \frac{Vin}{Rf} = \frac{(VmVin)}{VoRs}, \tag{31}$$

where R_e is the emulated resistance of the converter.

Therefore

$$Vm = \frac{Rs}{Re}(Vo) + \frac{Rs}{Rf}(Vo) \tag{32}$$

The effective value of emulated resistance R_{e2} offered by the controller is

$$R_{e2} = \frac{RfRe}{Rf + Re} \tag{33}$$

Thus for every switching period, the integrator resets and the ramp voltage starts from zero for the next switching cycle. Thus, the above controller eliminates the input perturbations and load disturbances in one switching period. The overall control structure is simple and easy to implement.

5. Controller realization through simulation

In this section, the performance comparison of the converter based on both conventional PI control and improved resettable integrator control are discussed. The detailed simulation studies for both controls are carried out using PSIM software. The BLIL converter specifications are as follows: output power $P_o = 300\,W$, output voltage $Vo = 400\,V$, switching frequency $f_s = 70\,kHz$, inductors $L1 = L2 = L3 = L4 = 0.63\,mH$, capacitor $= 470\,\mu F$.

The control algorithms are implemented using a TMS320LF28335 DSP processor. The processing speed and the external clock frequency for the processor are configured as 150 MHz and 30 MHz. The simulated dynamic response of the converter using the conventional control technique, when the input voltage is changed from 230 $Vrms$ to 110 $Vrms$, is shown in Figure 5. It can be seen that when the supply voltage is reduced, the input current tracks the voltage only after two cycles to correct the power factor closer to 0.9. This is because of the sluggish external voltage loop, which should first detect the change in output voltage and the current reference is changed accordingly. It adjusts the duty cycle of the switches, which results in the slow response of the conventional controller. Similarly Figures 6a and 6b show the response of the output voltage when a negative and positive step load change is introduced at $t = 0.38\,s$ and it takes more than 4 cycles $(t > 0.08s)$ to attain the steady state condition. To predict the performance of the improved resettable integrator, the PI controller with gain $(K_p = 1, K_I = 33.33)$ is tested for power factor correction with supply variations. It is

obvious that the input power factor remains 0.99 for both the cases, in spite of the input voltage change as shown in Figure 7. Here the input current traces the instantaneous value of input voltage very fast and hence the figure shows a very good power factor with the proposed controller.

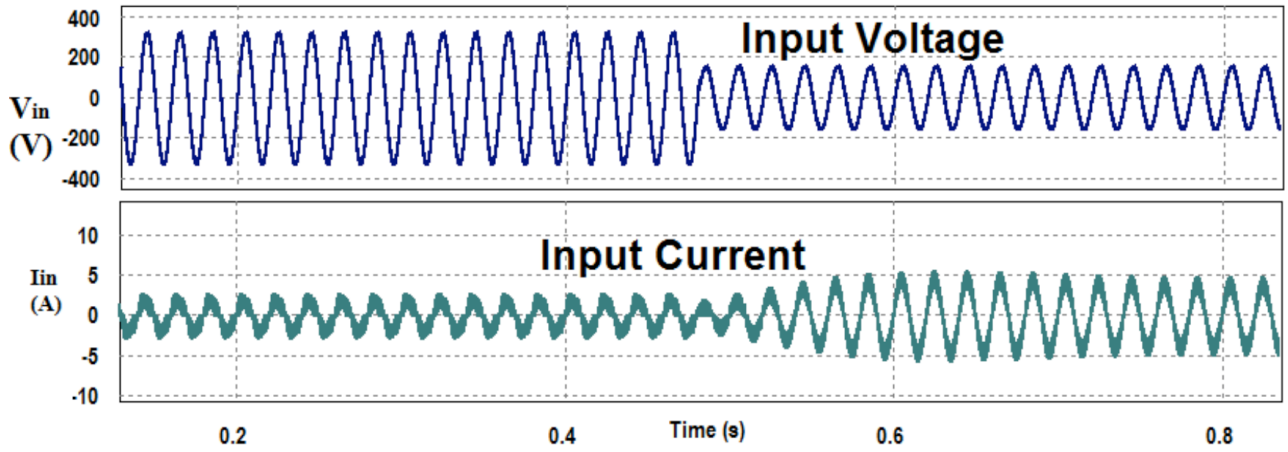

Figure 5. Simulated waveforms of input voltage and input current of BLIL when input voltage is changed from 230 Vrms to 110 Vrms with conventional control.

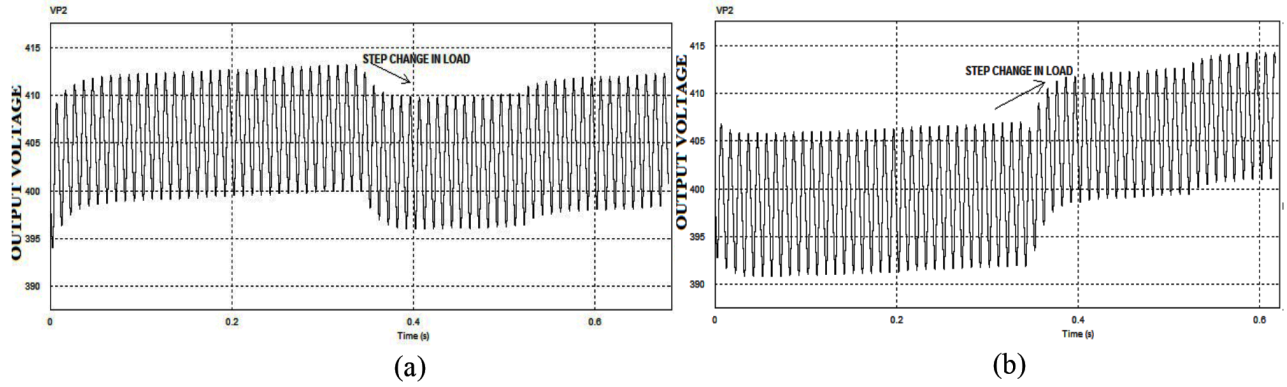

Figure 6. Dynamic response of output voltage (a) negative step load change and (b) positive step load change using PI control.

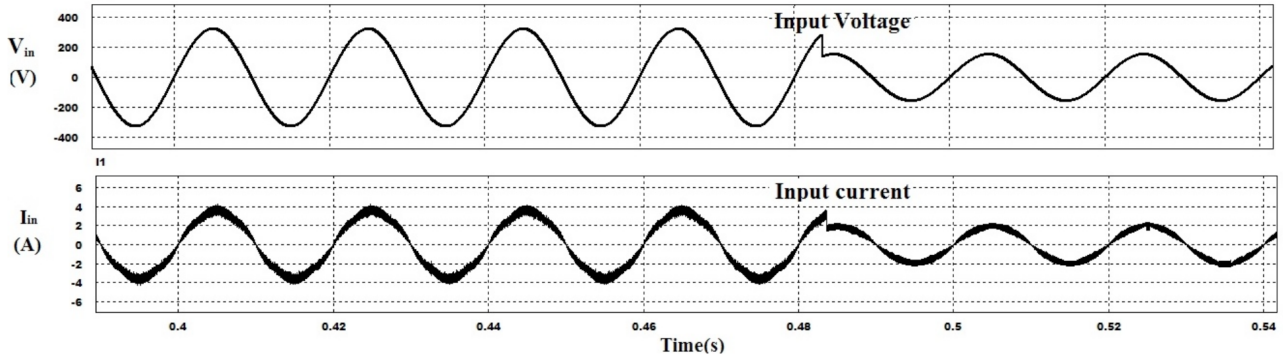

Figure 7. Waveforms of input voltage, current for 230 Vrms and 110 Vrms power supply.

The voltage stress on the devices is reduced as compared to the conventional control method as illustrated

in Figures 8a and 8b. The controller rejects the disturbances in one switching cycle, which eliminates the overshoot and undershoots of voltage across the device. A step load change of 320 W is introduced as shown in Figure 9 at time $t = 0.38\,s$ to demonstrate the fast dynamic response of the proposed controller. This illustrates that the controller adjusts the duty cycle instantaneously and the output voltage attains its steady state in less than three cycles $(t < 0.06s)$.

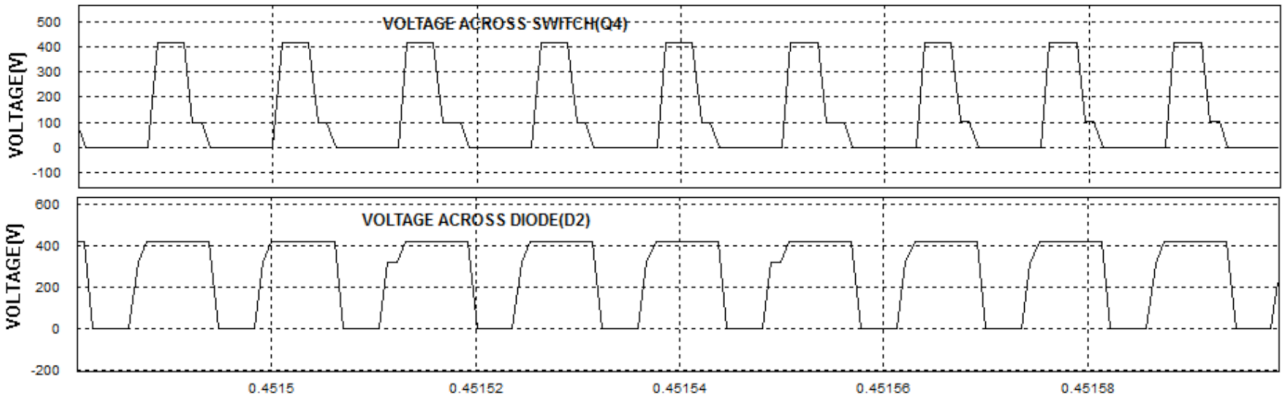

Figure 8. (a) Voltage across the switch $(Q4)$, (b) Voltage across the diode (D2).

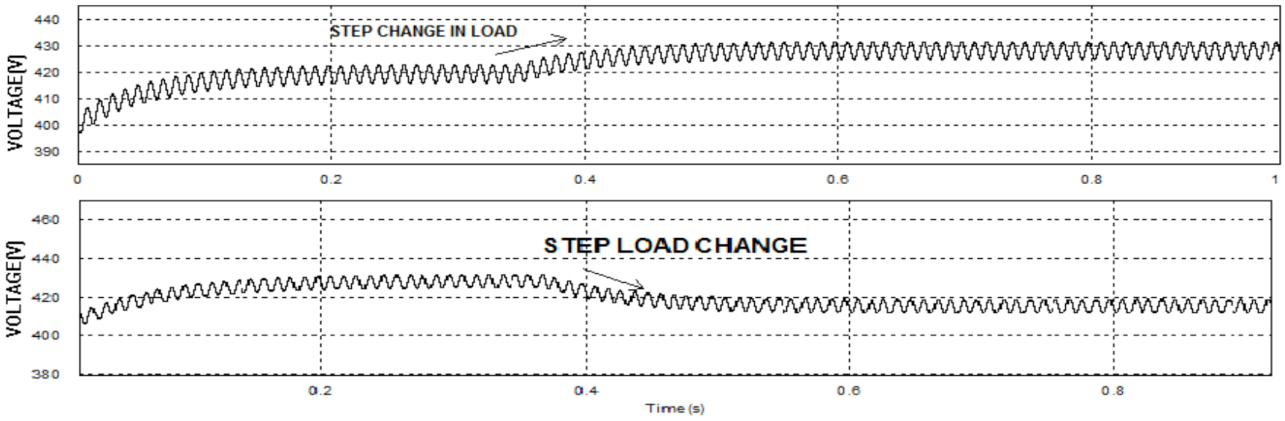

Figure 9. Dynamic response of output voltage for (a) positive step load change (b) negative step load change with proposed controller.

6. Hardware results

A prototype of 300 W is designed to verify the dynamic performance of the controller. A DSP processor TMS320LF28335 is used to implement both the conventional and resettable integrator algorithms.

TMS320LF28335 is a floating point processor and has 32-bit fixed point architecture as C28 $\times\times$ DSCs, which includes a single precision IEEE 754 floating point unit. In addition, the processor has 32 $\times$ 32 MAC and 64-bit processing capability, which results in high performance on handling numerical resolution problems. The input voltage and input current waveform are depicted in Figures 10a and 10b for 230 Vrms and 110 Vrms. The power factor is maintained closer to unity when the input voltage is reduced from 230 Vrms to 110 Vrms. Figures 11a and 11b show the power factor correction of the controller for various load condition such as 20% (60 W) and 75% (230 W). The power factor for the system is found to be 0.84 for light load condition and 0.99 for full

load condition. The THD of input current at full load with predominant third and fifth harmonic components is shown in Figures 12a and 12b. The third harmonic component is 4.8% and fifth harmonic component is 4.9%, which are well within IEC 61000-3-2 standard during a wide range of load variations.

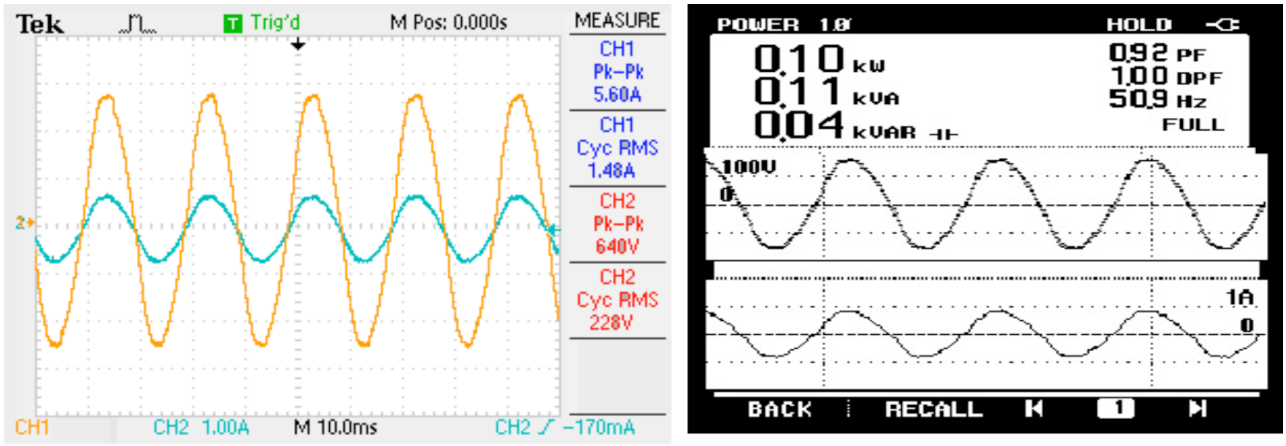

Figure 10. (a) Input voltage and input current waveforms for 230 Vrms, (b) Input voltage and input current waveforms for 110 Vrms.

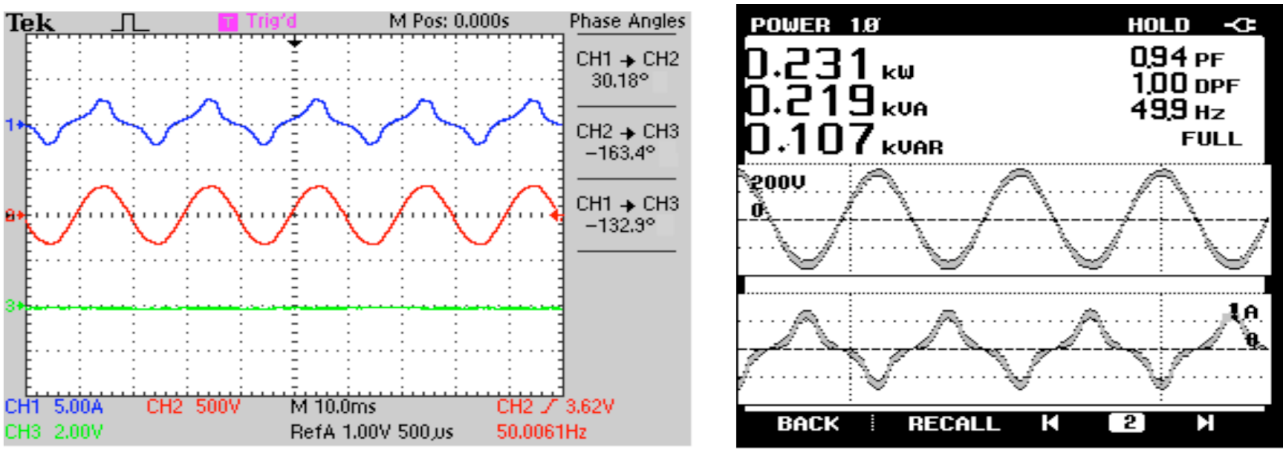

Figure 11. Waveforms showing power factor at (a) 20% load and (b) 75% load.

The variation in power factor with load is shown graphically in Figure 13a. It can be inferred from Figure 13a that improved resettable control operates at a high power factor $(pf > 0.85)$ for all load conditions, whereas the conventional PI control has a poor power factor $(pf \leq 0.57)$ under light load conditions. The comparison between the efficiency of the converter for varying load conditions with the conventional control method and the resettable integrator control is shown in Figure 13b. Thus, the improved resettable integrator controller gives an efficiency of 92% at low load and 97% at full load conditions. Thus it provides a very simple and reliable solution for power factor correction and efficient energy use.

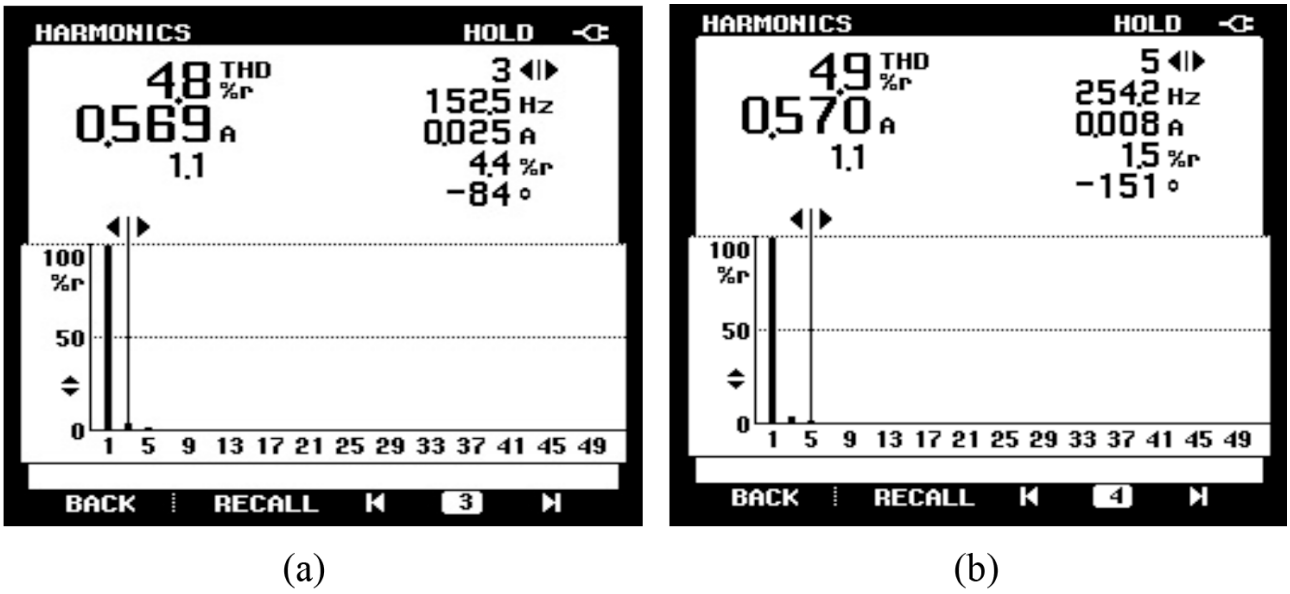

Figure 12. THD of input current showing (a) third and (b) fifth harmonics.

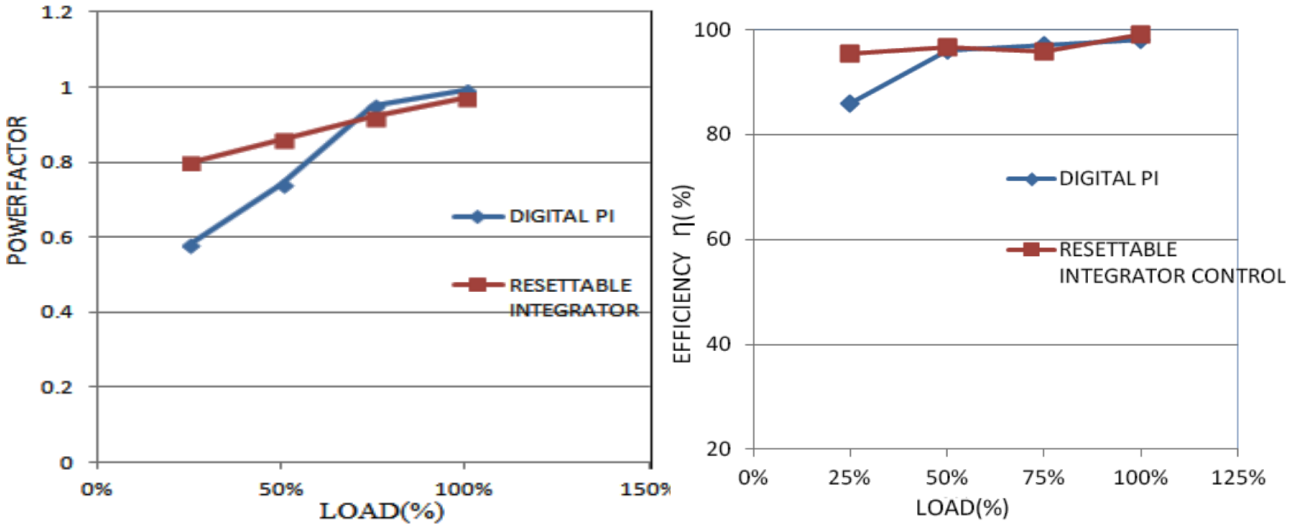

Figure 13. (a) Power factor vs. load, (b) Efficiency comparison of PI control and resettable integrator control.

7. Conclusion

An improved resettable integrator technique is implemented for a bridgeless interleaved PFC boost converter for improving the dynamic performance under variable load and supply conditions. In this improved technique, a fictitious current signal is synthesized with the input voltage, which helps to reject the supply disturbances, and maintains nearly unity power factor. The power factor correction and voltage regulation of the converter are compared with those of the conventional control method. From the simulation and experimental results, it can be observed that the resettable integrator technique is superior for BLIL boost converter used in PHEV battery charger applications.

References

[1] Singh B, Singh BN , Chandra A, Haddad KA, Pandey A, Kothari DP. A review of single-phase improved power quality AC-DC converters. IEEE T Ind Electron 2003; 50: 962-981.

[2] Musavi F, Eberle W, Dunford WD. A high-performance single-phase bridgeless interleaved PFC converter for plug-in hybrid electric vehicle battery chargers. IEEE T Ind Appl 2011; 47: 1833-1843.

[3] Redl R. Power factor correction in single-phase switching mode power supplies - an overview. Int J Electron 1994; 77: 555-582.

[4] Grasblum P. Implementing PFC average current mode control using the MC9S12E128. Freescale Semiconductor Application Note AN3052, 2005.

[5] Zhang Y, Xu W, Yu Y. The PFC with average current-mode and voltage fuzzy controller for the output voltage. In: International Symposium on Intelligent Information Technology Application, IEEE IITA, 2008; pp. 771-775.

[6] Najafi E, Vahedi A, Mahanfar A, Yatim AHM. A new controlling method based on peak current mode (PCM) for PFC. In: IEEE 2008 Power and Energy Conference PEC; 2008; pp. 1103-1107.

[7] Maswood AI, Liu F. A unity power factor front end rectifier with hysteresis current control. IEEE T Energy Conver 2011; 21: 153-160.

[8] Liu YF, Sen PC. Large-signal modeling of hysteretic current-programmed converters. IEEE T Power Electr 1996; 11: 423-430.

[9] Pahlevaninezhad M, Das P, Moschopoulos G, Jain P. A study of nonlinear controller for AC/DC boost PFC converters. In: IEEE Explorer 2013; 1878-1883.

[10] Pahlevaninezhad M. A new control approach based on the differential flatness theory for an AC/DC converter used in electric vehicles. IEEE T Power Electr 2012; 27: 2085-2103.

[11] Das P, Pahlevaninezhad M, Drobnik J, Moschopoulos G, Jain PK. A nonlinear controller based on a discrete energy function for an AC/DC boost PFC converter. IEEE T Power Electr 2013; 28: 5458-5476.

[12] Smedley KM, Cuk S. One cycle control of switching converters. IEEE T Power Electr 1995; 10: 625-633.

[13] Ghodke DV, Sreeraj ES, Chatterjee K, Fernandes BG. One cycle-controlled bidirectional AC to DC converter with constant power factor. IEEE T Ind Electr 2009; 56: 1499-1510.

[14] Jin T, Smedley KM. Operation of unified constant-frequency integration controlled three phase active power filter with unbalanced load. Proc IEEE APEC 2003; 1: 148-153.

[15] Qiao C, Smedley KM, Maddaleno F. A single-phase active power filter with one-cycle control under bipolar operation. IEEE T Circuits Syst 2004; 51: 1623-1630.

[16] Bento AAdM, Vieira PKP, Silva ERCd. Application of the one-cycle control technique to a three-phase three-level NPC rectifier. IEEE T Ind Appl 2014; 50: 1177-1184.

[17] Chiang HC, Lin FJ, Chang JK, Chen KF, Chen YL, Liu KC. Control method for improving the response of single-phase continuous conduction mode boost power factor correction converter. IET Power Electr 2016; 9: 1792-1800.

[18] Musavi F, Eberle W, Dunford WG. A high-performance single-phase AC-DC power factor corrected boost converter for plug in hybrid electric vehicle battery chargers. In: IEEE Energy Conversion Congress and Exposition Atlanta, Georgia, 2010.

[19] Musavi F, Eberle W, Dunford WG. Efficiency evaluation of single-phase solution for AC-DC PFC boost converters for plug-in hybrid electric vehicle battery chargers. In: IEEE Vehicle Power and Propulsion Conference Lille, France, 2010.

[20] Loughlin M. An Interleaved PFC pre-regulator for high-power converters. Topic 5: Texas Instrument Power Supply Design Seminar, 2000; 5-14.

[21] Chen M, Mathew A, Sun J. Nonlinear current control of single-phase PFC converters. IEEE T Power Electr 2007; 22: 2187-2194.

[22] Sudheer L, Kanimozhi G, Sreedevi VT. Integrator controlled semi-bridgeless PFC boost converter. In: IEEE 2015 International Conference on Circuit, Power and Computing Technologies 2015; India: IEEE. pp. 1-6.