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Calculation of current limiting reactance of hybrid SFCL for low voltage ride-through capability enhancement in DFIG wind farms

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Abstract: This paper presents a new approach for the low voltage ride-through capability enhancement of doubly-fed induction generator (DFIG) wind farms using a hybrid superconducting fault current limiter (SFCL) of the first peak current limiting type, which has the advantage of a fast recovery time. A design for the hybrid SFCL, focusing on current limiting reactor (CLR) reactance calculation, is proposed in this paper to determine an appropriate value for the CLR reactance that satisfies the grid code requirements of the DFIG wind turbines. High-temperature superconductors (HTS) such as Bi-2212, YBCO, Bi-2223, Ti-2223, and Hg-1223 are investigated for use in the hybrid SFCL. The recovery time and first peak current reduction effectiveness are the criteria for selecting the HTS. In the proposed method, a during-fault voltage from the grid code requirement is used as an input parameter to compute the reactance of the CLR. Based on the results of the base-case simulations conducted on the DIgSILENT PowerFactory software, the Bi-2223 HTS with the first peak of fault current less than 4.5 kA and recovery time of 2.5 s is selected for adoption in the hybrid SFCL. The calculated results of the proposed method are compared with the simulation results of the hybrid SFCL, in terms of the DFIG wind turbine fault ride-through capability enhancement, to demonstrate that the performance of the proposed method satisfies the grid code requirements.

Key words: Doubly-fed induction generator, wind turbines, low voltage ride-through capability, high-temperature superconductor, hybrid superconducting fault current limiter, grid code requirement

1. Introduction

For improving industrial and economic growth, power systems have to generate sufficient electricity to satisfy the demands of the power consumers. Fossil fuels such as coal and natural gas have commonly been utilized to produce electricity in a combined cycle power plant; however, this process emits greenhouse gases such as carbon dioxide and particles into the atmosphere, causing global warming and environmental pollution. To solve this problem, renewable energy, which is clean energy from natural resources comprising wind, solar, hydro, etc., has been directly utilized to generate electricity. Nowadays, wind power is being increasingly used to improve the efficiency of supplying the load reliably. For this reason, the doubly-fed induction generator (DFIG) based on a wind turbine system is becoming one of the most significant topics in power system research, especially from the point of view of fault ride-through or low voltage ride-through capability enhancement. When a fault occurs in a DFIG wind farm, the DFIG should be detached from the grid because of the high rotor current of the DFIG and the power electronic devices protection scheme. However, a large DFIG wind farm tripping may lead to loss in the stability margin and may affect reliability of the electrical system. Thus, an important

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standard of the DFIG wind turbine, called the fault ride-through capability, must be investigated to achieve the grid code demands [1–3]. To solve the low voltage ride-through issue, the protective circuit, which is a resistive crowbar, is implemented on the rotor winding of the DFIG covering the converters. A minimum threshold crowbar for fault ride-through improvement has been experimentally demonstrated in [4]. The low voltage ride-through capability enhancement of the DFIG using a single-phase DC crowbar has been thoroughly investigated in [5]. However, if a disturbance occurs while the crowbar is being activated in the rotor circuit, the converters will open the circuit, causing the DFIG to consume reactive power from the grid, thereby decreasing the voltage at the terminal. The low voltage ride-through capability advancement has been investigated using different concepts to enhance the grid code fulfillment of the DFIG. A performance evaluation of a DC-link brake chopper used to improve the low voltage ride-through is presented in [6]. The rotor side converter (RSC) controller approach, which uses a feed-forward transient current control, has been commonly implemented in DFIGs to improve the low voltage ride-through, suppressing transient rotor currents [7]. In [8] and [9], dynamic voltage restorers have been applied, enhancing the fault ride-through under symmetrical and asymmetrical grid faults. The low voltage ride-through capability improvement in DFIG wind turbines, achieved by controlling the rotor current without crowbars by using a direct control over the rotor magnetic flux, has been proposed in [10], and it diminishes the transients of the rotor current. In [11], an innovative control strategy is proposed, which uses the current control loops of the RSC and the designed grid side convertor (GSC) to enhance the fault ride-through capability of the DFIG wind turbine (2.0 MW/575 V). It is implemented using the PSCAD/EMTP software. Although these techniques can enhance the fault ride-through or low voltage ride-through of the DFIG, the controller designs are very complicated to implement. Moreover, the first peak of the fault current of the DFIG wind turbines cannot be reduced. Thus, superconducting fault current limiters (SFCLs) have been utilized for improving the fault ride-through and for peak fault current reduction. The fault ride-through capability improvement of the DFIG with SFCL has been examined in [12], to verify that it satisfies the grid code requirements. SFCLs combined with other devices for fault ride-through capability enhancement have been utilized in [13] and [14]. However, the actual behaviors of the superconductor, such as the resistance and recovery time, have not been demonstrated adequately. Because the recovery time of the SFCL is several seconds, it can disturb the stability margin of the power system. On the other hand, the long recovery time of the high-temperature superconductors (HTS) cannot handle a reclosing criterion. To reduce the recovery time, a hybrid SFCL technique using a current-limiting resistor/reactor (CLR) as the fault-current–limiting device has been proposed in [15] for utilization in Korean power systems.

This paper offers a hybrid SFCL design based on CLR reactance calculation for improving the fault ride-through capability of DFIG wind turbines, satisfying the grid code requirements of Ireland, Italy, Sweden, and Denmark. The curtailment of the first peak of fault current and recovery time of the superconducting material are considered during the selection of the HTS material used in the hybrid SFCL. The calculated CLR reactance is compared with the simulation results to reveal that the proposed method can determine a CLR that achieves the low voltage ride-through capability stipulated by the grid code requirement.

2. DFIG fault ride-through capability and grid code requirements

The number of large wind farms being installed globally has been increasing continuously, resulting in hundreds of GW of capacity. A major issue faced by large wind farms in power systems is the disturbances existing near the wind farm, which lead to the tripping of wind turbines. This phenomenon can perturb the power system stability or the rotor angle stability. For this reason, a standard for wind turbine requirements, which

is the grid code requirement, was announced to enable wind turbines to ride through the faults without any detachment, called the "fault ride-through capability." The grid code requirements of the wind turbines include a voltage–time characteristic with a minimum satisfactory voltage during fault incidence. Figure 1 demonstrates the voltage profiles of the grid code requirements of various countries [1]. The required during-fault voltages or minimum acceptable voltages (pu) are illustrated in Table 1. For the Italian grid, when the fault occurs, the terminal voltage of the DFIG should not be less than 20%, or 0.2 pu, to enable the DFIG to ride through the fault. When a fault occurs, the terminal voltage of the DFIG decreases instantaneously. In this condition, the DFIG converters, including the RSCs and GSCs, will not be able to improve the voltage sag incidence perfectly because of the converter size limitations. Therefore, when a fault occurs with voltage sag, the SFCL is utilized to solve the problem. Furthermore, the minimum voltage is an important aspect that must be investigated in this paper during the SFCL design, improving the fault ride-through capability of the DFIG satisfying the grid code requirements.

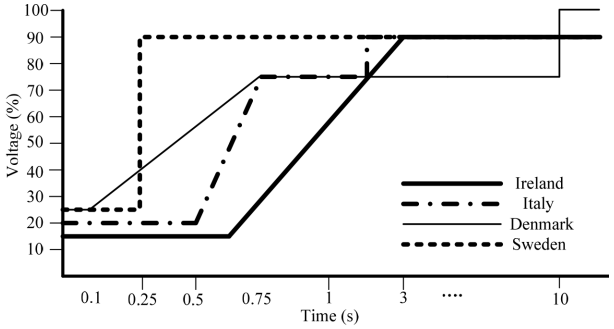

Figure 1. Grid code requirements of various countries.

Table 1. Minimum voltage as per grid code requirement.

Country	Minimum voltage (pu)
Ireland	0.15
Italy	0.2
Denmark <100 kV	0.25
Sweden <100 MW	0.25

3. Hybrid SFCL configuration and thermal-subsystem characteristics

A hybrid SFCL of the first peak limiting type is proposed in [16] to bypass the HTS to another limiter. The hybrid SFCL consists of a superconducting coil using a HTS material connected in parallel with the CLR, as demonstrated in Figure 2. The hybrid SFCL operations include normal and fault operations. In normal condition, the load current flows into the HTS because of zero impedance (S1 closed and S2 open). When a fault occurs, the HTS automatically quenches, rapidly increasing the resistance. In this case, the current will be divided and pass through the driving coil mechanism, acting as a fast switch or magnetic contactor controller. With this phenomenon, S2 closes instantly and then S1 opens, as illustrated in Figure 2b. After the first cycle of the fault, the CLR (as the current-limiting device) instantaneously receives the current stresses, instead of the HTS. The superconductor, which is the HTS, typically operates in three states—flux creep (superconducting state), flux flow, and resistive (normal) state—when the fault occurs. The thermal subsystem model of the HTS is described in [15]. To compute the resistance of the HTS, the electric field in each state must be determined, which can be described by

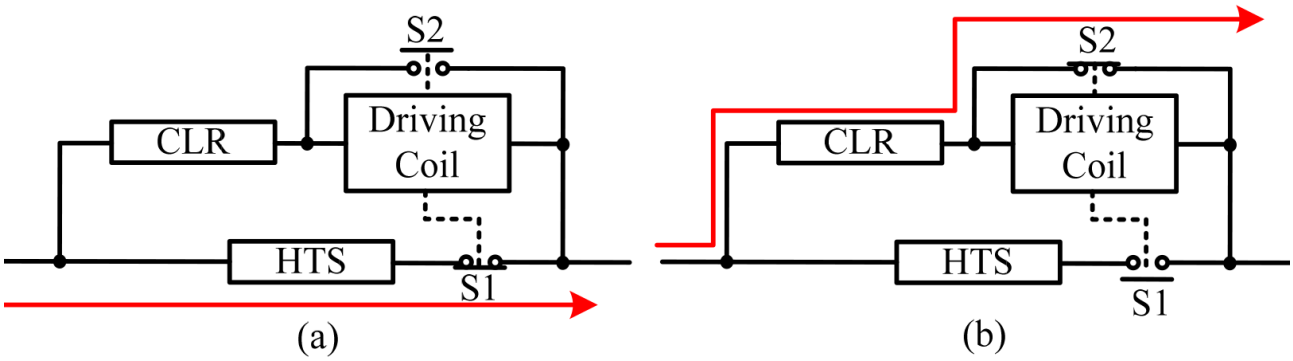

Figure 2. Hybrid SFCL operation: a) Normal condition; b) Fault condition.

$$E_f = E_c \left(\frac{J}{J_{ct}}\right)^{\alpha} \tag{1}$$

$$E_{ff} = E_0 \left(\frac{E_c}{E_0}\right)^{\frac{\delta}{\eta}} \left(\frac{T_c - 77}{T_c - T}\right) \left(\frac{J}{J_c}\right)^{\delta} \tag{2}$$

$$E_n = \rho J \left(\frac{T}{T_c}\right) \tag{3}$$

E_f, E_{ff}, and E_n are the electric fields of the flux creep, flux flow, and resistive states (V/m), respectively. T and $J$are the temperature (K) and current density (A/m^2) of the superconducting coil. The flux creep state exists when the electric field is less than or equal to the critical electric field of the superconducting coil. When the temperature of the superconducting coil becomes greater than the critical temperature, the superconductor will enter the resistive state. In this case, the resistance immediately quenches to curtail the first peak of the fault current. The resistance of the HTS in Ω, which depends on the length L_{sc} (m) and the cross-section area A (m^2) of the HTS, can be expressed as

$$R_{sc} = \frac{E \times L_{sc}}{J \times A} \tag{4}$$

3.1. Calculation of CLR reactance of the hybrid SFCL

This section presents the calculation of the CLR of the hybrid SFCL for fault ride-through enhancement. Figure 3a illustrates the single-line diagram of the DFIG wind farm considered in this paper. The DFIG wind farm includes 10 DFIGs (20 MW, 50 Hz) connected to the grid via transformers (2.222 MVA individual ratings) and the hybrid SFCL. For maximum effectiveness of the DFIG wind turbines' fault ride-through capability enhancement, the hybrid SFCL should be installed close to the DFIG wind farm. From Figure 3a, a simple equivalent circuit of the system during a fault event can be obtained to calculate the total short-circuit current using the short-circuit MVA method, as demonstrated in Figure 3b. In the previous section, the CLR acted as a limiter during the fault (S1 open, S2 closed). Therefore, based on this phenomenon, the equivalent circuit in this state can be acquired as shown in Figure 3b. The largest disturbance, which is a 100 ms symmetrical three-phase fault, is assumed to occur at bus B in the worst-case study because there is a possibility for fault incidence at that point. A procedure to determine the appropriate CLR reactance is shown below.

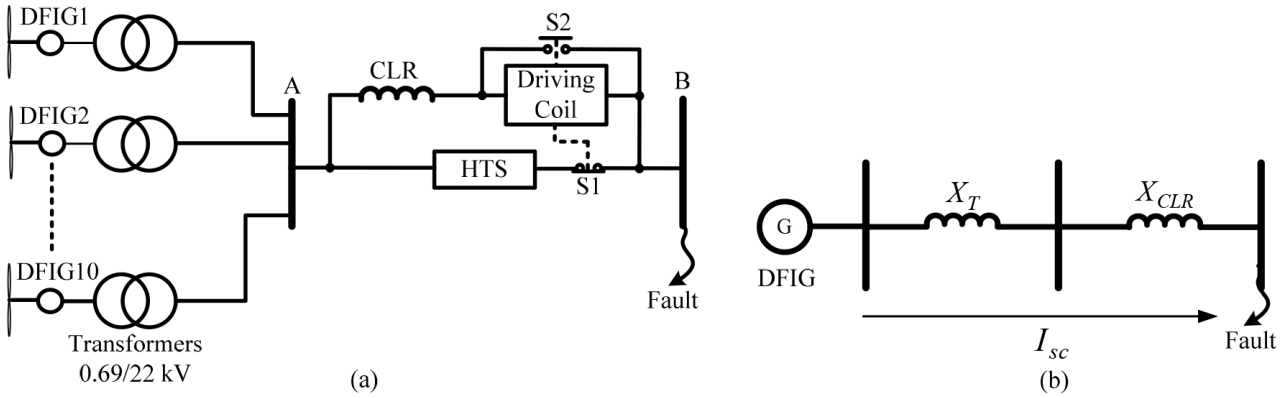

Figure 3. DFIG farm with SFCL: a) Single line diagram; b) Equivalent circuit.

3.2. Calculating the total short-circuit MVA

First, the short-circuit MVAs of the DFIG wind turbines, transformers, and CLR are expressed by the following equations:

$$S_{sc\_DFIG} = \sum_{i=1}^{n} \kappa\sqrt{3} V_l I_i \tag{5}$$

$$S_{sc\_T} = \sum_{i=1}^{n} \frac{S_{Ti}}{X_{Ti}} \tag{6}$$

$$S_{sc\_CLR} = \frac{V_L^2}{X_{CLR}} \tag{7}$$

The total short-circuit MVA in the case of a fault is described by

$$S_{sc\_total} = \frac{\left(\sum_{i=1}^{n} \kappa\sqrt{3} V_l I_i\right)\left(\sum_{i=1}^{n} \frac{S_{Ti}}{X_{Ti}}\right)\frac{V_L^2}{X_{CLR}}}{\left(\sum_{i=1}^{n} \kappa\sqrt{3} V_l I_i + \sum_{i=1}^{n} \frac{S_{Ti}}{X_{Ti}} + \frac{V_L^2}{X_{CLR}}\right)}, \tag{8}$$

where S_{sc_DFIG}, S_{sc_T}, and S_{sc_CLR} are the short-circuit MVAs of the DFIG wind turbines, transformers, and CLR, respectively. κ is the ratio of the lock rotor current to the rated current of the DFIG (pu). X_{Ti} and X_{CLR} are the ith transformer (pu) and CLR reactances (Ω), respectively. By substituting Eqs. (5)–(7) in Eq. (8), the short-circuit current can be calculated as described in Eq. (9).

$$I_{SC} = \frac{\left(\sum_{i=1}^{n} \kappa\sqrt{3} V_{Li} I_i\right)\left(\sum_{i=1}^{n} \frac{S_{Ti}}{X_{Ti}}\right)\frac{V_L^2}{X_{CLR}}}{\sqrt{3} V_L \left(\sum_{i=1}^{n} \kappa\sqrt{3} V_{Li} I_i + \sum_{i=1}^{n} \frac{S_{Ti}}{X_{Ti}} + \frac{V_L^2}{X_{CLR}}\right)} \tag{9}$$

In Eq. (9), the relation between the short-circuit current and the CLR reactance is described, which will be utilized in the next step.

3.3. Calculating the short-circuit current from the during-fault voltage of the grid code requirement

To calculate the CLR reactance, the minimum voltage grid code requirement (U_{DFIG}) must be considered as the input. Therefore, the during-fault voltage in terms of the CLR reactance, which is a summation of the during-fault transformer and CLR voltages (U_T and U_{CLR}), can be expressed as

$$U_{DFIG} = U_T + U_{CLR} \tag{10}$$

$$U_{DFIG} = \left(\frac{I_{SC}}{I_b}\right)\left(\frac{X_T + X_{CLR}}{X_b}\right) \tag{11}$$

Hence, from Eq. (10), the equation of the short-circuit current can be obtained using the following formula, where the subscript b represents the base quantity.

$$I_{SC} = I_b \frac{U_{DFIG}}{\left(\frac{X_T + X_{CLR}}{X_b}\right)} \tag{12}$$

By substituting Eq. (9) in Eq. (12), the CLR reactance can be computed successfully by defining a desired during-fault voltage of the grid code requirement. For example, in the previous section, the minimum satisfying voltage of the Irish grid was 0.15 pu with fault incidence. For this reason, the voltage has to be designed to be greater than this value by assuming $U_{DFIG} = 0.16\ pu$, and then the calculated CLR reactance will be 0.4 Ω. In the next section, the proposed method will be demonstrated and compared to the simulation results.

4. Results and discussion

To evaluate the proposed CLR calculation, the results of the proposed calculation are correlated with the simulation results. In this section, the study cases are divided into two parts—HTS material selection and the proposed method for determining the CLR reactance. First, the baseline scenario will provide the simulation results of a conventional SFCL configuration to examine the characteristics, including the first peak fault current reduction and the recovery time, for selecting the HTS material to be utilized in the hybrid case. Second, the hybrid case will demonstrate the proposed method for finding the CLR reactance and apply it to the EMT dynamic simulation of Figure 3a using the DIgSILENT PowerFactory software. A symmetrical three-phase fault with 100 ms fault duration is assumed to occur at bus B. The model of the HTS is implemented in this software to investigate the original characteristics of the HTS. Table 2 shows the SFCL parameters for the conventional and hybrid SFCLs.

4.1. HTS material selection for use in the hybrid SFCL

In this section, the selection of the HTS material for use in the hybrid SFCL configuration, which will be used in the case study, is presented. This scenario demonstrates the characteristics of the various composite HTS materials, namely, Bi-2212, YBCO, Bi-2223, Ti-2223, and Hg-1223, in the conventional SFCL, to investigate the peak fault current curtailment performance and recovery time. The HTS materials have different critical temperatures, as demonstrated in Table 3. Figure 4 illustrates a fault current at the 22 kV side of the DFIG with Bi-2212-, YBCO-, Bi-2223-, Ti-2223-, and Hg-2223-based conventional SFCLs and without the SFCL. With the various HTS materials, the first peak fault current reduction is diverse. Without the SFCL, the first peak current is 7.44 kA. The best first peak current reduction is for the Bi-2212-based SFCL, which can curtail

Table 2. SFCL parameters.

Nomenclature	Description	Value
T_s	Starting temperature of LN_2	77 K
L_{sc}	Superconductor length	50 m
d_{sc}	Superconductor diameter	0.004 m
J_c	Critical current density	1.5×10^7 A/m^2
δ	Flux flow region exponent	3
η	Flux creep region exponent	6
E_0	Electric field at transition state	0.1 V/m
E_c	Critical electric field	1.0×10^{-4} V/m
ρ	Resistivity in normal state	1.0×10^{-6} Ω.m

the peak current to 3.52 kA. Nevertheless, in a practical situation, the HTS material is not selected based on the first peak current curtailment performance alone; the recovery time of the HTS is also considered. In this typical SFCL case, the fault current flows into the HTS, which constantly receives the voltage stress. The characteristics of the HTS material, including the coil resistance and temperature, are presented in Figure 5. From the simulation results in Figure 5a, the highest HTS coil resistance is the Bi-2212-based SFCL because it has the lowest critical temperature in comparison with the other materials. Therefore, the Bi-2212 first changes its state to the resistive state. Figure 5b illustrates the HTS materials' temperatures in the case of fault occurrence. The results reveal that the maximum HTS temperature during the disturbance is for the Hg-1223-based SFCL. Nevertheless, the recovery time of Hg-1223 is lower than that of the others because it has the highest critical temperature. In this paper, for $I_{sc} < 4.5\ kA$ (40% of fault reduction) and recovery time lower than 2.5 s, the Bi-2223 will be considered for use as the hybrid SFCL in the next case study.

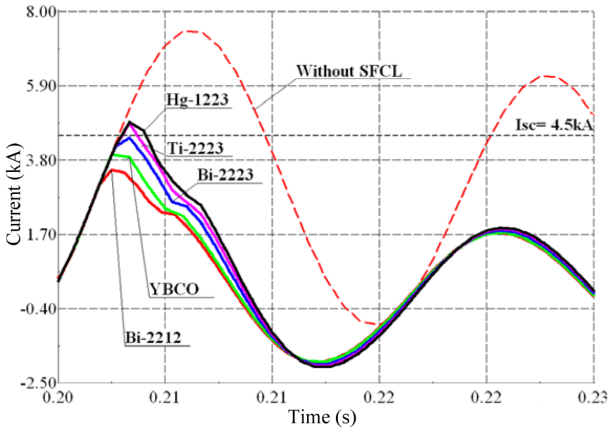

Figure 4. Current at 22 kV side with HTS materials for the conventional SFCL.

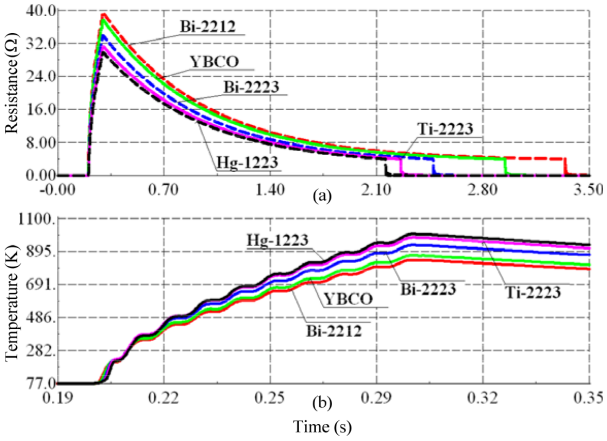

Figure 5. HTS characteristics of conventional SFCL: a) Resistance; b) Temperature.

4.2. Proposed CLR reactance calculation and simulation results comparison

In the previous case, the Bi-2223 was used in the hybrid SFCL configuration. In the case of fault occurrence, the hybrid SFCL will rapidly switch from the HTS to the CLR, limiting the fault current. Figure 6 shows the short-circuit current at the 22 kV side for different CLR reactances. The HTS materials quickly diminish the first peak of fault current with the same value as the conventional SFCL. After the first peak current, the CLR starts

Table 3. HTS critical temperatures.

Notation	Formula	T_c (K)
Bi-2212	$Bi_2Sr_2CaCu_2O_8$	85
YBCO	$YBa_2Cu_3O_7$	92
Bi-2223	$Bi_2Sr_2Ca_2Cu_3O_{10}$	110
Ti-2223	$Ti_2Ba_2Ca_2Cu_3O_{10}$	125
Hg-1223	$HgBa_2Ca_2Cu_3O_8$	134

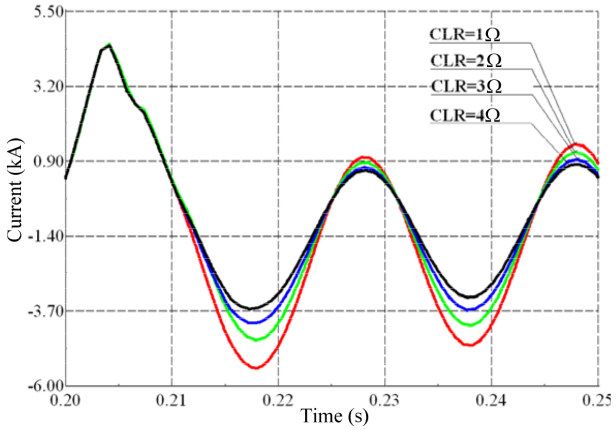

Figure 6. Side current at 22kV for various CLR reactances (Bi-2223-based hybrid SFCL).

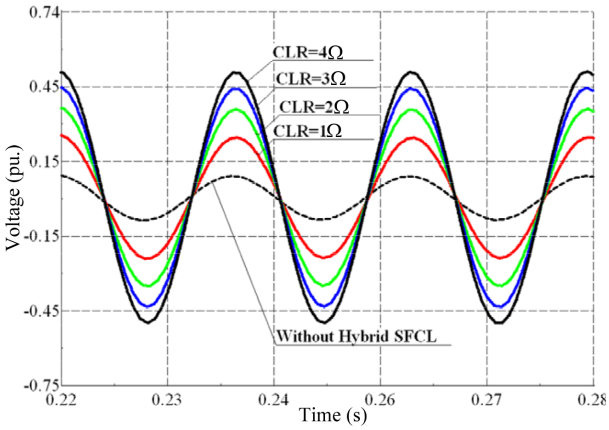

Figure 7. Fault voltage of the DFIG for various CLR reactances.

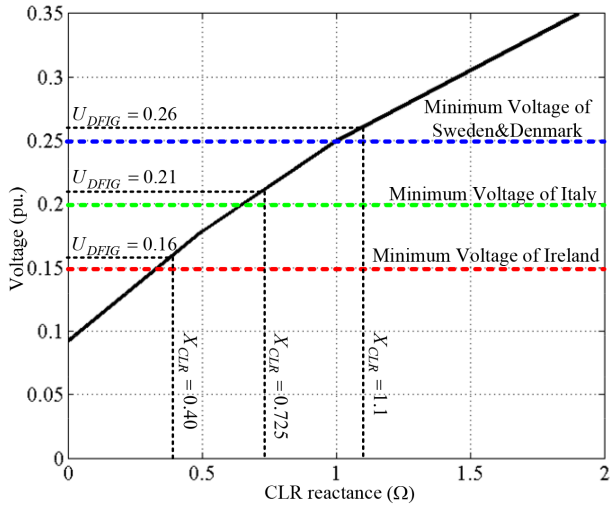

Figure 8. During-fault-voltage–CLR reactance relation of the proposed method.

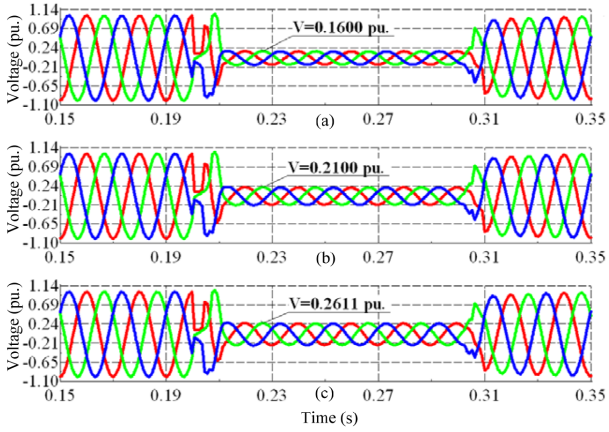

Figure 9. Simulation results of DFIG terminal voltage testing with a) X_{CLR} = 0.40 Ω; b) X_{CLR} = 0.725 Ω; and c) X_{CLR} = 1.1 Ω.

operating. On increasing the CLR reactance, the during-fault current can be reduced. The during-fault voltage of the DFIG is plotted in Figure 7 for various CLR reactances. According to the results with the hybrid SFCL, the voltage can be increased by adjusting the CLR reactance. Without the Bi-2223-based hybrid SFCL, during the fault incidence, the voltage drops down to 0.088 pu, which is less than the values stipulated by the Irish, Italian, Danish, and Swedish grid code requirements. Therefore, without the hybrid SFCL, the DFIG cannot

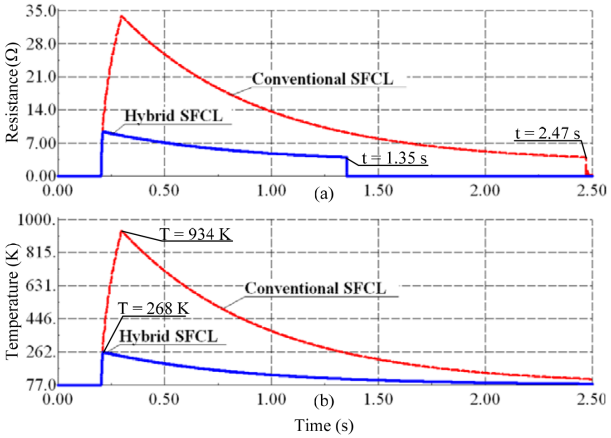

Figure 10. Hybrid and conventional SFCL behaviors.

ride through the fault, according to the grid code. On the other hand, with the hybrid SFCL, a suitable CLR reactance that can meet the voltage requirement of the code using the proposed CLR reactance calculation must be determined for reducing the cost of the hybrid SFCL in practice. In Section 4, the proposed CLR calculation in the hybrid SFCL was demonstrated. When $V_L = 22$ kV, $\kappa = 5.045$ pu, $X_T = 0.02$ pu, and $S_T = 22.22$ MVA, in addition to determining the CLR reactance, the desired during-fault voltage of the DFIG has to be substituted in Eq. (12). Thus, two equations with two parameters of the short-circuit current for CLR reactance will be obtained. To compute the CLR reactance satisfying the Irish grid code requirement with 0.15 pu of minimum acceptable voltage, the assumed parameters and $U_{DFIG} = 0.16$ pu can be substituted in Eq. (12) and then Eqs. (9) and (12) can be solved. Hence, the CLR reactance for satisfying the Irish grid code is 0.4 Ω. The CLR reactance for the Italian grid code is 0.725 Ω for a desired voltage $U_{DFIG} = 0.21$ pu. For the Swedish and Danish grid code requirements, for a desired during-fault voltage of the DFIG ($U_{DFIG} = 0.26$ pu), the CLR reactance is 1.1 Ω. The relation between the voltage and CLR reactance is demonstrated in Figure 8, where the minimum voltages of Sweden and Denmark, Italy, and Ireland are illustrated by the constant blue, green, and red dotted lines, respectively. For this reason, the appropriate CLR reactance can also be determined by using this relation for improving the fault ride-through of the DFIG satisfying the requirements. The calculated CLR reactance is also compared to the dynamic simulation results as shown in Figure 9. When the starting and clearing fault times are 0.2 and 0.3 s, respectively, the dynamic voltage of the DFIG is ready to be compared with the calculated results. The CLR reactance is assumed to be 0.4 Ω in DIgSILENT PowerFactory software, obtaining the results in Figure 9a. With fault incidence for CLR = 0.4 Ω, the voltage suddenly decreases to 0.16 pu. Therefore, from the comparison of the proposed method and the simulation results of testing the short circuit for Irish, Italian, Swedish, and Danish grid codes, the proposed method of calculating the CLR reactance for the fault ride-through capability of the DFIG, satisfies the grid code requirement and is usable. On the other hand, the main difference between the conventional and hybrid SFCL configurations is the recovery time of the superconductor. Figure 10 demonstrates the HTS resistance and temperature in Figures 10a and 10b, respectively. With the hybrid SFCL, the HTS immediately quenches, and the fault current will flow through the driving coil. The HTS receives the fault current in the first peak of the cycle only. As shown in the results, the hybrid SFCL can recover to the superconducting state within 1.35 s, in comparison with the conventional SFCL that recovers at 2.47 s (over 45% reduction in recovery time). Therefore, the recovery time of the HTS of the hybrid SFCL is less than that of the conventional SFCL. In this case, the maximum temperature of the HTS is suddenly decreased in the hybrid case as shown in Figure 10b. In the conventional case, the maximum

temperature of the HTS coil is 934 K, which is greater than that of the hybrid configuration by approximately 3.5 times.

5. Conclusions

This paper demonstrated a method for calculating the appropriate CLR reactance during the design of a hybrid SFCL for improving the low voltage ride-through capability of DFIG wind farms, which fulfilled the grid code requirement targets. HTS materials, such as Bi-2212, YBCO, Bi-2223, Ti-2223, and Hg-1223, were investigated for evaluating their first peak current reduction performances, and a suitable material was selected for use in the hybrid SFCL configuration. From the simulation results of the base case, Bi-2223 was selected for use in the hybrid SFCL case study. The proposed method required only one parameter, which was the desired during-fault voltage or the minimum satisfying voltage, obtained from the grid code requirement. The calculated CLR reactance was applied to the DFIG wind farm, and was compared with the simulated results, for each case. The proposed method was able to compute a CLR reactance that satisfied the grid code requirement, allowing the DFIG wind farm to ride through the fault. Hence, an appropriate and practical CLR reactance could be obtained using the proposed method, and the installation cost of the hybrid SFCL for improving the low voltage ride-through capability of the DFIG was apparently reduced. Moreover, the recovery time of the hybrid SFCL was less than that of the conventional SFCL, protecting the HTS coil life. In future works, the effects of the CLR reactance with a bus voltage will be investigated to evaluate the hybrid SFCL performance for improving the fault ride-through capability of large power systems and other renewable energy sources on a microgrid. In the protection aspect, the breaker reclosing times for hybrid SFCLs will be necessary to investigate the operations in the fault ride-through improvement. Therefore, a study of the fault ride-through capability and transient stability of the DFIG wind farm using a relay coordinate operation with the hybrid SFCL will be revealed shortly.

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