

Low-power voltage to a frequency-based smart temperature sensor with $+0.8/-0.75$ °C accuracy for -55 °C to 125 °C

Mudasir BASHIR*, Sreehari Rao PATRI, Krishna PRASAD

Department of Electronics and Communication Engineering, National Institute of Technology, Warangal, Telengana, India

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Abstract: The high power densities in system-on-chips demand accurate, low power, and compact smart temperatures for thermal monitoring. In this paper, a low-power CMOS-based smart temperature sensor, operating in the subthreshold region, for military applications (-55 °C to 125 °C) is presented. The sensor exploits the thermal dependency of the threshold voltage of MOS transistors to generate a voltage proportional to absolute temperature (V_{PTAT}). A frequency locked loop technique is employed to generate frequency from V_{PTAT} . The frequency variation due to temperature is measured by counting the rising edge with an asynchronous 12-bit counter. The large die area and requirement of external voltage regulator and reference clock hinder the integration of the on-chip sensors in SoCs. Therefore, a compact smart temperature is introduced with embedded temperature insensitive reference signal generators. The sensor is designed in CMOS 65 nm standard process and its operation is validated through postlayout results, considering a worst-case scenario. The sensor consumes power and area of 8.8 μ W and 0.009 mm², respectively, at a power supply of 0.5 – 1 V. After one-point calibration, the sensor has an accuracy of $+0.8/-0.75$ °C and a resolution of 0.26 °C for -55 °C to 125 °C. The sensor consumes energy of 4.8 nJ and has a figure of merit of 0.12 nJK².

Key words: Smart temperature sensor, low power, frequency locked loop, temperature insensitive ring oscillator, switched capacitors, calibration

1. Introduction

Integration of smart temperature sensors with radio frequency identification (RFID) has extended their range of applications, like in monitoring of food, in implantable medical devices, and for measuring environmental temperature [1]. Due to the challenges imposed by CMOS scaling and ubiquitous computing, the temperature sensors in RFID tags should be energy efficient while consuming less die area and power. The trend of application specific temperature sensors with dedicated signal conditioning interfaces has relaxed the constraint on the sensor performances. Besides a power consumption of a few microwatts and energy consumption of a few nanojoules per conversion, the sensor should have high resolution and simple calibration circuitry.

The typical accuracy for RFID temperature sensors varies from ± 0.1 °C for medical applications [2] to ± 1 °C for environmental and food monitoring applications [3]. However, with the process spread this accuracy can be achieved only after using different calibration and trimming techniques. Smart temperature sensors are calibrated by establishing a relation between the quantity values and the measurement uncertainties. Some common calibration techniques are laser trimming, batch calibration, binning, voltage and current calibration

*Correspondence: mudasir.mir7@gmail.com

etc., which explore the concept of traceability, correction, and adjustment [4]. Various temperature sensors have been introduced in CMOS technologies. A typical sensor compares a temperature dependent voltage with temperature insensitive voltage. These two voltages are generated by exploiting the complementary-to-absolute-temperature (CTAT) and proportional-to-absolute-temperature (PTAT) characteristics of a circuit. Then the reference and PTAT voltages are given to an analogue-to-digital converter (ADC) for digital output [4]. A high resolution of up to 0.002 °C can be achieved by employing complicated sigma-delta ($\Sigma\Delta$) ADC topologies [5]. However, for such a resolution with an accuracy of ± 0.25 °C from -70 °C to 130 °C, a sophisticated calibration technique is employed resulting in circuit complexity, increased cost, area, and power consumption [5]. To overcome these issues, frequency/time-to digital converters (FDC/TDC)-based smart temperature sensors have been introduced [6]. A dual delay locked loop-based temperature sensor is proposed in [7]. These sensors exploit the thermal dependency of the delay of digital gates. However, these sensors require hundreds of delay elements to achieve a target resolution [7]. This results in tradeoff between the resolution and the conversion rate of the sensor. The delay lines are sensitive to power supply variations affecting the overall accuracy of the sensor. A look-up table-based logarithmic counter is employed in [8], which results in large die area and inaccuracy. The TDC-based smart temperature sensors require two-point calibration and therefore require complex linearization techniques to achieve better accuracy. A temperature to frequency-based sensor is introduced in [9]. The sensor requires off-chip reference signals and a control amplifier, resulting in stability issues and complex chip integration. Moreover, the startup circuit is not employed, making the sensor slow. The TDC-based temperature sensors are more sensitive to noise. The estimation of noise contribution to the sensor can be modelled using the technique introduced in [10]. BJT-based temperature sensors [5,11] are quite accurate and require only one-point calibration to achieve an accuracy of $\leq \pm 0.2$ °C, but their compatibility issues with the CMOS process make them costly. Moreover, these sensors are not energy efficient as they dissipate energy of hundreds of nanojoules per conversion. Lately, MOSFETs are used to realize temperature sensors [12–17]. They generally exploit the thermal dependency of threshold voltage (V_{TH}) or leakage current of MOS transistors. Due to the spread in channel doping and gate-oxide thickness of MOSFETs, these sensors usually require multipoint calibration to achieve an accuracy of $\leq \pm 1$ °C. The relation of the V_{TH} of a MOS transistor on temperature is given by Eq. (1) [18].

$$V_{TH}(T) = V_{TH0} + \left(K_{T1} + \frac{K_{T1}L}{L_{eff}} + K_{T2} \cdot V_{BSeff} \right) \left(\frac{T}{T_{nom}} - 1 \right) \quad (1)$$

$$\text{and } \frac{\Delta V_{TH}}{\Delta T} \approx -1.8mV/K, \quad (2)$$

where V_{TH0} is the threshold voltage at temperature ($T_{nom} = 300$ K); K_{T1} , L , and K_{T2} are constants; L_{eff} is the effective length; and V_{BSeff} is the effective bulk to source voltage.

In this paper, a low-power and low-cost, energy-efficient CMOS-based smart temperature sensor for military applications (-55 °C to 125 °C) is presented. This work extends the temperature sensor configuration presented in our previous work [14]. The main contributions of this paper are as follows: on-chip temperature insensitive clock and voltage generator, startup circuitry, time-to-digital converter (TDC), and on-chip calibration technique. The sensor is designed in 65 nm CMOS process and its operation is validated through postlayout simulation results in the worst-case scenario. After one-point calibration, the sensor achieves an accuracy of $+0.8/-0.75$ °C and a resolution of 0.26 °C for a temperature range of -55 °C to 125 °C, while consuming area and power of 0.009 mm² and 8.8 μ W, respectively.

The rest of the paper is organized as follows: section 2 explains the structure and working principle of the proposed temperature sensor. In section 3, a detailed description of subblocks of the sensor and the calibration technique used is given. The post-layout simulation results, considering the worst case, are discussed in section 4, followed by the conclusion in section 5.

2. Structure and working principle

Figure 1 shows the functional block diagram of the proposed temperature sensor. The sensor consists of on-chip temperature insensitive voltage and frequency generator used as reference signals, a PTAT current generator with start-up circuitry, a subtractor with an integrator, voltage controlled oscillator (VCO), frequency-to-current converter, calibration circuitry, and an asynchronous TDC. The sensor employs a frequency loop technique through the subtractor, integrator, VCO, and frequency-to-current converter to generate the desired PTAT frequency. The difference of the PTAT current (I_{PTAT}) obtained from the PTAT current generator and the output current (I_{OUT}) from the frequency-to-current converter at the subtractor output is given to the integrator for obtaining the corresponding voltage (V_{OUT}). The V_{OUT} controls the frequency of the VCO, giving a PTAT frequency (F_{PTAT}). The F_{PTAT} is fed back to the subtractor as I_{OUT} using the frequency-to-current converter and every time the V_{OUT} keeps changing, resulting in variation in F_{PTAT} based on the ambient temperature variations. The F_{PTAT} is also given to an asynchronous TDC for digital output. An enable switch, controlled by a slow clock, is introduced to mitigate the idle power consumption and to reset the output counter value after predefined cycles. The calibration circuitry is realized by switch controlled current sources, where the switches are controlled by dynamic element matching.

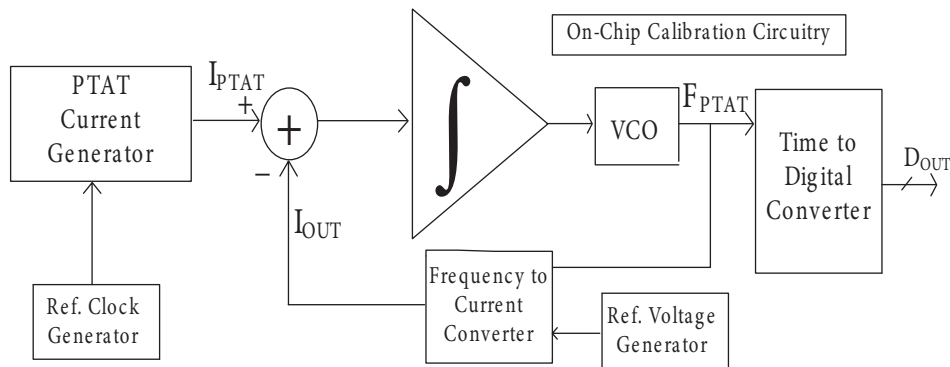


Figure 1. Block diagram of proposed temperature sensor.

3. Circuit-level implementation

3.1. PTAT current generator

A MOS transistor operates in the subthreshold region, when the gate-to-source voltage (V_{GS}) is smaller than the threshold voltage (V_{TH}) and drain-to-source voltage (V_{DS}) is greater than V_{TH} by several hundred millivolts. The drain current ($I_{D,Sub}$) equation for subthreshold region can be simply given as [18]

$$I_{D,Sub} = k \cdot I_{DO} \cdot e^{V_{GS}/nV_t}, \tag{3}$$

where k is the aspect ratio of MOS transistors, I_{DO} and n are the process dependent parameters, V_t is the thermal voltage given by $V_t = KT/q$ and is PTAT, q is the electronic charge (1.6×10^{-19} Coulomb), T is the temperature, and K is the Boltzmann’s constant (1.38×10^{-23} JK⁻¹).

The V_{GS} can be expressed from Eq. (3) as

$$V_{GS} = nV_t \cdot \ln \left(\frac{I_{D,Sub}}{I_{DO}(W/L)} \right) \quad (4)$$

The PTAT current generator is shown in Figure 2 [14], where the resistance is replaced by a switched capacitor (SC). The switches of the SC are controlled by the nonoverlapping clock signals ($F_{REF}, \overline{F_{REF}}$) generated by an on-chip temperature insensitive reference frequency generator. The transistors M_1 and M_2 , M_3 , and M_4 are of the same size to mitigate the mismatch effects. The difference between the gate to source voltage of M_5 and M_6 is given as

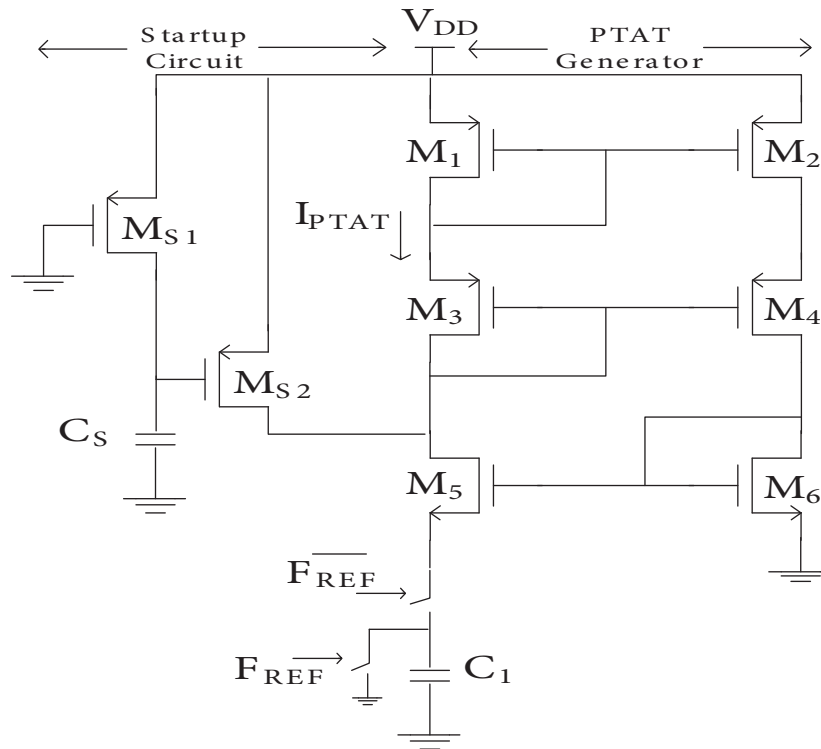


Figure 2. PTAT current generator.

$$V_{GS6} - V_{GS5} = I_{PTAT} \cdot R \quad (5)$$

where R is the resistance of SC given by

$$R = 1/C_1 F_{REF} \quad (6)$$

$$\text{and } V_{GS6} = nV_t \ln \left(\frac{I_{3,4}}{I_{DO}k_6} \right) \quad (7)$$

$$V_{GS5} = nV_t \ln \left(\frac{I_{3,4}}{I_{DO}k_5} \right) \quad (8)$$

Substituting values of R , V_{GS6} , and V_{GS5} , from Eqs. (6), (7), and (8) in Eq. (5) and solving, we get

$$I_{PTAT} = \frac{nKT}{q} \cdot C_1 F_{REF} \cdot \ln\left(\frac{k_5}{k_6}\right) \tag{9}$$

or

$$I_{PTAT} \propto T \tag{10}$$

Therefore, I_{PTAT} is directly proportional to absolute temperature. For better matching and mismatch cancellation, finger layout for large transistors and dummy devices is used.

3.2. Temperature insensitive reference signals

The temperature insensitive ring oscillator (TIRO) adapted from [19] is used for generating reference frequency signals. It consists of nine stages, where each stage is composed of a bootstrap circuit and a driver. The schematic of the TIRO is shown in Figure 3. The transistors M_{P2} and M_{N2} are used as switches controlled by the input signal (V_{IN}). The capacitors C_{BP} and C_{BN} behave as bootstrap circuits and are precharged by transistors M_{P1} and M_{N1} , respectively. The inverters (INV_N and INV_P) are used as drivers. The bootstrapped inverter gives an output swing of $-\beta V_{DD}$ to $2\beta V_{DD}$, where β is the boosting efficiency and V_{DD} is the power supply. Besides the advantages highlighted in [16], this bootstrapped ring oscillator (BTRO) can be used as TIRO, if designed carefully. At a power supply approximately equal to the threshold voltage of MOS transistors (~ 0.5 V), the BTRO operates in the subthreshold or linear region during the turned-on transient. Therefore, for one period of oscillation, the BTRO has two operating behaviors during the tuned-on transient operation. The period of BTRO remains invariant with temperature due to the opposite temperature behavior during the tuned-on transients. The total delay (τ_{total}) of a single stage TIRO is given as

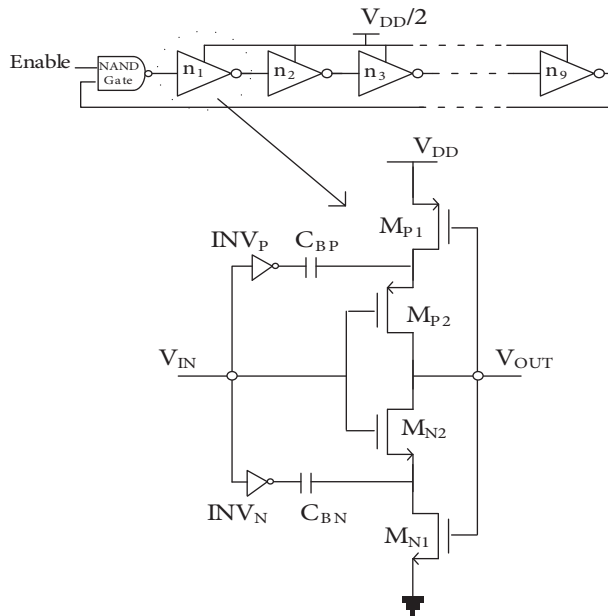


Figure 3. 9-Stage TIRO [19].

$$\tau_{total} = \tau_{lin} + \tau_{sub} \tag{11}$$

where τ_{lin} and τ_{sub} are the delay in the linear and subthreshold region, respectively. Considering the current flowing in both the linear and subthreshold region to be equal, the driving capability of both nMOS and pMOS transistors is the same. Then the τ_{total} is given as

$$\tau_{total} = \frac{k_f \cdot C_L \cdot (V_{DD} - V_o)}{\mu \cdot C_{dep} \cdot W/L \cdot V_T^2 \cdot \exp\left(\frac{V_{DD} - V_{TH}}{nV_T}\right)} + \frac{C_L (V_o - V_{50\%})}{\mu \cdot C_{ox} \cdot W/L \cdot (\beta 2V_{DD} - V_{TH})} \quad (12)$$

where C_{dep} and C_{ox} are the depletion and oxide capacitors, μ is the effective mobility, W/L is the aspect ratio of the transistors, and k_f is the fitting parameter.

The temperature insensitive voltage reference (TIVR) is adopted from [20], where the TIVR is realized in 0.35 μm CMOS process operating at a power supply of 1.4–3 V. The TIVR, in this work, generates a reference voltage of 550 mV at a power supply of 1 V. The circuit, shown in Figure 4, generates a negative and positive temperature coefficient (TC), which are combined to give a constant voltage with a zero TC. The current mirror (M_8 – M_9) and differential amplifier (M_1 – M_5) are employed to reduce the line sensitivity of the circuit by increasing the power supply rejection ratio (PSRR). To avoid the noise disturbances and parasitic oscillations, capacitors C_{C1} , C_{C2} , and C_{C3} are used. The stable state of TIVR in the zero bias condition is presented by using a start-up circuit (M_{12} – M_{16}). All the transistors are operated in the subthreshold region for low power consumption except M_{R1} .

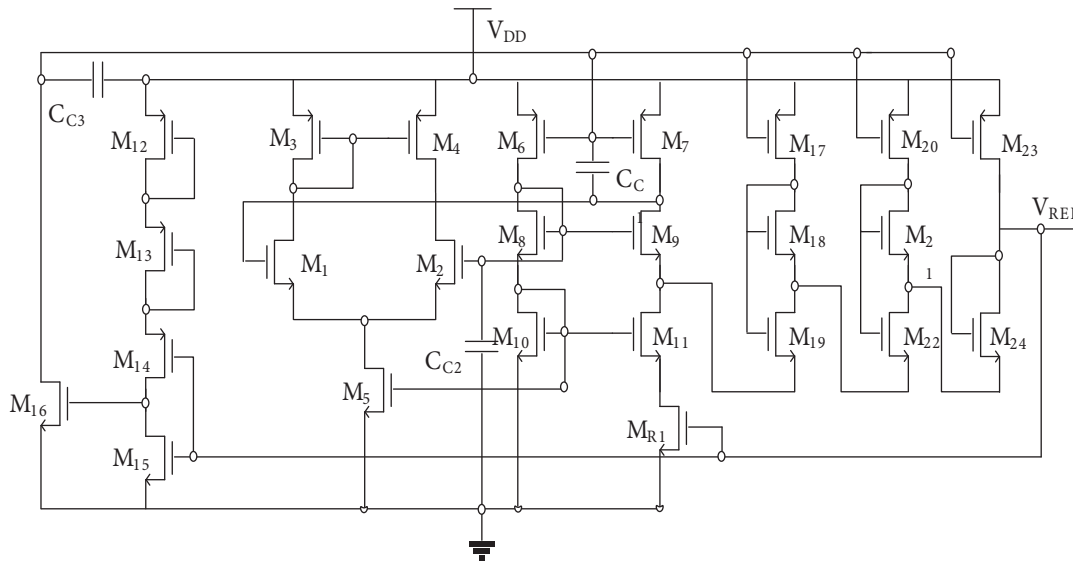


Figure 4. TIVR [20].

3.3. Counter

The frequency signals generated from the temperature sensor and the TIRO are converted into digital output through the asynchronous counter. The size of the counter is chosen so that it does not overflow the count value, mostly at high temperatures. Although more bits can be added to the counter, it increases the static power and will also impact the dynamic power, as the most significant bit (MSB) switching activity is small. A 12-bit asynchronous counter is realized using JK flip-flops, AND gates, and buffers, as shown in Figure 5.

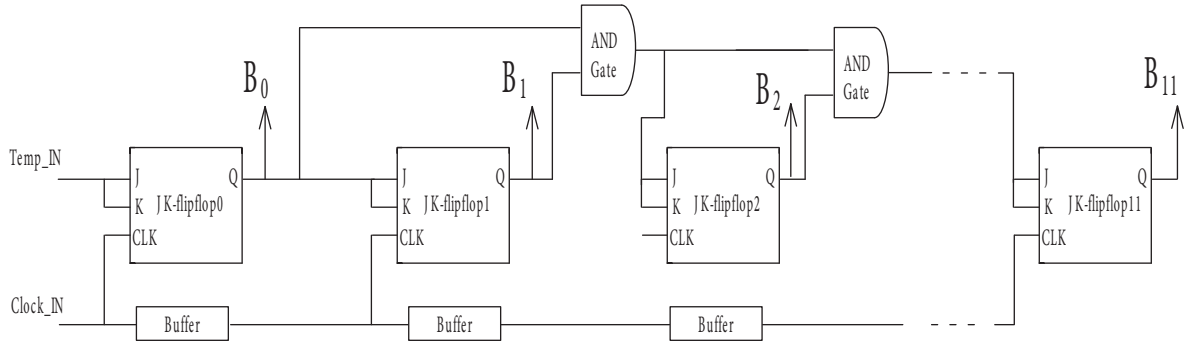


Figure 5. 12-bit asynchronous counter.

3.4. Frequency to current conversion

The frequency to current converter is used at the output of VCO to get the I_{OUT} from F_{PTAT} . The I_{OUT} is given by

$$I_{OUT} = C_2 F_{PTAT} V_{REF} \quad (13)$$

A simple current mirror is used to mirror the I_{OUT} into the subtractor. At the initial stage, the I_{OUT} is made equal to I_{PTAT} . Therefore, the F_{PTAT} can be expressed as

$$F_{PTAT} = \frac{C_1 F_{REF} nKT}{C_2 V_{REF} q} \ln \left(\frac{k_5}{k_6} \right) \quad (14)$$

or

$$F_{PTAT} \propto T, \quad (15)$$

where k_5 and k_6 are the aspect ratios of the transistors M_5 and M_6 , respectively and F_{REF} and V_{REF} are the temperature insensitive reference frequency and voltage sources.

4. Current subtractor, integrator, and voltage-to-frequency converter

The currents I_{PTAT} and I_{OUT} are given to a subtractor followed by an integrator. A voltage (V_{OUT}) proportional to the difference between I_{OUT} and I_{PTAT} is obtained at the integrator output. Transistor M_{12} , shown in Figure 6, mitigates the leakage current at higher temperature.

The voltage-to-frequency converter (VFC) or VCO is realized using three stages of the current starved ring oscillator, operating in the subthreshold region [14]. Two cascaded inverters are used at the output of the VCO to generate the nonoverlapping clock signals of F_{PTAT} . The frequency of oscillation is controlled by the bias current (I_{bias}) defined by the V_{OUT} , which is given as

$$F_{PTAT} = \frac{I_{bias}}{2nAC_L V_{DD}} \quad (16)$$

where I_{bias} is the current flowing through each stage, n is the number of stages, C_L is the load capacitance, and A is the delay fitting parameter.

4.1. Calibration technique

The variations due to the spread in gate-oxide and channel doping of MOS transistors affect the accuracy of the sensor. The process variation is mainly caused due to the V_{TH} mismatch in the I_{PTAT} generator ($\Delta V_{TH} = V_{TH6} - V_{TH5}$) and variation in switched capacitors (C_1 and C_2).

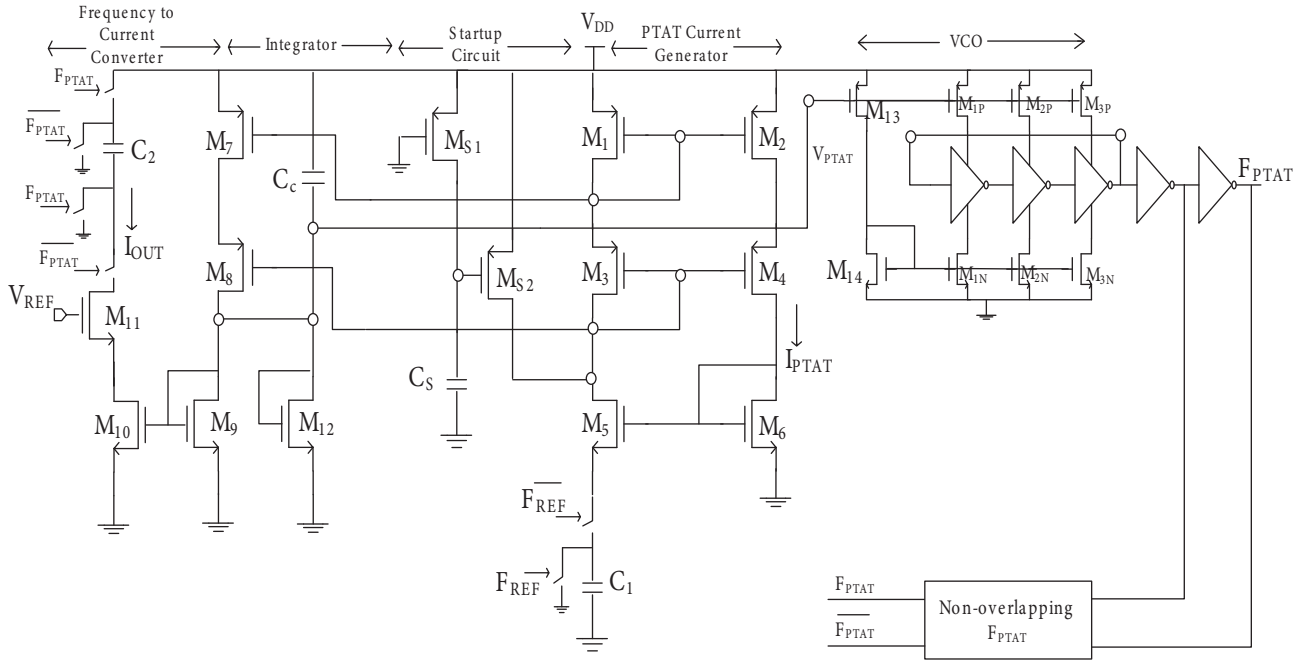


Figure 6. Entire circuit configuration of temperature sensor.

From Eq. (7), the variation in I_{PTAT} due to V_{TH} mismatch is given as

$$I_{PTAT_var} = \frac{nKT}{q} \cdot C_1 F_{REF} \cdot \ln\left(\frac{k_5}{k_6}\right) + C_1 F_{REF} \cdot \Delta V_{TH} \quad (17)$$

The additional term in the above equation defines the V_{TH} mismatches, resulting in the offsets. This can be negotiated by matching the transconductance of transistor M_5 with the conductance of SC. The variation in C_1 and ΔV_{TH} requires two-point calibration.

From Eq. (10), the variations due to process spread in F_{PTAT} are given as

$$F_{PTAT} = \frac{C_1 F_{REF} nKT}{C_2 V_{REF} q} \ln\left(\frac{k_5}{k_6}\right) + \frac{C_1 F_{REF} nKT}{C_2 V_{REF} q} \Delta V_{TH} \quad (18)$$

In the above equation, the additional terms C_1 and C_2 cancel each other's effects. F_{REF} , V_{REF} , and nKT/q are constants. Therefore, only ΔV_{TH} mismatch has to be calibrated, resulting in one-point calibration.

The increases in the inaccuracies due to process spread are reduced by trimming the sensor at 55 °C. The calibration technique employs conventional dynamic element matching (DEM) to achieve an accurate I_{PTAT} [5]. The I_{PTAT} is digitally adjusted by six current sources controlled by switches, realized using pMOS transistors operating in the triode region. Out of the six current sources, five are used to coarse trim I_{PTAT} and the sixth one is used to generate a bias current between 0 and I_{OUT} depending on the digital outputs.

5. Post-layout simulation results and discussions

The entire circuit configuration of the temperature sensor is shown in Figure 6. The operation of the proposed temperature sensor is validated through postlayout results, considering the worst case, for a temperature range of -55 °C to 125 °C and using a set of 65 nm CMOS standard process at a power supply of 0.5–1 V. The

layout of the proposed sensor is shown in Figure 7. The overall sensor consumes a power and area of $8.8 \mu\text{W}$ and 0.009 mm^2 , respectively. The variation in power consumption with temperature is shown in Figure 8.

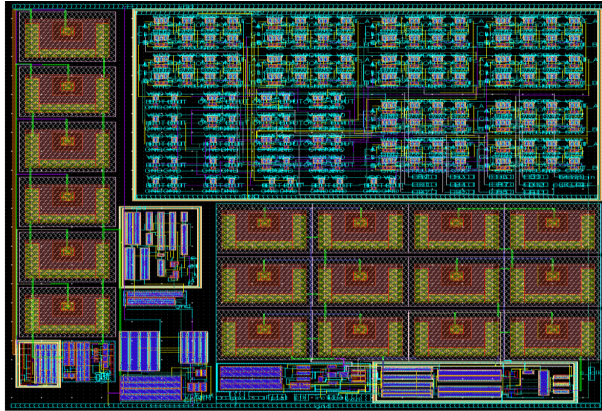


Figure 7. Layout of the temperature sensor.

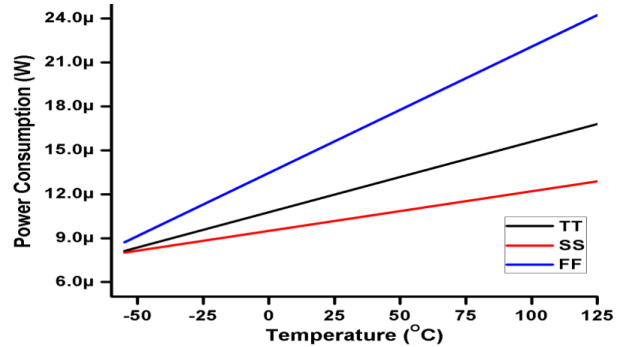


Figure 8. Variation in power consumption with temperature.

5.1. TIRO

The variation in the reference clock signal with temperature is shown in Figure 9. As can be seen, the TIRO has a frequency of 10 MHz at room temperature and varies within $\pm 0.12\%$ of the clock frequency over the desired temperature range.

5.2. TIVR

Figure 10 shows the reference voltage (V_{REF}) as a function of temperature from $-55 \text{ }^\circ\text{C}$ to $125 \text{ }^\circ\text{C}$, across all process corners. The average TC and power consumption of TIVR is $12 \text{ ppm}/^\circ\text{C}$ and 164 nW , respectively. V_{REF} shows the nonlinear dependency on temperature, which can be mitigated by employing curvature compensation techniques [20].

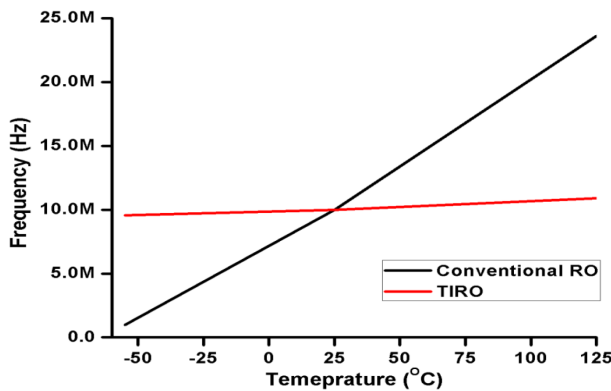


Figure 9. Variation in F_{REF} with temperature.

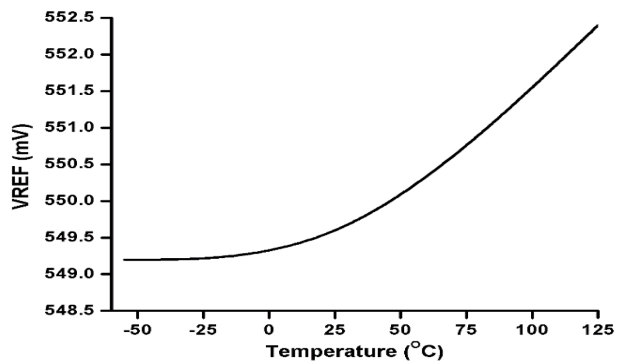


Figure 10. Variation in V_{REF} with temperature.

5.3. Temperature sensor

The variation in V_{PTAT} with temperature across process corners slow-slow (SS), fast-fast (FF), and typical-typical (TT) is shown in Figure 11. The V_{PTAT} varies almost linearly for a temperature range of $-55 \text{ }^\circ\text{C}$ to

+125 °C. The variation in F_{PTAT} with temperature across SS, FF, and TT corners is shown in Figure 12. The temperature sensor generates a frequency of 2.13 MHz and 18.25 MHz at -55 °C and +125 °C, respectively.

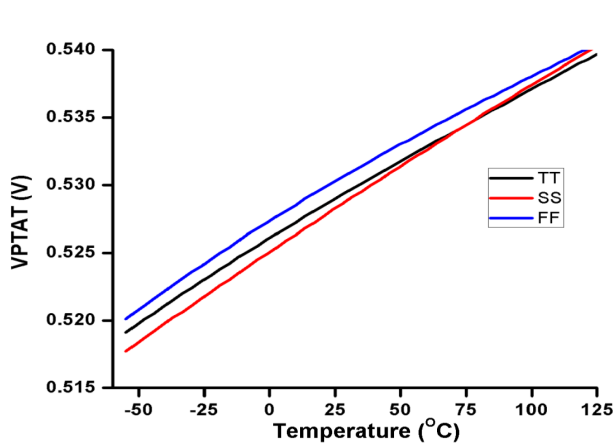


Figure 11. Variation in V_{PTAT} with temperature.

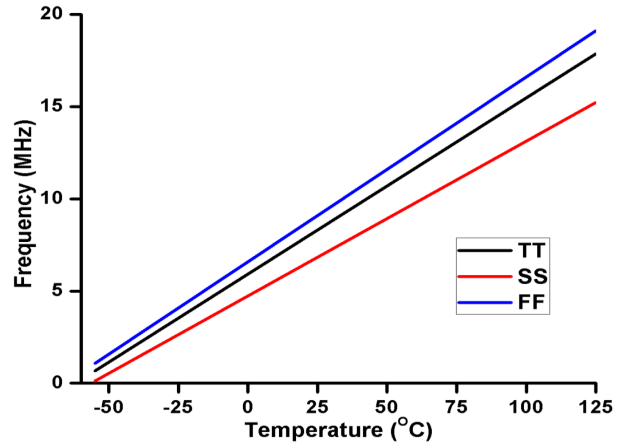


Figure 12. Variation in F_{PTAT} with temperature.

Figure 13 shows the digital output of corresponding temperature values for a temperature range of -55 °C to +125 °C, across SS, FF, and TT corners. Using linear fitting curve for a value of $R^2 = 0.99998$, the temperature value is translated from the counter digital value as

$$\text{Temperature} = 0.066 \times \text{count}_{\text{value}} - 395.3 \tag{19}$$

The effect of nonlinearities due to the temperature variation is defined by the accuracy of the temperature sensor. After one trim at 55 °C, the sensor achieves an accuracy of +0.8 °C/-0.75 °C across all process corners, as shown in Figure 14. The sensor has a resolution of 0.26 °C over the same temperature range. The sensor consumes energy of 4.8 nJ.

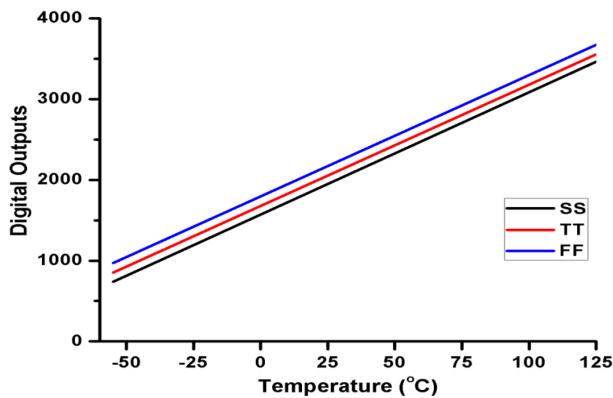


Figure 13. Digital output with temperature.

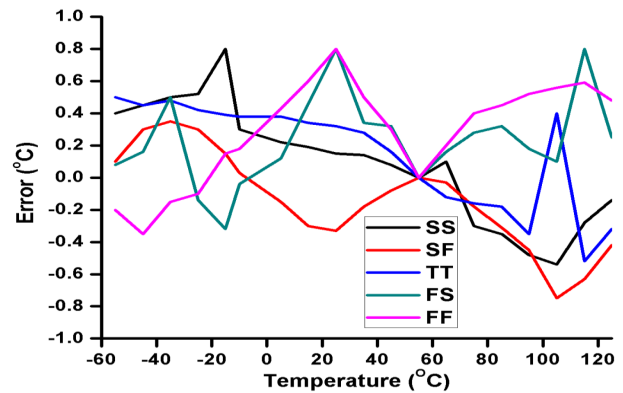


Figure 14. Accuracy of temperature sensor.

The TDCs are more sensitive to supply voltage variations than ADCs, thereby affecting the accuracy of sensors. In order to find the variation in error of the temperature sensor, supply voltage is varied at specific temperature (-40 °C, 25 °C, and 120 °C). The sensor error varies from +0.028 to -0.038 for ±10% of supply voltage, as shown in Figure 15.

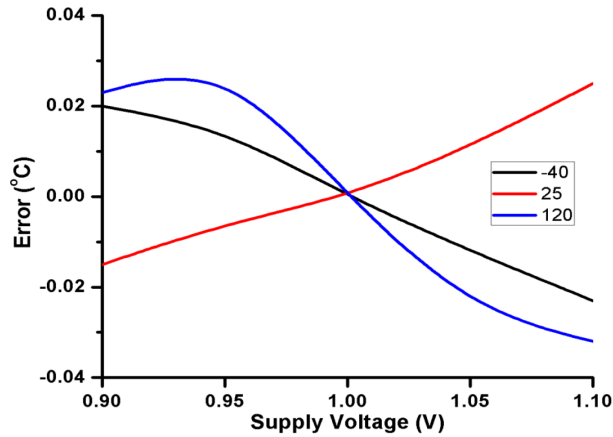


Figure 15. Error variations due to supply voltage.

5.4. Comparison with related works

The performance summary and comparison of the proposed temperature sensor with recent related sensors is given in the Table. The energy efficiency of the sensor can be benchmarked for calculating the resolution figure of merit (FoM) (F_R), defined as [4]

$$F_R = E \cdot s^2, \quad (20)$$

where E is the energy consumed and s is the resolution of the sensor. The sensor has a F_R of 0.12 nJK². A comparison with all CMOS-based smart temperature sensors is shown in Figure 16.

Table. Comparison with related works.

Parameter	This work	[12]	[13]	[16]	[17]
Year	2017	2013	2016	2017	2015
Technology (nm)	65	65	65	180	40
Type	CMOS	CMOS	CMOS	CMOS	CMOS
Supply (V)	0.5-1	1	1	1	0.5-1
Temperature range (°C)	-55 to 125	0 to 110	0 to 100	-20 to 120	-40 to 100
Resolution (°C)	0.26	0.18	0.3	0.048	0.02
Conversion time (μ s)	0.1	2.1	22	1	20
Calibration	1	1	2	2	2
Inaccuracy (°C)	+0.8/-0.75	\pm 1.5	\pm 0.9	\pm 2	+0.97/-0.95
Power consumption (μ W)	8.8	500	154	93.6	241
Area (mm ²)	0.009	0.008	0.0082	0.188	0.058
Energy (nJ)	4.8	1.1	3.4	93.6	0.004
R-FoM (nJK ²)	0.12	0.97	0.31	0.22	0.0016

6. Conclusion

A low-power smart temperature sensor has been designed in 65 nm CMOS standard process for a temperature range of -55 °C to 125 °C. The sensor employs a frequency locked loop technique to generate a frequency from voltage proportional to absolute temperature. The frequency is then given to an asynchronous 12-bit counter for digital output. An on-chip temperature insensitive clock and voltage references are developed to generate the references signals. After one-point calibration, the sensor results in an accuracy of +0.8/-0.75 °C, for a

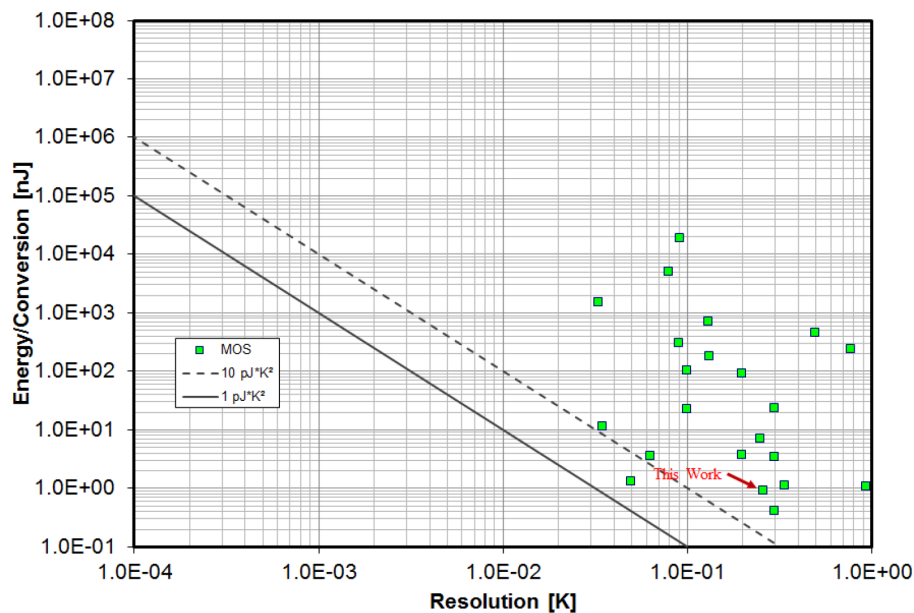


Figure 16. Comparison of the presented sensor with published sensors.

temperature range of $-55\text{ }^{\circ}\text{C}$ to $125\text{ }^{\circ}\text{C}$ with a resolution of $0.26\text{ }^{\circ}\text{C}$ for the same temperature range. The sensor consumes an area and power of 0.009 mm^2 and $8.8\text{ }\mu\text{W}$, respectively. The subthreshold operation makes the sensor suitable for low-power RFID applications.

References

- [1] Pertijs MAP, Huijsing JH. Precision Temperature Sensors in CMOS Technology. 1st ed. Dordrecht, the Netherlands: Springer, 2006.
- [2] Vaz A, Ubarretxena A, Zalvide I, Pardo D, Solar H, Garcia-Alonso A, Berenguer R. Full passive UHF tag with a temperature sensor suitable for human body temperature monitoring. *IEEE T Circuits-II* 2010; 57: 95-99.
- [3] Opasjumruskit K, Thanthipwan T, Sathusen O, Sirinamarattana P, Gadmanee P, Pootarapan E, Wongkomet N, Thanachayanont A, Thamsirianunt M. Self-powered wireless temperature sensors exploit RFID technology. *IEEE Pervas Comput* 2006; 5: 54-61.
- [4] Meijer GCM, Pertijs MAP, Makinwa KAA. Smart Sensor Systems: Emerging Technologies and Applications. 1st ed. Chichester, UK: Wiley, 2014.
- [5] Aita AL, Pertijs MAP, Makinwa KAA, Huijsing JH, Meijer GCM. Low-power CMOS smart temperature sensor with a batch-calibrated inaccuracy of $\pm 0.25\text{ }^{\circ}\text{C}$ from $-70\text{ }^{\circ}\text{C}$ to $130\text{ }^{\circ}\text{C}$. *IEEE Sens J* 2013; 13: 1840-1848.
- [6] Chen P, Chen TK, Wang YS, Chen CC. A time-domain sub-micro watt temperature sensor with digital set point programming. *IEEE Sens J* 2009; 9: 1639-1646.
- [7] Woo K, Meninger S, Xanthopoulos T, Crain E, Ha D, Ham D. Dual-DLL-based CMOS all digital temperature sensor for microprocessor thermal monitoring. In: International Solid-State Circuits Conference (ISSCC) Digest of Technical Papers; 2009; San Francisco, CA: IEEE. pp. 68-69.
- [8] Ituero P, Ayala, J, Lopez-Vallejo M. A nanowatt smart temperature sensor for dynamic thermal management. *IEEE Sens J* 2008; 8: 2036-2043.
- [9] Ueno K, Asai T, Amemiya Y. Low-power temperature-to-frequency converter consisting of subthreshold CMOS circuits for integrated smart temperature sensors. *Sens Actuators, A* 2011; 165: 132-137.

- [10] Tutsoy O. Design and comparison base analysis of adaptive estimator for completely unknown linear systems in the presence of OE noise and constant input time delay. *Asian J Control* 2016; 18: 1020-1029.
- [11] Souri K, Chae Y, Makinwa KAA. A CMOS temperature sensor with a voltage-calibrated inaccuracy of ± 0.15 °C (3σ) from -55 °C to 125 °C. *IEEE J Solid-St Circ* 2013; 48: 292-301.
- [12] Hwang S, Koo J, Kim K, Lee H, Kim C. A 0.008 mm² 500 /spl mu/W 469 kS/s frequency-to-digital converter based CMOS temperature sensor with process variation compensation. *IEEE T Circuits-I* 2013; 60: 2241-2248.
- [13] Anand T, Makinwa KAA, Hanumolu PK. A VCO based highly digital temperature sensor with 0.034 °C/mV supply sensitivity. *IEEE J Solid-St Circ* 2016; 51: 2651-2663.
- [14] Bashir M, Patri SR, KSR K. An ultralow power, 0.003 -mm² area, voltage to frequency based smart temperature sensor for -55 °C to 125 °C with one-point calibration. *Turk J Elec Eng & Comp Sci* 2017; 25: 2995-3007.
- [15] Bashir M, Patri SR, Krishnaprasad KSR. On-chip CMOS temperature sensor with current calibrated accuracy of -1.1 °C to $+1.4$ °C (3σ) from -20 °C to 150 °C. In: 2015 19th International Symposium on VLSI Design and Test; 2015; Ahmedabad India: IEEE. pp. 1-5.
- [16] Huang Q, Joo H, Kim J, Zhan C, Burm J. An energy-efficient frequency-domain CMOS temperature sensor with switched vernier time-to-digital conversion. *IEEE Sens J* 2017; 17: 3001-3011.
- [17] Saligane M, Khayat-zadeh M, Zhang Y, Jeong S, Blaauw D, Sylvester D. All-digital SoC thermal sensor using on-chip high order temperature curvature correction. In: 2015 IEEE Custom Integrated Circuits Conference (CICC); 2015; San Jose, CA: IEEE. pp. 1-4.
- [18] Allen PE, Holberg DR. CMOS Analog Circuit Design. 2nd ed. New York, NY, USA: Oxford University Press, 2010.
- [19] Ho Y, Yang YS, Su C. A 0.2 - 0.6 V ring oscillator design using bootstrap technique. In: Asian Solid-State Circuits Conf. (ASSCC), Dig. Tech. Papers; Nov. 2011; Jeju: IEEE. pp. 333-336.
- [20] Ueno K, Hirose T, Asai T, Amemiya Y. A 300 nW, 15 ppm/°C, 20 ppm/V CMOS voltage reference circuit consisting of subthreshold MOSFETs. *IEEE J Solid-St Circ* 2009; 44: 2047-2054.