

Decoupled indirect duty cycle PWM technique with carrier frequency adjustment for a matrix converter

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Abstract: The conventional sinusoidal pulse width modulation (SPWM) and the space vector PWM (SVPWM) switching techniques are widely used for power converters due to their ability to control the harmonic content of the output voltage. The most popular PWM techniques used in matrix converters are direct space vector modulation (DSVM) and indirect space vector modulation (ISVM). Since these techniques are complex and difficult to implement, there is demand for a PWM technique with minimum computation to operate matrix converters continuously. In this paper, decoupled indirect duty cycle (DIDC) PWM technique is proposed for the conventional matrix converter (CMC). This technique eliminates the duty cycle computations required for every switching period. In addition, the carrier frequency adjustment technique (CFAT) is proposed to improve the quality of both output voltages and input currents. A MATLAB–Simulink-based simulation proves the efficiency of the proposed algorithms, and an experimental setup is developed to validate them.

Key words: Carrier frequency adjustment, decoupled indirect duty cycle, mathematical modeling of matrix converters, space vector pulse width modulation, sinusoidal pulse width modulation

1. Introduction

The matrix converter functions as a direct AC-to-AC converter that interconnects two independent three-phase systems at different frequencies. Mathematical formulation of modulation technique for a matrix converter (MC) through direct transfer function approach was first proposed by Alesina and Venturini [1]. Later, to increase the voltage transfer ratio (VTR), the optimum Alesina Venturini (OAV) method [2] was proposed. A conceptually different fictitious DC link concept [3,4] was used to decouple the controller into smaller independent modules. A scalar control algorithm, using max–mid–min pulse width modulation (PWM) technique and rotating space vector, was used to eliminate the common mode voltage and synthesize the outputs of the matrix converter-fed induction machines system. For the modeling, analysis, and control of the MC, a generalized technique using singular value decomposition has been proposed [5–14]. The decoupling of the MC into a fictitious current source converter and fictitious voltage source inverter is shown in Figures 1a and 1b, respectively.

2. Mathematical modeling of the proposed decoupled indirect duty cycle PWM

The mathematical modeling of the decoupled indirect duty cycle (DIDC) PWM technique [15] is derived by decoupling modulation matrix (μ) into input and output matrixes, given by Eq. (1).

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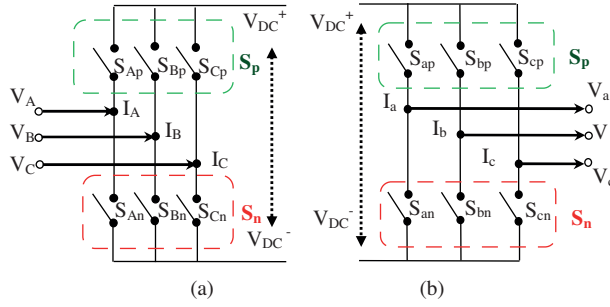


Figure 1. Matrix converter: a) input converter, b) output converter.

$$\mu = \begin{bmatrix} \mu_{Aa} & \mu_{Ab} & \mu_{Ac} \\ \mu_{Ba} & \mu_{Bb} & \mu_{Bc} \\ \mu_{Ca} & \mu_{Cb} & \mu_{Cc} \end{bmatrix} = \begin{bmatrix} \mu I_{ap} & \mu I_{an} \\ \mu I_{bp} & \mu I_{bn} \\ \mu I_{cp} & \mu I_{cn} \end{bmatrix} \times \begin{bmatrix} \mu C_{Ap} & \mu C_{Bp} & \mu C_{Cp} \\ \mu C_{An} & \mu C_{Bn} & \mu C_{Cn} \end{bmatrix} \quad (1)$$

The input converter is modeled to give the expected input currents at each leg of the converter, given by Eqs. (2)–(4) as follows:

$$I_A = I_m \sin(\omega_s t + \varphi_i) \quad (2)$$

$$I_B = I_m \sin(\omega_s t + \varphi_i + 120^\circ) \quad (3)$$

$$I_C = I_m \sin(\omega_s t + \varphi_i + 120^\circ), \quad (4)$$

where I_m represents maximum current; I_A , I_B , and I_C represent converter current at each leg; and ω_s represents angular frequency. The conduct time for each leg in a given sampling period defines the duty cycle for each leg. This cycle is proportional to the absolute value of the input reference given by Eqs. (5)–(7), and is shown in Figure 2.

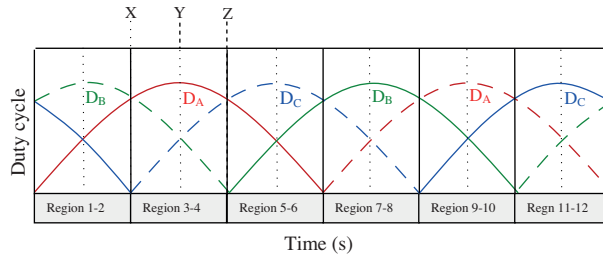


Figure 2. Duty cycles of the input converter legs.

$$D_A = |\sin(\omega_s t + \varphi_i)| \quad (5)$$

$$D_B = |\sin(\omega_s t + \varphi_i + 120^\circ)| \quad (6)$$

$$D_C = |\sin(\omega_s t + \varphi_i + 120^\circ)|, \quad (7)$$

where D_A , D_B , and D_C are the duty cycles of each leg.

Conduction time for each leg is proportional to the magnitude of the phase voltage at unity power factor. For example, at point Y in Figure 2, where phase A voltage is maximum, the leg corresponding to phase A conducts for the entire switching period, whereas the legs corresponding to phases B and C conduct for half the switching period. It is observed that the duty cycle of the leg corresponding to phase B reduces progressively, whereas the duty cycle of the leg corresponding to phase C increases progressively. During the X to Z interval, the phase A leg duty cycle is maximum.

The modulation function for each switch is given by Eqs. (8)–(13).

$$\mu C_{Ap} = (D_A + \sin(\omega_s t + \varphi_i))/2 \tag{8}$$

$$\mu C_{Bp} = (D_B + \sin(\omega_s t + \varphi_i + 120^\circ))/2 \tag{9}$$

$$\mu C_{Cp} = (D_C + \sin(\omega_s t + \varphi_i + 120^\circ))/2 \tag{10}$$

$$\mu C_{An} = (D_A \sin(\omega_s t + \varphi_i))/2 \tag{11}$$

$$\mu C_{Bn} = (D_B \sin(\omega_s t + \varphi_i + 120^\circ))/2 \tag{12}$$

$$\mu C_{Cn} = (D_C \sin(\omega_s t + \varphi_i + 120^\circ))/2, \tag{13}$$

where μC_{Ap} , μC_{Bp} , and μC_{Cp} are the modulation functions of the positive switches corresponding to phases A, B, and C, respectively; μC_{An} , μC_{Bn} , and μC_{Cn} are the modulation functions of the negative switches corresponding to phases A, B, and C, respectively.

At all points in the XZ region, except for Y where D_A is maximum, the input converter does not conduct for a period of $(1 - D_A) \times T_S$, i.e. all the legs of the converter are turned off for a period of $(1 - D_{max}) \times T_S$. Since the algorithm is derived from the assumption that the load is highly inductive, it is necessary to provide a freewheeling path for the inductive load currents. This is achieved by turning on both switches of any one leg of the output converter. This action modifies the modulation function of each switch.

The leg in which both switches are ON for a period of $(1 - D_{max}) \times T_S$ is selected based on the common mode voltage reduction rule [9]. The switches in the leg having the minimum duty cycle should be connected to the floating load terminal of the matrix converter during freewheeling. Extending this idea, it can be formulated that in the XY region, both switches of leg C conduct for an additional period of $(1 - D_A) \times T_S$, since leg C has the minimum duty cycle. Similarly, in the YZ region, both switches of leg B conduct for the same additional period. The duty cycle of switches $\mu C_{D_{min-p}}$ and $\mu C_{D_{min-n}}$ in the leg with the minimum duty cycle D_{min} are given by Eqs. (14) and (15).

$$\mu C_{D_{min-p}} = \mu C_{D_{min-p}} + (1 - D_{max}) \tag{14}$$

$$\mu C_{D_{min-n}} = \mu C_{D_{min-n}} + (1 - D_{max}) \tag{15}$$

Figure 3 shows the modified duty cycle of the switches in leg A. When the phase A voltage is minimum, both switches of leg A conduct for an additional period of $(1 - D_B)$ in Region 1, where the B-phase voltage is maximum. Similarly, the other phases conduct for an additional period in the other regions. Table 1 gives the input converter’s switch modulation function in terms of duty cycle. Figures 4a and 4b show the duty cycle of the positive and negative switches of the input converter, respectively.

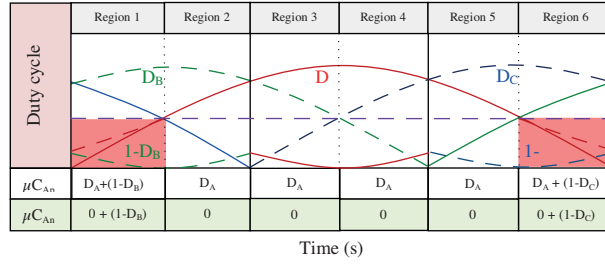
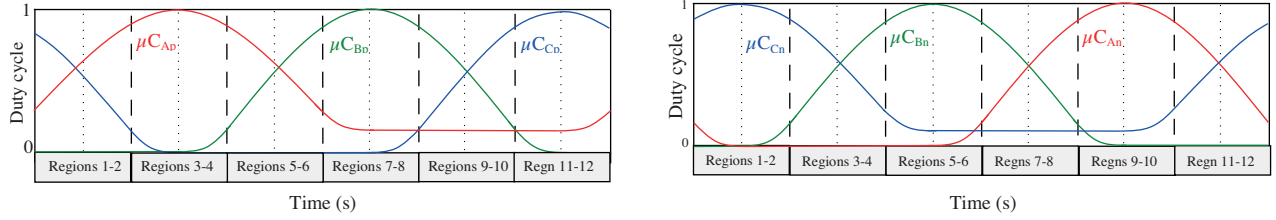

Figure 3. Duty cycle formulations for input converter switches SAP and San.

Figure 4. a) Duty cycles of the positive switches for the input converter. b) Duty cycles of the negative switches for the input converter.

Table 1. Input converter switch modulation function.

Switches	Regions					
	1	2	3	4	5	6
μC_{Ap}	$1 + D_A - D_B$	D_A	D_A	D_A	D_A	$1 + D_A - D_C$
μC_{Bp}	0	0	0	$1 - D_A$	$1 + D_B - D_C$	D_B
μC_{Cp}	D_C	$1 + D_C - D_B$	$1 - D_A$	0	0	0
μC_{An}	$1 - D_B$	0	0	0	0	$1 - D_C$
μC_{Bn}	D_B	D_B	D_B	$1 + D_B - D_A$	$1 - D_C$	0
μC_{Cn}	0	$1 - D_B$	$1 + D_C - D_A$	D_C	D_C	D_C
Switches	Regions					
	7	8	9	10	11	12
μC_{Ap}	$1 - D_B$	0	0	0	0	$1 - D_C$
μC_{Bp}	D_B	D_B	D_B	$1 + D_B - D_A$	$1 - D_C$	0
μC_{Cp}	0	$1 - D_B$	$1 + D_C - D_A$	D_C	D_C	D_C
μC_{An}	$1 + D_A - D_B$	D_A	D_A	D_A	D_A	$1 + D_A - D_C$
μC_{Bn}	0	0	0	$1 - D_A$	$1 + D_B - D_C$	D_B
μC_{Cn}	D_C	$1 + D_C - D_B$	$1 - D_A$	0	0	0

The output converter is modeled to give the expected output phase voltages, as given by Eqs. (16)–(18).

$$V_a = V_m \sin(\omega_o t + \varphi_o) \quad (16)$$

$$V_b = V_m \sin(\omega_o t + \varphi_o + 120^\circ) \quad (17)$$

$$V_c = V_m \sin(\omega_o t + \varphi_o + 240^\circ) \quad (18)$$

The duty cycles of legs D_a , D_b , and D_c for sinusoidal pulse width modulation (SPWM) and the required constraints are given by Eqs. (19) and (20), respectively.

$$D_a = D_b = D_c = 1 \quad (19)$$

$$\mu I_{ip} + \mu I_{in} = 1, \quad (20)$$

where $i = a, b, \text{ or } c$, and μI_{ip} and μI_{in} are the duty cycles of the upper and the lower arm switches, respectively. The duty cycle of each switch for SPWM [7,16–18] is given by Eqs. (21)–(23).

$$\mu I_{ap} = (1 + \sin(\omega_o t + \varphi_o)) / 2 \quad (21)$$

$$\mu I_{bp} = (1 + \sin(\omega_o t + \varphi_o - 120^\circ)) / 2 \quad (22)$$

$$\mu I_{cp} = (1 + \sin(\omega_o t + \varphi_o + 120^\circ)) / 2 \quad (23)$$

However, the sine PWM method reduces the DC bus utilization to $\frac{V_{dc}}{2}$ of the phase voltage, which, in turn, reduces the performance of the MC. To increase the DC bus utilization by a factor of $\frac{2}{\sqrt{3}}$, a third harmonic zero-sequence component is used to modify the duty cycles of the legs in [19–21], as given by Eq. (24).

$$D_a = D_b = D_c = 1 - Z_{3c} \quad (24)$$

where Z_{3c} is the third harmonic zero-sequence component, whose shape and offset is given by Eq. (25):

$$Z_{3c} = ((12K_0) + K_0 \mu I_{max-p} + (1K_0) \mu I_{min-p}), \quad (25)$$

where K_0 is the ratio between the two zero vectors of the inverter, V_0 and V_7 . The output converter does not conduct current for a period of $Z_{3c} \times T_s$. This means that all the legs are disconnected from the source for a period $Z_{3c} \times T_s$. It is required to provide a freewheeling path to the inductive load currents while turning off the output converter. This is achieved by turning on all the switches in the upper or lower arms of the converter. As the common mode voltage of the MC depends only on the zero vectors of the input converter, the zero vectors of the output converter are not significant enough to reduce the common mode voltage. Hence, for easy digital implementation of zero vectors, the value of K_0 is chosen as 1. This modifies Eq. (25) as Eq. (26):

$$Z_{3c} = (1 - \mu I_{max-p}), \quad (26)$$

where $\mu I_{max-p} = \max |\mu I_a, \mu I_b, \mu I_c|$.

Figure 5 shows the duty cycle of the output converter leg. The modified duty cycle of the switches of the output converter is given by Eqs (27)–(29), and its pictorial representation is shown in Figure 6.

$$\mu I_{ap}^* = ((1 + \frac{2}{\sqrt{3}} \sin(\omega_o t + \varphi_o)) / 2) + Z_{3c} \quad (27)$$

$$\mu I_{bp}^* = ((1 + \frac{2}{\sqrt{3}} \sin(\omega_o t + \varphi_o - 120^\circ)) / 2) + Z_{3c} \quad (28)$$

$$\mu I_{cp}^* = ((1 + \frac{2}{\sqrt{3}} \sin(\omega_o t + \varphi_o + 120^\circ)) / 2) + Z_{3c} \quad (29)$$

Figures 7a and 7b show the duty cycle of the positive and negative switches of the output converter, respectively. By superimposing the three-phase rectified waveforms $|W_{123}|$, the duty cycle of the negative switch is obtained

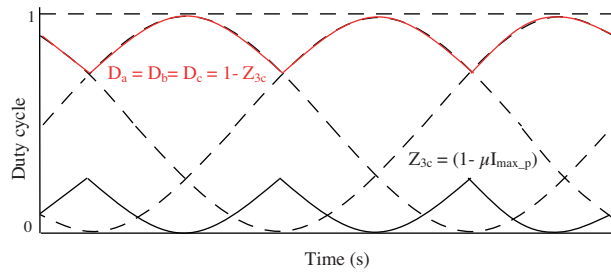


Figure 5. Duty cycles of the output converter leg.

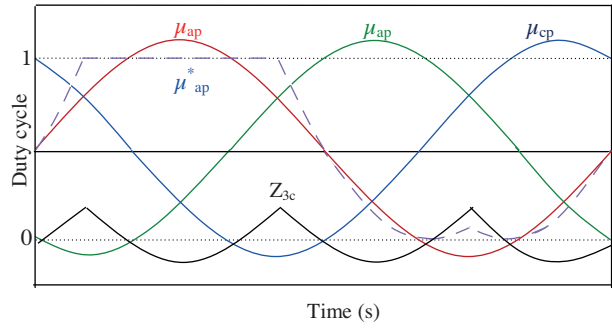


Figure 6. Formulation of switch (Sap) duty cycle for the output converter.

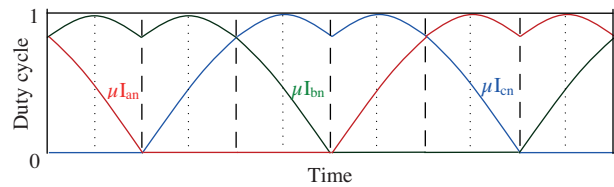
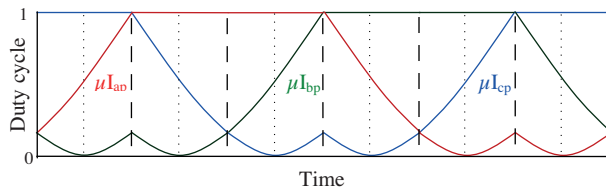


Figure 7. a) Duty cycles of the positive switches for the output converter. b) Duty cycles of the negative switches for the output converter.

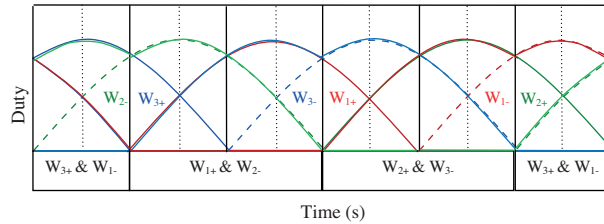


Figure 8. Duty cycles of the negative switches superimposed on the new reference W_{123} .

Table 2. Duty cycles for all the switches of the output converter as a function of $|W_{123}|$.

Regions	W_{1+} & W_{2-}	W_{2+} & W_{3-}	W_{3+} & W_{1-}
μI_{ap}	1	$(1 - W_2)$	$(1 - W_1)$
μI_{bp}	$(1 - W_2)$	1	$(1 - W_3)$
μI_{cp}	$(1 - W_1)$	$(1 - W_3)$	1
μI_{an}	0	$ W_2 $	$ W_1 $
μI_{bn}	$ W_2 $	0	$ W_3 $
μI_{cn}	$ W_1 $	$ W_3 $	0

as shown in Figure 8. The duty cycle of each switch is the selected portions of the waveforms $|W_{123}|$. Table 2 shows the duty cycle of each switch as a function of the new reference signal $|W_{123}|$ in each distinct region.

The extracted duty cycles from different segments of the line voltage at different times are compared with a high-frequency carrier to produce the switching signals for the MC. The extraction of duty cycle and switching signals is performed using a simple op-amp-based analogue circuit, which eliminates the need for a processor and ADC to sense the line voltage for fixing the reference current for the fictitious current source converter.

2.1. Analytical treatment of DIDC PWM

With the conventional indirect space vector PWM (ISVPWM) technique, the duty cycles of MCs are computed using the concept of duty cycle sharing (DCS) between output voltage vector (OVV) duty cycle and input current vector (ICV) duty cycle, as stated in the literature [21–25].

With the DIDC PWM technique, the matrix converter’s ICV and OVV are applied simultaneously for a duration of (pT_S , qT_S , and rT_S) and (xT_S , yT_S , and zT_S), as shown in Figure 9a. This shows that duty cycle sharing between all OVVs and the ICV, as in the ISVPWM technique, cannot be achieved with the DIDC PWM technique, which leads to a deterioration of input current and output voltage quality.

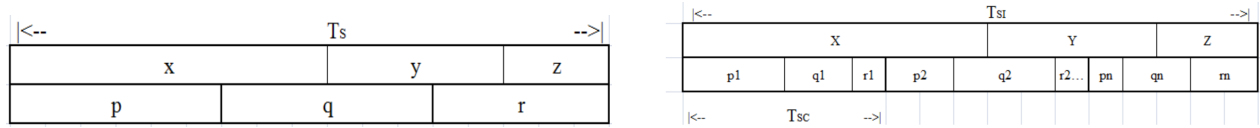


Figure 9. a) Sharing of duty cycle with the DIDCPWM technique. b) Sharing of duty cycles with DIDCPWM with CFAT.

To overcome the above issue with the DIDC PWM technique, carrier frequency adjustment technique (CFAT) is proposed, where the ICV and OVV are applied simultaneously for a duration of (pT_{SC} , qT_{SC} , and rT_{SC}) and (xT_{SI} , yT_{SI} , and zT_{SI}), as shown in Figure 9b, where T_{SC} ($f_{sic} = 1/T_{SC}$) and T_{SI} ($f_{soc} = 1/T_{SI}$) are the switching period of the converter and inverter, respectively.

Case 1: when n is an integer. n is defined as the ratio between T_{SI} and T_{SC} ($T_{SI} = nT_{SC}$ (or) $T_{SI} = (1/n) T_{SC}$).

The sharing of voltage and current vectors in CFAT is performed using the following expressions:

$$\left. \begin{aligned}
 dx_i p_j &= f\{p_j, nx_i (j - 1)\} \\
 dx_i q_j &= f\{q_j, nx_i (j - 1) - p_j\} \\
 dx_i r_j &= f\{r_j, nx_i (j - 1) - p_j - q_j\} \\
 dy_i p_j &= f\left\{0, \frac{p_j}{n} y_i, \frac{(j-1)+p_j-nx_i}{n}, \frac{n(1-z_i)-(j-1)}{n}\right\} \\
 dy_i q_j &= f\left\{0, \frac{q_j}{n}, y_i, \frac{(j-1)+p_j+q_j-nx_i}{n}, \frac{n(1-z_i)-(j-1)-p_j}{n}\right\} \\
 dy_i r_j &= f\left\{0, \frac{r_j}{n}, y_i, \frac{(j-1)+p_j+q_j-nx_i}{n}, \frac{n(1-z_i)-(j-1)-p_j-q_j}{n}\right\} \\
 dz_i p_j &= f(j - 1) + p_j n(1 - z_i) \\
 dz_i q_j &= f(j - 1) + p_j + q_j - n(1 - z_i) \\
 dz_i r_j &= fj - n(1 - z_i),
 \end{aligned} \right\} \tag{30}$$

where for any given i , the duty cycles of the DIDC PWM technique with CFAT are given below:

$$d_{vxcx} = \sum_{j=1}^n dx_i p_j, \quad d_{vxcy} = \sum_{j=1}^n dx_i q_j, \quad d_{vycx} = \sum_{j=1}^n dy_i p_j, \quad d_{vycy} = \sum_{j=1}^n dy_i q_j,$$

and

$$d_z = \sum_{j=1}^n dx_i r_j + \sum_{j=1}^n dy_i r_j + \sum_{j=1}^n dz_i p_j + \sum_{j=1}^n dz_i q_j + \sum_{j=1}^n dz_i r_j$$

The duty cycles of ISVPWM and DIDCPWM with CFAT were computed for different ratios of T_{SC} and T_{SI} (i.e. for different values of n) in MATLAB. The duty cycle of DIDCPWM with CFAT approximates the duty cycles of ISVPWM technique as n increases. Although the duty cycles of DIDCPWM with CFAT match the duty cycles of ISVPWM as n increases, the total harmonic distortion (THD) is found to be higher due to the frequent switching of the zero vectors.

Case 2: n is a fraction.

This case can be divided into the two following subcases.

Case 2a: n is rational fraction.

In cases where n is $1/2, 1/3, 1/4, 1/5, 1/6, \dots$, the sharing of voltage and current vectors is similar to Case 1.

Case 2b: n is irrational fraction.

Since such analytical treatment is not possible for this case, simulations were performed in Simulink environment, and the THD values were determined for the input current using FFT analysis. For $n = 3/4$, the THD results were found to be lowest compared to all other cases due to minimum usage of zero vectors.

3. Carrier frequency adjustment technique

CFAT is proposed to reduce the THD of the MC. The carrier frequency of the input ($f_{s_{ic}}$) and output converter ($f_{s_{oc}}$) are kept different for CFAT. Figure 10a shows THD of the input current at an output frequency of 20 Hz for $f_{s_{ic}} = f_{s_{oc}}$. Figure 10b shows the THD of the input current at an output current frequency of 20 Hz for $f_{s_{ic}} \neq f_{s_{oc}}$. It is understood that the input current THD is much higher for the same carrier frequency when $f_{s_{ic}} = f_{s_{oc}}$ than when ($f_{s_{ic}} \neq f_{s_{oc}}$). Eq. (31) gives the computation of the THDs for different values of $f_{s_{ic}}$ and $f_{s_{oc}}$ at constant output frequency.

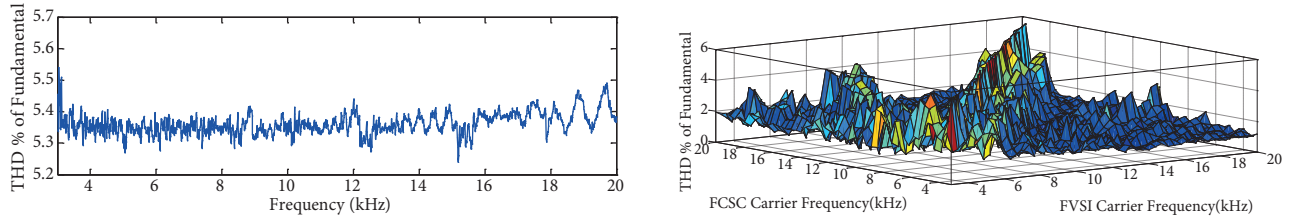


Figure 10. a) THD for $f_{s_{ic}} = f_{s_{oc}}$ with $f_o = 20$ Hz. b) THD when $f_{s_{ic}} \neq f_{s_{oc}}$ with $f_o = 20$ Hz.

$$THD = \frac{1}{I_1} \sqrt{\sum_{i=2}^{100} I_i^2} \quad (31)$$

where I_1 and I_i are the fundamental and i th harmonic components of input current, respectively.

Figure 11a gives the THD for various ratios of $f_{s_{ic}}$ to $f_{s_{oc}}$ and load frequencies. Figure 11b gives the plot of THD vs. output load current frequencies for $f_{s_{ic}}$ -to- $f_{s_{oc}}$ ratios of 1:1 and 1:3/4. For the $f_{s_{ic}}$ -to- $f_{s_{oc}}$ ratio of 1:3/4, the THD is found to be 3.14% at different output frequencies, which is within the acceptable limit of 5%. Hence, to improve the THD of the input current for a wide range of output frequencies, the ratio of $f_{s_{ic}}$ -to- $f_{s_{oc}}$ is chosen as 1:3/4.

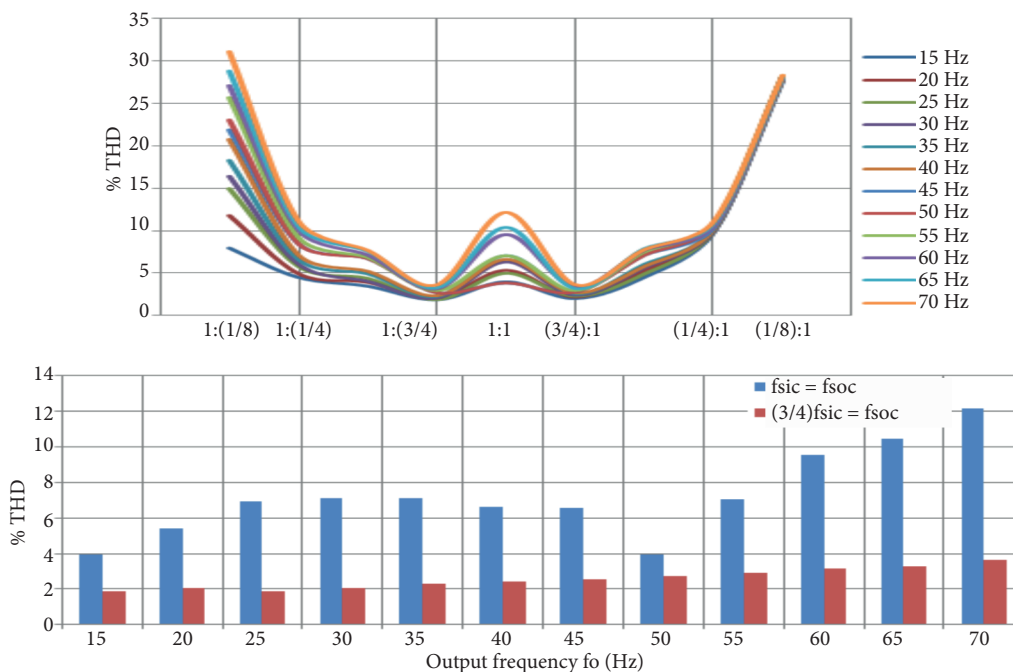


Figure 11. a) THD for different ratios of f_{sic} and f_{soc} with varying f_o . b) THD for ratios of $f_{sic} = f_{soc}$ and $3/4 f_{sic} = f_{soc}$ with varying f_o .

4. Simulations

The performance of the proposed DIDC PWM technique for MC is studied in MATLAB Simulink environment. The simulation parameters are listed in Table 3. Figures 12a and 12b show the harmonic spectrum of the input currents with and without CFAT, respectively. The harmonic spectrum of the input currents without CFAT has high lower order harmonics, whereas with CFAT they are reduced. A low-pass filter is designed to improve the input current spectrum with 1-kHz cut-off frequency. Figure 13 shows the output current spectrum of the MC when the ratio of f_{sic} -to- f_{soc} is 1:3/4 and the THD is found to be 0.56%, which is within the acceptable limit. For a modulation index of 0.75, Figures 12b and 13 show that the input and output current spectrum have a THD of 1.84% and 0.56%, respectively.

Table 3. Simulation parameters for the DIDC PWM technique.

Quantity	Value
R-L load	R = 20 Ω , L = 21 mH
Input phase voltage	100 V
Input voltage frequency	50 Hz
Input filter	L = 2.5 mH, C = 10 μ F, R_d = 15 Ω
Output voltage frequency	25 Hz
Modulation index	0.75
Switching frequency	7 kHz

Figures 14a and 14b show the input and output current waveforms for the unity input power factor, which is nearly sinusoidal. For a lower modulation index, the THD of the input and output currents remains the same. Figures 14c and 14d show the output line and phase voltages, respectively.

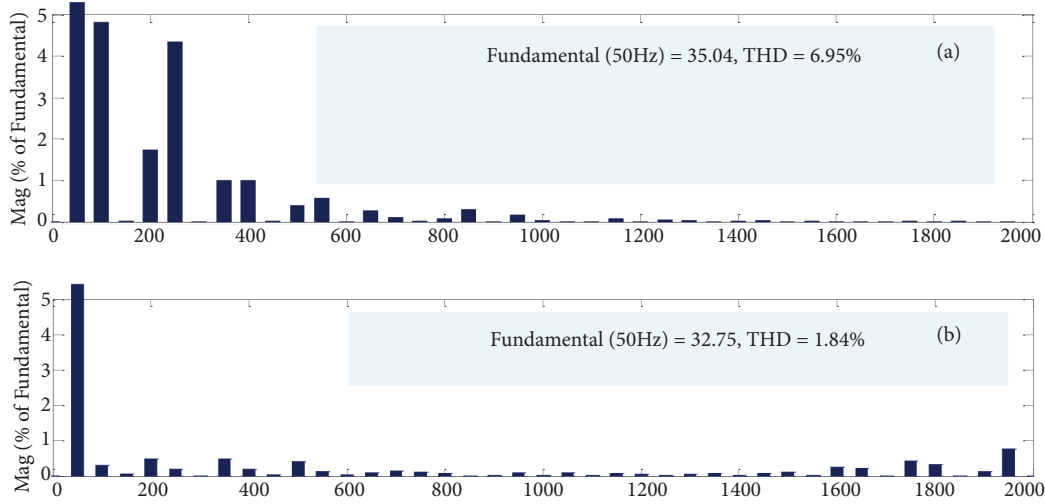


Figure 12. Input current spectrum at $f_o = 25$ Hz : a) $f_{sic} = f_{soc}$, b) $\frac{3}{4} f_{sic} = f_{soc}$.

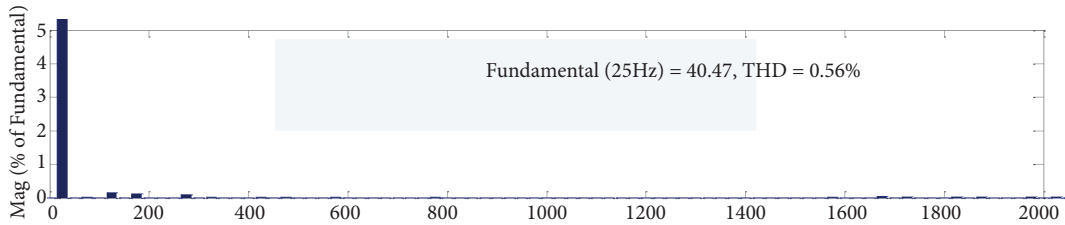


Figure 13. Output current spectrum at $f_o = 25$ Hz with $\frac{3}{4} f_{sic} = f_{soc}$.

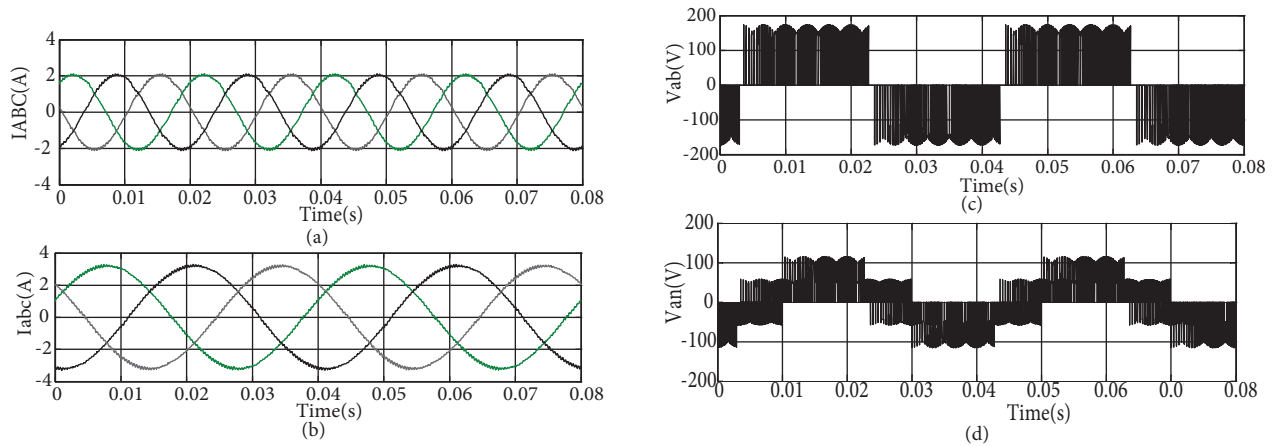


Figure 14. Simulation results: a) input current, b) output current, c) output line voltage, and d) output phase voltage.

5. Hardware implementations

A 1.5-kVA prototype MC is developed to test the proposed control algorithms. Figure 15 shows the block diagram of hardware implementation. The prototype consists of a control circuit, a CONCEPT gate driver module (6SD106EI), and an MC module with bidirectional switches (ST Microelectronics-IRFP460). The control circuit consists of an analogue input acquisition board and logic circuits. The logic circuit is implemented using a field programmable gate array (FPGA) board (SPARTEN3E-XC3S500E). The FPGA generates the

switching pulses for the MC. The absolute values of the input references are obtained from the analogue acquisition board. This board consists of zero crossing detectors, comparators, and precision rectifiers. The duty cycle information is obtained from the input references. A current sensing circuit is used for determining the direction of the current. The duty cycles are compared with a high-frequency carrier signal to generate the switching information for the input and output converters, using FPGA.

The experiment was conducted with an input phase voltage of 100 V, switching frequency of 7 kHz, $R_L = 20 \Omega$, $L_L = 21 \text{ mH}$, and a modulation index of 0.75. The MC is used to convert the 50-Hz input voltage into a 25-Hz output voltage. Figure 16 shows the laboratory prototype of the MC.

Figure 17 shows the selected waveforms obtained from the experimental setup. These results help to verify the effectiveness of the proposed DIDC PWM technique for MC. Figures 17a and 17b show the filtered input and output currents of the MC, respectively. Figures 17c and 17d show the output line and phase voltages, respectively.

The four-step commutation procedure was implemented to overcome the commutation problem. This technique eliminates the very narrow switching pulses, which leads to the open circuit of the inductive load. In order to overcome this problem, the duty cycles were recalculated by simulation. Figures 14a, 14b, 17a, and 17b show that the input and the output current waveforms for practical implementation deviate from those of the simulation.

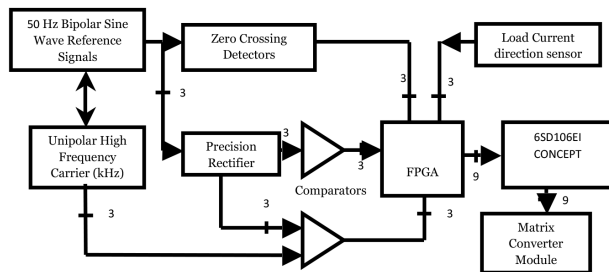
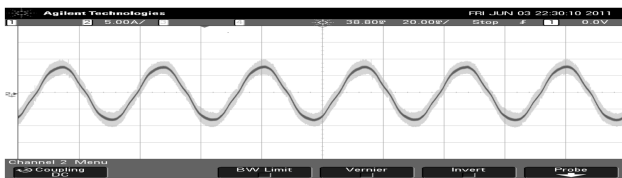


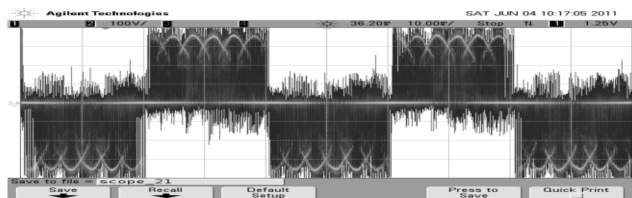
Figure 15. Block diagram of the hardware implementation.



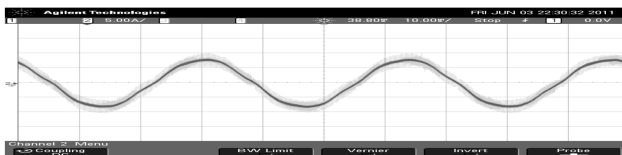
Figure 16. Laboratory prototype of the matrix converter.



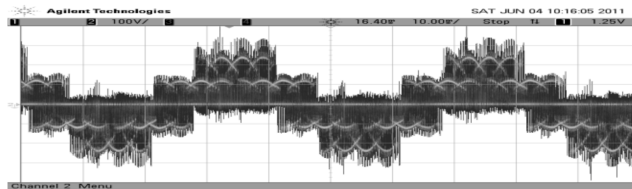
(a)



(c)



(b)



(d)

Figure 17. Hardware results: a) input current, b) output current, c) output line voltage, and d) output phase voltage.

6. Conclusion

In this paper, DIDCPWM with CFAT has been proposed to eliminate computational complexity for determining the duty cycle without affecting the voltage transfer ratio. It is implemented using a simple analogue circuit, which replaces the need for analogue-to-digital converters (ADCs) and high-speed processors. The DIDC PWM technique showed higher harmonic content in the input current when compared to the ISVM technique. However, the harmonic content of the output voltage did not deviate much. The proposed technique decreases the input current harmonics when the ratio of input-to-output carrier frequency is 1:3/4, improving the quality of the output as much as possible. The efficacy of the proposed algorithm is verified by both simulation and experimental results.

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