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Ultra low-power DC voltage limiter for RFID application in 0.18-μm CMOS technology

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Abstract: In this paper, a low-power DC voltage limiter is designed for radio frequency identification tags. In this design, the low-power bandgap reference (BGR) circuit, which is insensitive to temperature, and also the comparator are used for the voltage limiter circuit. To make the I-V curve approach the ideal one, four inverter stages are employed to the output of the comparator. The structure of the BGR and comparator use only MOSFET transistors that work in subthreshold region when the limiter is inactive. These two blocks have power consumption of 220 pW and 1300 pW, respectively. The limited output voltage is 1.5 V and the current consumption when the tag and the reader are far from each other is 31.56 nA, which is very insignificant compared with the total current consumption of the tag. The chip area of the voltage limiter circuit is 1936 μm^2. The simulation is done in 0.18-μm CMOS technology and the operational frequency is 960 MHz.

Key words: DC limiter, radio frequency identification, low power consumption, bandgap reference, proportional to absolute temperature, complementary to absolute temperature

1. Introduction

In passive radio frequency identification (RFID) technology, the tag power is supplied from the waves sent from the reader. Figure 1 shows different parts of the block diagram of the RFID tag power supply. First, after receiving AC waves, which are sent from the reader by the tag antenna, these waves are converted to DC voltage by the rectifier. Then the regulator eliminates the ripple of the rectifier output and the achieved voltage from DC to DC converter is changed into various voltage levels and consequently employed by different parts of the tag [1]. If the distance between the tag and the reader is reduced, the received power is increased based on Eq. (1) and thus it is possible to damage the circuit:

$$P_r = P_t G_t G_r \left(\frac{\lambda}{4\pi R}\right)^2, \tag{1}$$

where P_t is the RF power sent from the reader, G_t is the reader antenna gain, P_r is the received power, G_r is the tag antenna gain, λ is the wave length, and R is the distance between the tag and reader. For avoiding the damage resulting from the high received power, the block of the DC voltage limiter is employed after the rectifier block. When the received power reaches the defined value, the limiter provides the deviated path for the current, so it prevents the increasing of the DC voltage. One of the main characteristics of the limiter is the

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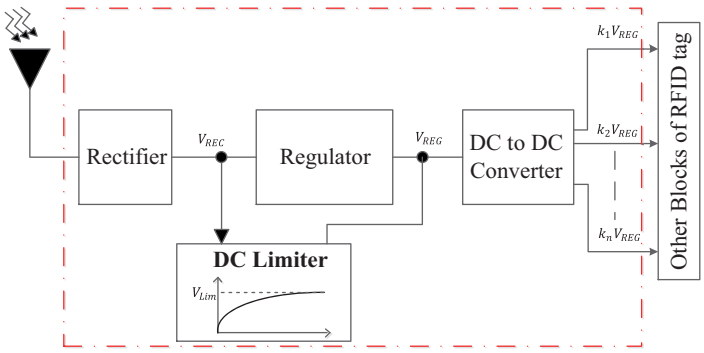

Figure 1. The power supply block of the RFID tag.

insignificant deviated current for the long distance of the tag and the reader. Therefore, the power dissipation is decreased and the reading range of the RFID system is increased.

In [2], diode connection NMOS transistors that work as the zener diode were used to deviate current. In this design, when the tag and reader are far from each other, the current is in the range of microamperes, which is considerable compared with the current consumption of the tag. In [3,4], the output of the other tag blocks such as the bandgap reference (BGR) and the voltage regulator are used for eliminating the voltage deviation of the limiter arising from process and temperature variations. This voltage variation against process and temperature variations in the range of 35 °C to 45 °C is ± 0.05 V.

In the limiter structure usually the BGR block is used to generate the reference voltage for comparison with the main voltage. In most of the BGR circuits, BJT transistors are used. In such transistors beta is changed by the variation of temperature and this characteristic is used in BGR circuits [5–10]. Since the main purpose of this design is reducing the power consumption and chip area, and due to the fact that BJT transistors consume more current than MOSFET transistors in the same conditions, the design of a BGR with BJT transistor dissipates more power. Also, by using BJT transistors, BiCMOS technology is required, which increases the price of fabrication in comparison with the CMOS technology that is used for MOSFET transistors. In [11] two different designs were used for producing the reference voltage, designed based on various temperature characteristics of NMOS transistors with different oxide thicknesses. This method complicates the process of fabrication. In [12] a diode connected transistor was used, supplied by a current source insensitive to voltage variations. The temperature coefficient of the BGR in [12] is somewhat high.

In the proposed DC voltage limiter, two blocks of comparator and BGR are utilized. The used blocks in this circuit are designed with MOSFET transistors. Due to the fact that all transistors work in the subthreshold region, the power consumption is very low. The use of four inverter stages at the output of the comparator helps the deviation of the current and the limitation of the output voltage as soon as the input voltage increases from the limited voltage.

In the BGR, only the MOSFET transistors are used, and for increasing the output voltage level, the cascade connection of the circuit core is used in proportional to absolute temperature (PTAT) and complementary to absolute temperature (CTAT) voltage generators.

Section 2 describes the structure of the proposed limiter. The BGR circuit and its subblocks, the comparator and the voltage divider, are evaluated in Sections 3 and 4, respectively. Finally the simulation results, comparison, and design layout are presented in Section 5.

2. The total structure of the proposed DC limiter

Figure 2 shows the complete structure of the proposed limiter. In this design, part of the output voltage of the rectifier (V_{REC}) is sampled by the voltage divider block. This sampled voltage is compared with the BGR voltage by the comparator block. The BGR voltage is insensitive to temperature variations.

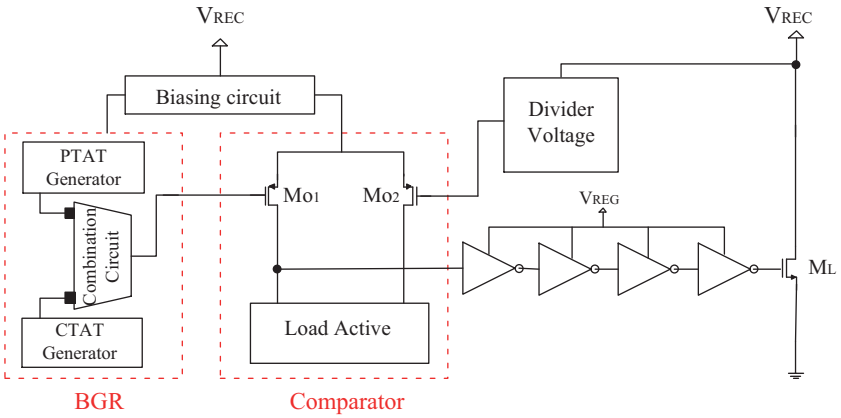

Figure 2. The complete structure of the proposed DC limiter.

In order to make the V-I characteristic curve of the limiter voltage be near the ideal one, four consecutive inverters are employed for the comparator output. If the difference of the sampled voltage and BGR voltage reaches the defined value, the outputs of the first and the third inverters become low while the outputs of the second and fourth inverters become high. In this case, transistor M_L becomes active and suddenly a large amount of current deviates and prevents the increase of the output voltage. Given the fact that the inverters are biased with the output voltage of the regulator (V_{REG}), when V_{REC} becomes slightly more than V_{Lim}, high voltage is employed at the gate of M_L and consequently it can prevent the increasing of the output voltage (Eq. (2)).

$$V_{REC}=\begin{cases} V_{REC} & \text{if} \quad V_{REC}<V_{Lim} \\ V_{Lim} & \text{if} \quad V_{REC}>V_{Lim} \end{cases} \tag{2}$$

V_{Lim} (limited voltage) is the constant value and in this work is 1.5 V. Therefore, the current consumption at V_{Lim} voltage and the duration of the off-state position of the limiter can be neglected.

3. The BGR structure

3.1. Basic principle of a BGR

The BGR structure is shown in Figure 3. This circuit includes four parts: the PTAT voltage generator, CTAT voltage generator, weight combination circuit, and bias circuit, which is insensitive to voltage variations. The circuit works as follows: the voltage combination block combines the PTAT voltage (it has a proportional relationship to the absolute temperature) and the CTAT voltage (it has a complementary relationship to the absolute temperature) and produces voltage independent of the temperature [13]. The different parts of the BGR are evaluated in the following sections.

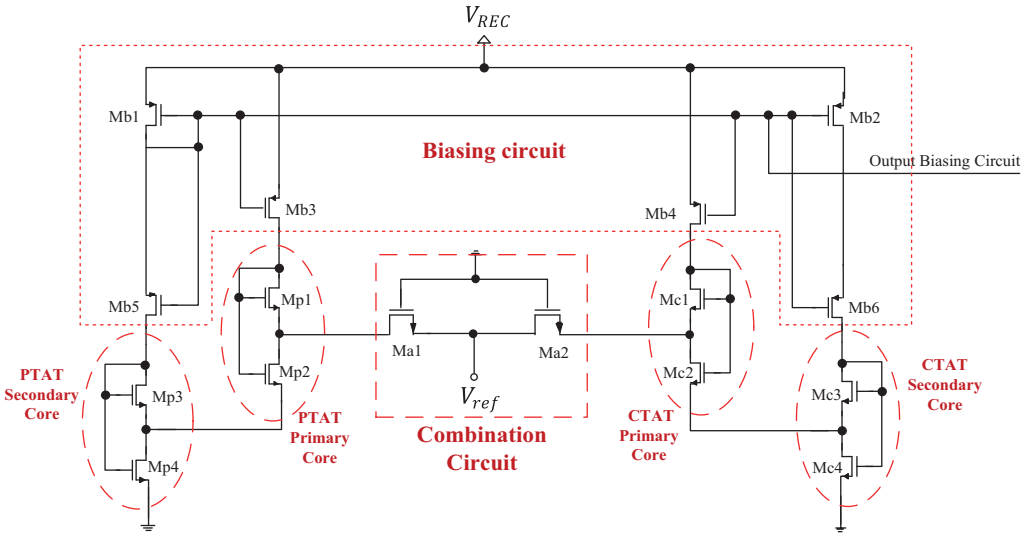

Figure 3. The BGR circuit.

3.2. The bias circuit

A fixed bias circuit that has insignificant sensitivity to input voltage variations is used in the designed circuit. This circuit is utilized for biasing the BGR and comparator blocks. Considering the fact that the voltage of the BGR circuit is supplied from V_{REC}, when the voltage is close to the limited voltage and when the limiter is off, the power consumption of the BGR is high. To solve this problem M_{b5} and M_{b6} transistors are employed, which cause all transistors used in the BGR structure to work in the subthreshold region when the limiter is off.

The maximum power dissipation of the bias circuit shown in Figure 3 is related to the second stage of PTAT and CTAT blocks. If transistors M_{b5} and M_{b6} are inserted into the second stage of the PTAT and CTAT blocks, the gate-source voltages of these blocks' transistors are set for working in the subthreshold region. Therefore, the power dissipation of this block can be neglected when the reader and the tag are far from each other.

3.3. PTAT and CTAT voltage generators

The PTAT and CTAT voltage generators are shown in Figure 3. The main core of the PTAT generator includes two NMOS transistors, which are connected to each other, and the output of the PTAT generator is the difference of the gate-source voltages of these two transistors [13,14].

Based on the bias circuit shown in Figure 3 and the working region of the transistors, the gate-source voltage of the subthreshold region is stated as in Eq. (3):

$$V_{gs} = \eta V_T \ln\left(\frac{I}{I_S\left(\frac{W}{L}\right)}\right) + V_{th} \tag{3}$$

where I_S is the specific current, V_{th} is the threshold voltage of the transistor, V_T is the thermal voltage, W/L is the transistor aspect ratio, and η is the subthreshold slope factor. If W/L of transistor M_{p1} is K_1 times more than that of transistor M_{p2}, the gate-source voltage difference of these two transistors equals the PTAT voltage that is achieved as in Eq. (4). Due to the positive temperature coefficient of V_T, by increasing the

temperature the PTAT voltage is increased.

$$V_{PTAT}=V_{gs,p2}-V_{gs,p1}=\eta V_T \ln(K_1) \tag{4}$$

where $K_1\,(K_1>1)$ is the ratio of the W/L of the M_{p1} transistor to the W/L of the M_{p2} transistor. If the output is in the form of the gate-source voltage difference of the two transistors, by considering Eqs. (3) and (4) for transistors M_{C1} and M_{C2}, the CTAT voltage can be produced [12]. In this condition if the W/L of transistor M_{C2} is $K_1^{'}\,(K_1^{'}>1)$ times more than that of transistor M_{C1} the output voltage is $-\eta V_T \ln(K_1^{'})$. That is decreased by increasing the temperature. A topology similar to that of the PTAT circuit is used and the W/L value of its transistors (M_{C1} and M_{C2}) is chosen precisely in order to create voltage insensitive to the temperature by combining the PTAT and CTAT voltages.

If only the primary core is used, for increasing the output voltage level, the sizes of M_{C1}, M_{C2}, M_{P1}, and M_{P2} transistors should be increased, which culminates in increasing the chip area and the power consumption. In the presented design, the secondary core is cascaded to the main core in order to increase the output voltage level by combining the two voltages with the help of the weight combination circuit. As shown in Figure 3, the outputs of the PTAT and CTAT voltage generators are calculated as in Eqs. (5) and (6):

$$V_{PTAT}=(V_{gs,p2}-V_{gs,p1})+(V_{gs,p4}-V_{gs,p3})=\eta V_T \ln(K_1)+\eta V_T \ln(2K_2)=\eta V_T \ln(2K_1K_2), \tag{5}$$

$$V_{CTAT}=(V_{gs,c2}-V_{gs,c1})+(V_{gs,c4}-V_{gs,c3})=-\eta V_T \ln\left(K_1^{'}\right)-\eta V_T \ln\left(2K_2^{'}\right)=-\eta V_T \ln\left(2K_1^{'}K_2^{'}\right), \tag{6}$$

where $K_1\,(K_1>1)$ is the ratio of the W/L of the M_{P1} transistor to the W/L of the M_{P2} transistor and $K_1^{'}\,(K_1^{'}>1)$ is the ratio of the W/L of the M_{C2} transistor to the W/L of the M_{C1} transistor. $K_2\,(K_2>1)$ is the ratio of the W/L of the M_{P3} transistor to the W/L of the M_{P4} transistor and $K_2^{'}\,(K_2^{'}>1)$ is the ratio of the W/L of the M_{C4} transistor to the W/L of the M_{C3} transistor. Eqs. (5) and (6) clarify that the voltage levels of PTAT and CTAT are improved. On the other hand, the secondary core has more control of the output voltages of PTAT and CTAT for minimizing the variations versus temperature.

3.4. The weight combination circuit

Given that the voltage variation of PTAT and CTAT is not the same in the given temperature range, the weight combination circuit is used to produce voltage insensitive to temperature.

In this configuration, the M_{a1} and M_{a2} transistors work in the cut-off region and the characteristics of the internal capacitors of the transistors are used. By analyzing the capacitance structure of the weight combination circuit, Eq. (7) is achieved:

$$V_{ref}=aV_{PTAT}+b.V_{CTAT}, \tag{7}$$

where a and b are the weight coefficients of V_{PTAT} and V_{CTAT}, respectively, and are dependent on the capacitance structure of the M_{a1} and M_{a2} transistors [13]. That resulted from Eqs. (8) and (9), respectively:

$$a=\frac{C_{DB1}}{C_{DB1}+C_{GB1}+C_{BS2}+C_{GB2}} \tag{8}$$

$$b=\frac{C_{BS2}}{C_{DB1}+C_{GB1}+C_{BS2}+C_{GB2}} \tag{9}$$

where C_{GB} is the gate-body capacitor, C_{DB} is the drain-body capacitor, and C_{BS} is the body-source capacitor of the M_{a1} and M_{a2} transistors.

The voltage variation of V_{CTAT} related to the temperature is lower than that of V_{PTAT}; thus, with the created weight coefficient and the combination of them, a constant voltage versus temperature is produced. By adjusting the value of W and L of the M_{a1} and M_{a2} transistors, the weight coefficient can be set appropriately.

4. The structure of the voltage divider and the comparator

Figure 4 shows the structure of the voltage divider and the comparator with four consecutive inverters connected at the output of the comparator. Six NMOS transistors (M_{d1}–M_{d6}) are used in the topology of the voltage divider as the diode connection. Due to the fact that all six transistors have the same structure and size, they work in the subthreshold region when the voltage is lower than V_{Lim}. On the other hand, since only MOSFET transistors are used in the design of the voltage divider and no resistors exist in this structure, the current consumption and the chip area are reduced. By the variation of the distance between reader and tag and also the input voltage, $V_{REC}/3$ is compared with the voltage of V_{ref}.

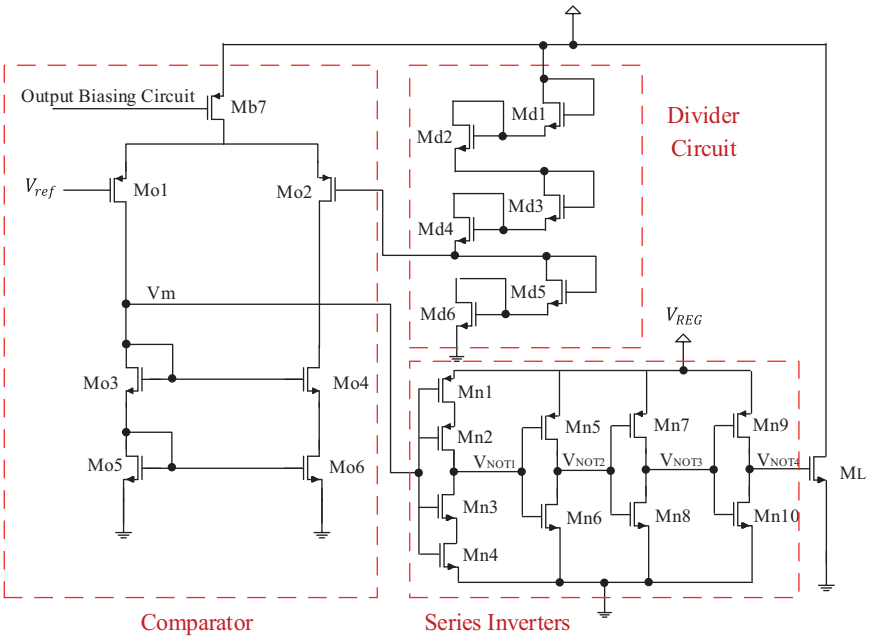

Figure 4. The structure of the voltage divider and the comparator.

A differential pair is utilized in the design of the comparator block. Based on the operation of the M_{b7} transistor in the subthreshold region, when the limiter is off the current consumption is very low. In addition, a cascade current mirror is used as an active load in the comparator block.

If the comparator output is employed by the M_L transistor directly, by the variation of the input voltage, the operation of the transistor varies from the cut-off region to the saturation region with a temperate slope. Therefore, the current deviates from the ideal case at limited voltage (V_{Lim}). In the proposed design, four series inverters, which are biased by the output of the regulator (M_{n1}–M_{n10}), are employed. The advantage of this design is that a large amount of current deviates when the input voltage is slightly more than V_{Lim}. Indeed, the V-I characteristic curve of the limiter improves to the ideal one.

In the first inverter the series pass-gate transistors are used. This structure significantly affects the decreasing of the power consumption of this block [15].

5. Simulation results

The simulation and the layout design of the proposed circuit are done in TSMC 0.18-μm CMOS technology at an operational frequency of 960 MHz. The presented simulations are based on the schematic and postlayout, which are done with Cadence software. In this design the confined voltage of the limiter is 1.5 V. Due to the fact that the required power of the tag is supplied from the waves sent by the reader, the increase of the distance between the tag and reader reduces the received power of the tag. Therefore, the lower power dissipation of the tag subblocks increases the reading range. Since the increase of supply voltage of the subblocks increases the power dissipation of the tag, in this design the transistors are biased in the subthreshold region to decrease the power consumption and the maximum supply voltage of 1.5 V is considered for the limiter output. The size of transistors (W/L) is presented in Table 1.

Table 1. The size of transistors.

Transistor	W/L (μm/μm)	Transistor	W/L (μm/μm)	Transistor	W/L (μm/μm)	Transistor	W/L (μm/μm)
M_{b1}	3/0.18	M_{c1}	0.25/0.8	M_{o3}	2/1	M_{n1}	0.25/5
M_{b2}	2/0.18	M_{c2}	1/0.5	M_{o4}	0.25/0.25	M_{n2}	0.25/5
M_{b3}	3/0.18	M_{c3}	0.25/1.5	M_{o5}	1/1	M_{n3}	0.25/3.3
M_{b4}	3/0.18	M_{c4}	1/0.5	M_{o6}	2/0.25	M_{n4}	0.25/3.3
M_{b5}	4/0.18	M_{p1}	7.2/0.18	M_{d1}	0.25/5	M_{n5}	0.5/0.18
M_{b6}	4/0.18	M_{p2}	0.5/5	M_{d2}	0.25/5	M_{n6}	2/0.18
M_{b7}	5/0.18	M_{p3}	7.2/0.18	M_{d3}	0.25/5	M_{n7}	0.5/0.18
M_{a1}	5/0.18	M_{p4}	0.5/5	M_{d4}	0.25/5	M_{n8}	2/0.18
M_{a2}	2.6/0.18	M_{o1}	3.6/0.18	M_{d5}	0.25/0.4	M_{n9}	0.5/0.18
M_L	4×5/0.18	M_{o2}	3.6/0.5	M_{d6}	0.25/0.4	M_{n10}	2/0.18

The voltage of the series inverter, which is supplied from the regulator, is considered as 1 V.

The power dissipation variations of the BGR block versus the input voltage, which comes from the distance between tag and reader, are shown in Figure 5. When the limiter is deactivated ($V_{in} < V_{Lim}$), the power dissipation of the BGR is lower than 220 pW.

Figure 6 shows the variation of the power consumption of the voltage comparator block versus the variation of the input voltage. When the limiter is off ($V_{in} < V_{Lim}$), the power consumption is 1300 pW.

Figure 7 shows I-V characteristic of the limiter when V_m (output of voltage comparator circuit) and V_{NOT4} (output of fourth inverter circuit) voltages are employed at the gate of the M_L transistor. In the ideal case when the limiter starts at the desired input voltage, the drawing current that is created for protecting the tag is infinite. For the correct performance of the limiter and for making the proposed limiter's characteristic close to the ideal one, four stage inverters are used after the output of the comparator to produce the appropriate voltage level at the output of the fourth inverter after the limiter starts its work. Finally, by employing this output at the gate of transistor ML, the characteristic curve is almost equal to the ideal one. By increasing the number of inverters, the characteristic curve reaches the ideal curve, but the circuit dissipates more power.

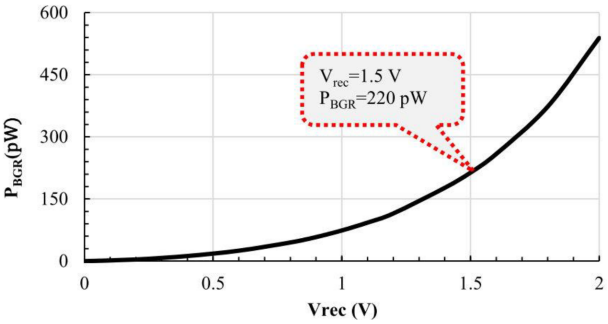

Figure 5. The power dissipation curve of the BGR circuit versus the input voltage variations.

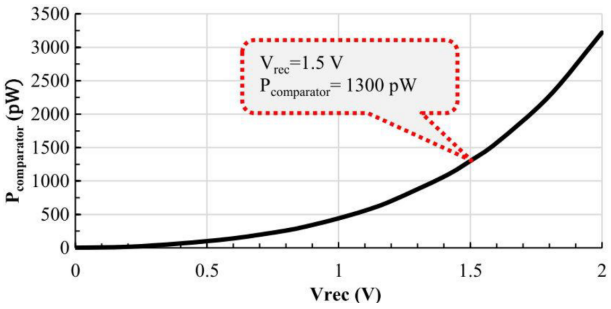

Figure 6. The variation of power consumption of the voltage comparator block versus the input voltage.

Therefore, four inverters are used to make a tradeoff between the power dissipation and having a near-ideal characteristic curve. In this condition the output is confined to 1.5 V and consequently prevents the damage of the tag subblocks.

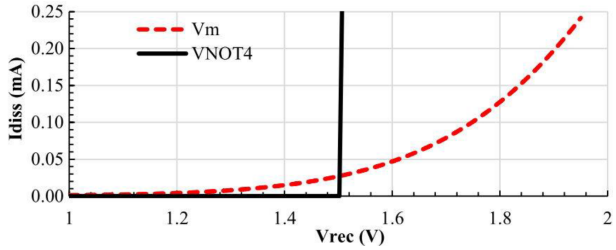

Figure 7. I-V characteristic of the voltage limiter when V_m and V_{NOT4} are employed to the gate of M_L.

The power dissipation curve of the proposed limiter, related to the V_{rec} variations in the range of 1–2 V, is shown in Figure 8 for schematic and postlayout simulation. The total power dissipation of the limiter block is due to the power dissipation of V_{rec} and V_{reg} supply voltages. Figure 8a presents the power dissipation of V_{rec}, which is about 2.14 nW and 2.16 nW at 1.5 V of V_{Lim} for schematic and postlayout simulation, respectively. Figure 8b shows the power dissipation of V_{reg}, which is about 27.14 nW and 30.12 nW at the limiter voltage for schematic and postlayout simulation, respectively. Therefore, the power dissipations of the proposed limiter for schematic and postlayout simulations are 31.56 nW and 32.28 nW, respectively, which are very low compared to the power dissipation of the RFID tag and can be ignored. In the postlayout simulation, despite schematic simulation, the parasitic capacitors and resistors of the circuit elements affect the simulation of the circuit. The simulations are done considering the parasitic capacitors and resistors. The difference of Figures 8a and 8b is related to the parasitic elements. The parasitic elements are more effective during the variation of input voltage level and starting time of the limiter. The pulse behavior and creation of two different slopes in Figures 8a and 8b are due to the parasitic elements, which culminate in the high leakage of current during the starting time of the limiter.

The variation of the limited voltage based on the temperature variation in the range of –20 °C to 70 °C is shown in Figure 9. In the mentioned temperature range the voltage variation is ± 0.043 V and the temperature coefficient is 322.22 ppm/°C. The average of current dissipation is about 34.22 nA in this temperature range and 31.56 nA at room temperature.

Figure 10 shows the Monte Carlo simulation of the limited voltage due to the process variation and

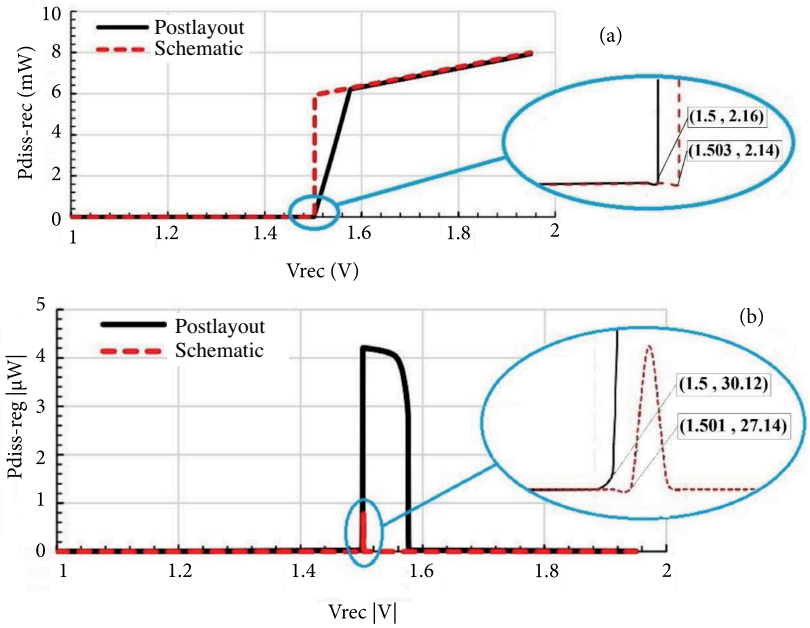

Figure 8. The power dissipation curve versus V_{rec} variations in the range of 1–2 V for (a) V_{rec} supply voltage, (b) V_{reg} supply voltage.

mismatch for 100 runs. The mean value (μ) and the standard deviation (σ) of this simulation are 1.45 V and 0.1 V, respectively; therefore, the coefficient of variation (σ / μ) is 6.9%.

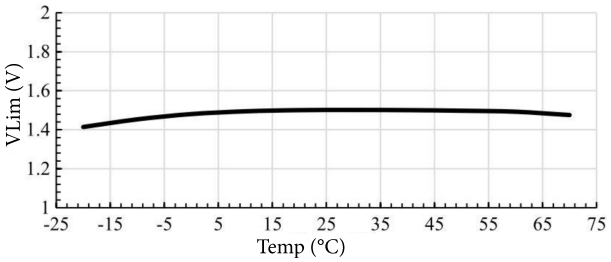

Figure 9. The limited voltage variation versus the temperature variation.

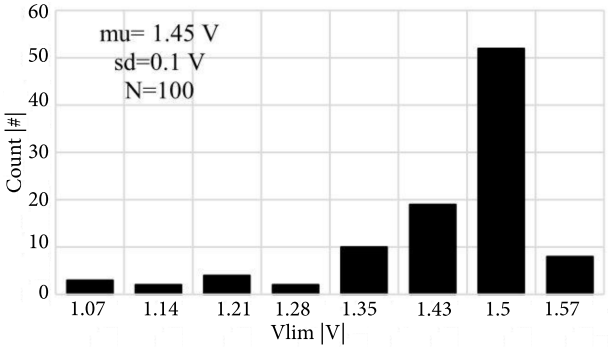

Figure 10. Monte Carlo simulation of the limited voltage for 100 runs.

The layout of the proposed DC limiter is shown in Figure 11. This figure is separated based on subblocks shown in Figure 2 and the proposed limiter layout is measured at about 1936 μm^2.

Table 2 compares the proposed limiter with the other designed circuit. The current consumption of the proposed limiter is significantly lower than that of other references. On the other hand, the chip area of the layout is lower than that of other designs and the other parameters are acceptable.

6. Conclusion

In this paper a low-power DC limiter is designed. The used blocks in this circuit are designed with MOSFET transistors and all of the transistors work in the subthreshold region. In this design the limited voltage is

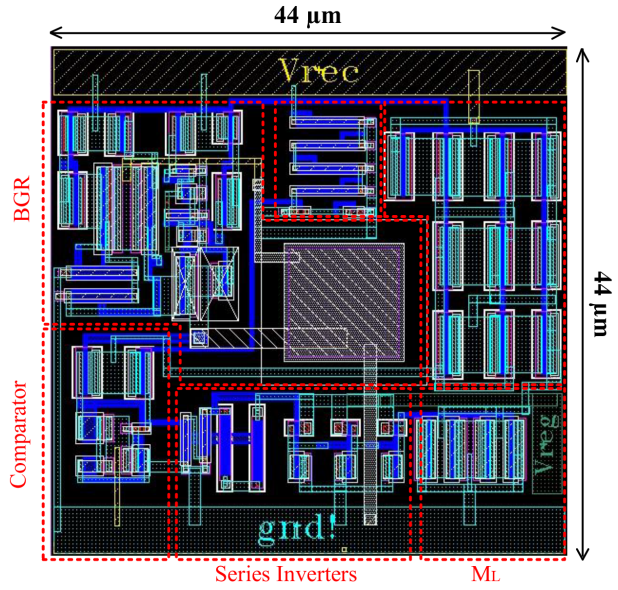

Figure 11. The layout of the complete proposed voltage limiter.

Table 2. The comparison of the proposed limiter with the other designed circuit.

[17]*	[16]	[3]	This work	
0.18	0.18	0.35	0.18	Technology [μm]
2	2	2.9	1.5	Voltage limiting [V]
2250	120	150	31.56	Current consumption [nA]
[–40 to 125]	[–20 to 80]	[35 to 45]	[–20 to 70]	T. range [°C]
40,600	8832	–	1936	Chip area [μm^2]

*Total of energy harvest chain.

considered about 1.5 V and the power and current consumption at this voltage are 32.28 nW and 31.56 nA, respectively. The output voltage variation of the limiter is very insignificant compared with the temperature variation and its temperature coefficient is 322.22 ppm/°C. In addition, the chip area of the proposed limiter is 1936 μm^2.

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