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Wide bandwidth CMOS four-quadrant mixed mode analogue multiplier using a second generation current conveyor circuit

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Abstract: This paper presents a new realization for a CMOS four-quadrant analogue multiplier. The proposed circuit is composed of three second generation current conveyor circuits (CCII), two NMOS transistors operating in the linear region, and four passive resistances. It can be operated in current mode and voltage mode without changing the circuit topology. The simulations results of the proposed mixed mode multiplier are verified by TSPICE simulator based on the BSIM3v3 transistor model for TSMC 0.18 μm CMOS process available from MOSIS at 25 °C with $\pm$0.8 V supply voltage. Through the use of resistive compensation with different passive resistance values, the voltage mode responses present $\pm$0.25 V dynamic range with THD less than 0.114% and wide bandwidth extended from 3.42 GHz to 4.1 GHz. The current mode responses show $\pm$150 μA dynamic range with a maximum THD value about 0.083% and large bandwidth expanded from 2.67 GHz to 3.12 GHz.

Key words: Multiplier, CCII, mixed mode, four-quadrant, accuracy, resistive compensation technique

1. Introduction

Analogue multipliers are considered a basic building block widely used in many systems and applications. They can be found in adaptive filters, frequency doublers, modulators, demodulators, automatic gain, controlling artificial neural networks, image processing, and fuzz logic controllers. This device has generally two inputs (X, Y) and a single output (Z). The relationship between input–output terminals is given as Z = K X Y, where K is a constant with suitable dimension. The multiplier circuits are classified into three groups depending on the operating mode. It can be configured in voltage mode, current mode, or mixed mode and it can be functioned in one-quadrant, two-quadrant [1–3], or four-quadrant [4–11].

In the literature, a variety of multiplier circuits using active elements such as current conveyor (CC) [12–17], operational trans-conductance amplifier (OTA) [18,19], and operational amplifier (Op-amp) [20,21] have received a considerable attention thanks to their good features, namely high accuracy, large dynamic range, wide bandwidth, small active chip area, and low power consumption.

In this paper, a new configuration of a CMOS four-quadrant mixed mode analogue multiplier circuit composed of three second generation current conveyor circuits, two NMOS transistors operating in the linear region, and four passive resistances is proposed. In the order to improve its bandwidth, a resistive compensation technique is used at the level of all current mirrors of CCII. The TSPICE simulator based on the BSIM3v3 transistor model (level 49) for TSMC 0.18 μm CMOS process available from MOSIS has been used to verify the

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simulation results of the proposed CCII circuit and multiplier circuit. The second generation current conveyor circuit CCII is characterized by large dynamic range with an excellent accuracy, high output impedance at Z and Y terminals, a low input impedance at X terminal ($R_X = 14.79\ \Omega$), and unity voltage and current gains. According to different values of resistance compensation, the voltage and current mode bandwidths are extended respectively from 4.23 GHz to 5.66 GHz and from 3.91 GHz to 4.95 GHz with 290 μW power consumption. The proposed multiplier is simulated with the same simulation conditions of CCII. The DC simulation results present large dynamic ranges of $\pm$250 mV with THD less than 0.114% in voltage mode and $\pm$150 μA with a maximum THD value about 0.083% in current mode. The AC simulation results show wide bandwidths extended from 3.42 GHz to 4.1 GHz in voltage mode and from 2.67 GHz to 3.12 GHz in current mode.

2. Bandwidth aspects in second generation current conveyors

2.1. Resistive compensation technique

The use of wide bandwidth integrated circuits is required for numerous applications operating at high frequency. In the order to reuse the classic circuit structures and to make it adaptive for technological development, the designers usually use the resistive compensation technique by integrating a passive resistance between the gate and drain of each primary transistor pair of the current mirror.

The simple current mirror circuit and their equivalent schema are presented in Figure 1. The relationship between input and output current is given in (1). By considering that the transistors M1 and M2 are identical ($C_{gs1} = C_{gs2} = C_{gs}$, $r_{o1} = r_{o2} = r_o$, $g_{m1} = g_{m2} = g_m$) and the hypothesis given in (2) is verified, the transfer function became under the form of first order filter (3), whose bandwidth depends on trans-conductance (g_m) and gate-source capacitance (C_{gs}) [22–24].

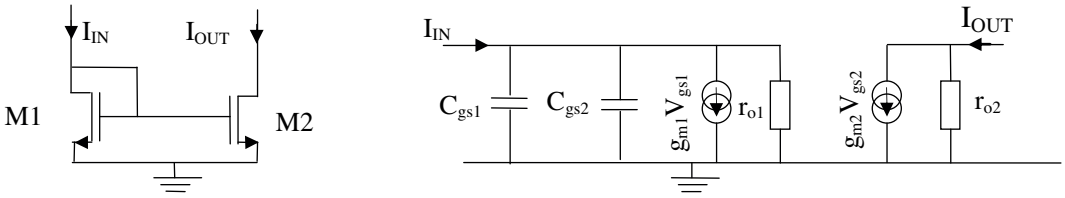

Figure 1. Simple current mirror and their equivalent schema.

$$\frac{I_{OUT}}{I_{IN}} = \frac{g_m r_o + 1}{s2r_o C_{gs} + g_m r_o + 1} \tag{1}$$

$$r_o g_m >> 1 \tag{2}$$

$$\frac{I_{OUT}}{I_{IN}} = \frac{1}{s\frac{2}{g_m} C_{gs} + 1} \tag{3}$$

The pulsation and cutoff frequency expressions are given by

$$\omega_o = \frac{g_m}{2C_{gs}} \quad f_o = \frac{g_m}{4\pi C_{gs}}$$

The simple current mirror with a passive resistance R added between the two gates of M1 and M2 transistors and their equivalent schema are presented in Figure 2.

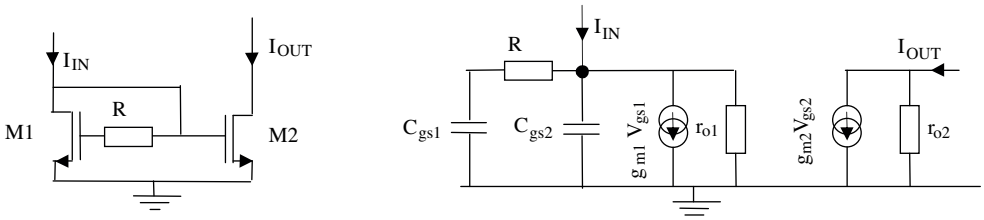

Figure 2. Current mirror circuit with resistance compensation and their equivalent schema.

The relationship between the input and output current of a simple current mirror with resistance compensation is given in (4). By using (2), the transfer function has become as shown in (5). This equation has two poles and one zero.

$$\frac{I_{OUT}}{I_{IN}} = \frac{(r_o g_m + 1)(sRC_{gs} + 1)}{s^2 R r_o C_{gs}^2 + s(R + 2r_o) C_{gs} + r_o g_m + 1} \tag{4}$$

$$\frac{I_{OUT}}{I_{IN}} = \frac{sRC_{gs} + 1}{s^2 \frac{R}{g_m} C_{gs}^2 + s\frac{(2r_o + R)}{r_o g_m} C_{gs} + 1} \tag{5}$$

By choosing $R = 1/g_m$, the zero is cancelled out by one of the poles. The pulsation and cutoff frequency expressions are given as follows:

$$\omega_o = \frac{g_m}{C_{gs}} \quad f_o = \frac{g_m}{2\pi C_{gs}}$$

The bandwidth of a simple current mirror with a resistive compensation technique is enhanced by a factor of two as compared to a simple current mirror.

2.2. Extended bandwidth of second generation current conveyor CCII

The CMOS realization of the second generation current conveyor circuit is presented in Figure 3. The input stage of the CCII circuit is composed of a symmetric operational transconductance amplifier (OTA) circuit formed by a PMOS differential pair (M1, M2) biased by M19 and three current mirrors, (M3, M4), (M5, M6), as well as (M7, M8).

Assuming that all transistors are operated in the saturation region and all the transistor pairs are matched, the voltage at terminal X follows successfully the voltage applied at terminal Y. The voltage offset is given by

$$\Delta V = V_X - V_Y \approx \lambda_p \left(V_{D1} \sqrt{\frac{2I_{D1}}{\mu_n C_{ox} \left(\frac{W}{L}\right)_1}} - V_{D2} \sqrt{\frac{2I_{D2}}{\mu_n C_{ox} \left(\frac{W}{L}\right)_1}} \right), \tag{6}$$

where λ_p is the channel length modulation parameter. (V_{D1},V_{D2}) and (I_{D1},I_{D2}) are the drain voltages and the drain currents of transistors M1 and M2.

It is clear that the offset voltage is null. The drain currents of transistors M1 and M2 are identical because the drains of transistors M7 and M8 are connected respectively to the drains of transistors M4 and M6.

The output stage composed of transistors M10 to M18 is constituted by two current mirrors and two offset adjustment. In the order to obtain good current follower responses between terminals X and Z, the dimensions of transistors must have been well calculated. The current mirror M11–M14 has the same characteristics than

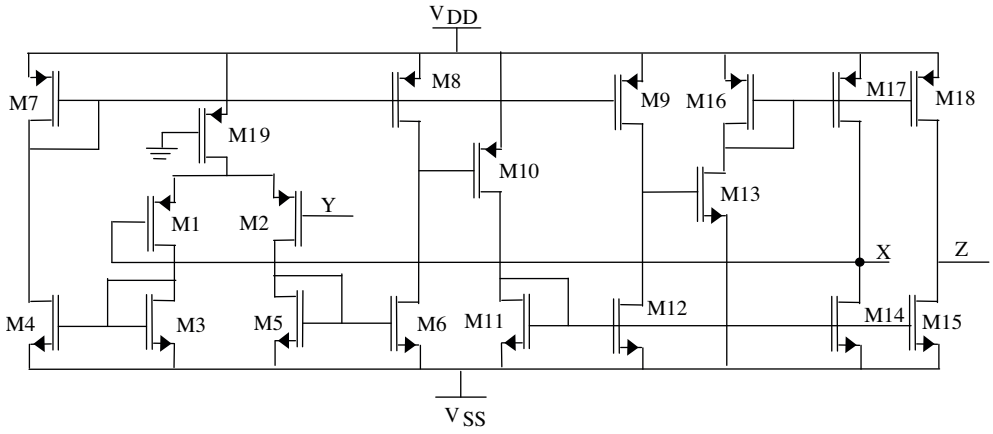

Figure 3. Proposed second generation current conveyor CCII circuit.

the two current mirrors M3–M4 and M5–M6 since the drain of transistor M9 is connected to the drain of transistor M12. Moreover, the connection of the two drain terminals of the transistors M17 and M13 makes it possible to have two identical current mirrors M7–M9 and M16–M18.

Considering that the transistors of NMOS and PMOS current mirrors are characterized by the same transconductance (g_{mN}, g_{mP}), same capacitor (C_{gsN}, C_{sgP}), and same resistance seen at the drain of transistor (r_N, r_P), the voltage transfer function of the proposed CCII is given by (7). It is in the form of standard normalized with thirteen poles and thirteen zeros (8).

$$A_V(s) = \frac{Vx}{Vy} = \frac{a_0 + a_1 s + a_2 s^2 + ... + a_{13} s^{13}}{b_0 + b_1 s + b_2 s^2 + ... + b_{13} s^{13}} \tag{7}$$

$$A_V(s) = A_0 \frac{\left(1 + \frac{s}{\omega_{Z1}}\right)\left(1 + \frac{s}{\omega_{Z2}}\right) .... \left(1 + \frac{s}{\omega_{Z13}}\right)}{\left(1 + \frac{s}{\omega_{P1}}\right)\left(1 + \frac{s}{\omega_{P2}}\right) ... \left(1 + \frac{s}{\omega_{P13}}\right)}, \tag{8}$$

where

- ω_{Z1}, ω_{Z2}, ..., ω_{Z13} denote the location of zeros,
- ω_{P1}, ω_{P2}, ..., ω_{P13} denote the location of poles,
- A_0 shows the gain of transfer function. It is equal to the ratio between a_0 and b_0.

Assuming widely separated zeros ($\omega_{Z1} << \omega_{Z2} << .. << \omega_{Z13}$), the coefficients of the numerator (s, s^2, s^3,..., s^{13}) can be approximated as

$$\frac{a_1}{a_0} \approx \frac{1}{\omega_{Z1}} \Rightarrow \omega_{Z1} \approx \frac{a_0}{a_1}$$

$$\frac{a_2}{a_0} \approx \frac{1}{\omega_{Z1}\omega_{Z2}} \Rightarrow \omega_{Z2} \approx \frac{a_1}{a_2}$$

$$\vdots$$

$$\frac{a_{13}}{a_0} \approx \frac{1}{\omega_{Z1}\omega_{Z2}\omega_{Z3}....\omega_{Z13}} \Rightarrow \omega_{Z13} \approx \frac{a_{12}}{a_{13}}$$

Similarly, assuming widely separated poles ($\omega_{P1} << \omega_{P2} <<...<< \omega_{P13}$), the coefficients of the denominator (s, s^2, ..., s^{13}) can be approximated as

$$\begin{aligned}
&\frac{b_1}{b_0} \approx \frac{1}{\omega_{P1}} \Rightarrow \omega_{P1} \approx \frac{b_0}{b_1} \\
&\frac{b_2}{b_0} \approx \frac{1}{\omega_{P1}\omega_{P2}} \Rightarrow \omega_{P2} \approx \frac{b_1}{b_2} \\
&\vdots \\
&\frac{b_{13}}{b_0} \approx \frac{1}{\omega_{P1}\omega_{P2}...\omega_{P13}} \Rightarrow \omega_{P13} \approx \frac{b_{12}}{b_{13}}
\end{aligned}$$

By substituting $s = j\omega$ and at $\omega = \omega_H$, the squared magnitude of transfer function is given by

$$|A(j\omega_H)|^2 = \frac{\left(1+\frac{\omega_H^2}{\omega_{Z1}^2}\right)\left(1+\frac{\omega_H^2}{\omega_{Z2}^2}\right)...\left(1+\frac{\omega_H^2}{\omega_{Z13}^2}\right)}{\left(1+\frac{\omega_H^2}{\omega_{P1}^2}\right)\left(1+\frac{\omega_H^2}{\omega_{P2}^2}\right)...\left(1+\frac{\omega_H^2}{\omega_{P13}^2}\right)} = \frac{1}{2} \tag{9}$$

The ω_H expression can be given by [25]

$$\omega_H \cong \frac{1}{\sqrt{\left(\frac{1}{\omega_{P1}^2}+...+\frac{1}{\omega_{P13}^2}\right) - 2\left(\frac{1}{\omega_{Z1}^2}+...+\frac{1}{\omega_{Z13}^2}\right)}} \tag{10}$$

By considering these approximations ($\omega_{P1} << \omega_{P2} <<...\omega_{P13}$ and $\omega_{P1} << \omega_{Z1} << \omega_{Z2}...<< \omega_{Z13}$), the cut-off frequency of CCII is roughly equal to the cut-off frequency of the first pole.

$$1 + \frac{\omega_H^2}{\omega_{P1}^2} = 2 \Rightarrow \omega_H = \omega_{P1} \Rightarrow f_H = f_{P1} \tag{11}$$

The bandwidth expression of CCII is given by

$$\omega_H = \frac{g_{mP}g_{mN}}{9g_{mP}g_{mN}r_{19}C_{sg2} + 4g_{mN}C_{sgP} + (g_{mN}+9g_{mP})C_{gsN}} \tag{12}$$

In the order to improve bandwidth, the resistive compensation technique was applied in all current mirrors of the proposed CCII. Assuming that all NMOS current mirrors are compensated by the same resistance value R_N and all PMOS current mirrors are compensated by the same resistance value R_P, the bandwidth expression of the second generation current conveyor using the resistive compensation technique is given by

$$\omega_H = \frac{g_{mN}^2 g_{mP} r_N^2 r_P^2}{\left[\begin{array}{l}(g_{mP}(9+R_P g_{mP}) + g_{mN}(R_P g_{mP} + R_P g_{mP} + 1))\, r_N^2 r_P^2 g_{mN} C_{gsN} \\ +9r_{19}r_N^2 r_P^2 g_{mN}^2 g_{mP} C_{sg1} + 4\left(r_N^2 r_P^2 g_{mN}^2 - g_{mP}R_N(r_N+r_P)^2\right)C_{sgP}\end{array}\right]} \tag{13}$$

Based on Eqs. (12) and (13), it is necessary that the resistances R_N and R_P verify the following relationship to have a wider bandwidth:

$$0 \leq R_P \leq \frac{4R_N(r_N+r_P)^2 C_{sgP}}{(g_{mP}+2g_{mN})r_N^2 r_P^2 g_{mN} C_{gsN}} \tag{14}$$

2.3. Simulation results of CCII

The performances of the CMOS second generation current conveyor circuit with and without using the resistive compensation technique are verified by TSPICE based on the BSIM3v3 transistor model (level 49) for the TSMC 0.18 μm CMOS process available from MOSIS at 25 °C. This circuit is powered with $\pm$0.8 V supply voltage. The aspect ratios (W/L) of the MOS transistors were taken as 5 μm/0.18 μm for M1, M2, and M19, 1 μm/0.18 μm for all NMOS transistors, and 2 μm/0.18 μm for all PMOS transistors.

In order to verify the theoretical analysis performed, we have extracted the transistor aspect ratios of CCII, as given in Table 1. The simulation results of the CCII circuit are verified with different resistance values R_N (5 kΩ, 10 kΩ, 20 kΩ, 30 kΩ, 40 kΩ) and R_P fixed to 10 Ω. In order to minimize the increase in temperature and surface, the passive resistance used for the resistive compensation technique is replaced by an active resistance under the form of an NMOS transistor (Ma) such that their drain and source terminals are connected to two gates of transistors M1a and M2a, as shown in Figure 4.

Table 1. The transistors aspect ratios of CCII.

	M1, M2	M19	M_N	M_P
Type	PMOS	PMOS	NMOS	PMOS
Region	Saturation	Linear	Saturation	Saturation
I_d	–45.08 μA	–90.18 μA	45.08 μA	–46.77 μA
I_{bs}, I_{bd}	0.	0.	0.	0.
V_{gs}	–646.72 mV	–800.00 mV	714.90 mV	–758.12 mV
V_{ds}	–731.83 mV	–153.20 mV	714.90 mV	–758.34 mV
V_{bs}	0.	0.	0.	0.
V_{TH}	–479.56 mV	–490.30 mV	494.93 mV	–475.31 mV
V_{DSAT}	–152.35 mV	–258.53 mV	159.60 mV	–235.87 mV
BETA	3.081 mV	2.98 mV	2.26 mV	1.21 mV
R_s, R_d	0.	0.	0.	0.
g_m	491.12 $\mu\Omega^{-1}$	386.64 $\mu\Omega^{-1}$	358.44 $\mu\Omega^{-1}$	291.98 $\mu\Omega^{-1}$
g_{ds}	18.66 $\mu\Omega^{-1}$	371.18 $\mu\Omega^{-1}$	13.33 $\mu\Omega^{-1}$	13.37 $\mu\Omega^{-1}$
g_{mb}	144.15 $\mu\Omega^{-1}$	126.71 $\mu\Omega^{-1}$	81.27 $\mu\Omega^{-1}$	87.36 $\mu\Omega^{-1}$
g_{bd}, g_{bs}	0.	0.	0.	0.
C_{gs}	7.083 fF	7.05 fF	1.75 fF	2.84 fF
C_{gd}	3.16 fF	3.51 fF	823.99 fF	1.26 fF
C_{gb}	231.54 aF	127.25 aF	109.80 aF	86.76 aF
C_{bd}, C_{bs}	0.	0.	0.	0.

The DC voltage mode and current mode characteristics of CCII are presented respectively in Figures 5 and 6. With different resistance values, we note that there is no change in these results. In voltage mode, the current conveyor circuit has good linearity over the rail to rail dynamic range (–0.8 V to 0.8 V) with 0.06% error at the end of the transfer curve. The output current characteristic curve vs. input current shows a maximum error of 0.012% for an input dynamic varied from –280 μA to 280 μA.

The AC voltage gains between Y and X are plotted in Figure 7. The static gains are equal to unity and the cut-off frequencies without and with resistance compensation are extended from 4.23 GHz to 5.66 GHz,

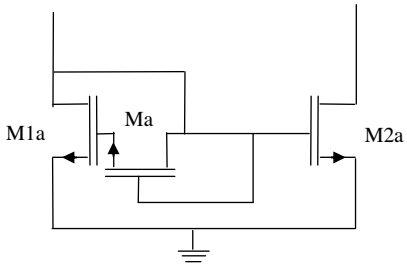

Figure 4. Simple current mirror with active resistance compensation.

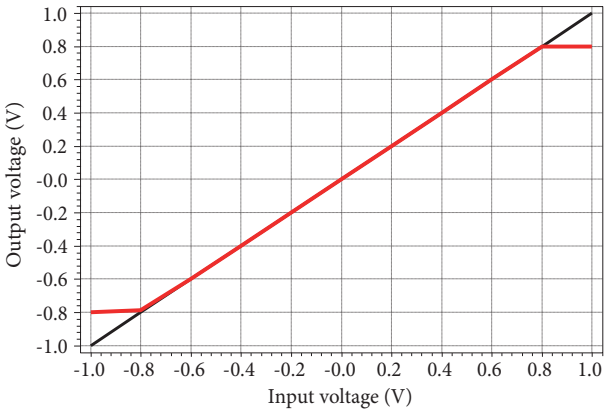

Figure 5. Output voltage variation as function of input voltage.

as noted in Table 2. The AC current gains between X and Z are shown in Figure 8. This circuit has unity static gains and the bandwidth values without and with resistance compensation are prolonged from 3.91 GHz to 4.95 GHz, as shown in Table 2. The parasitic resistances R_X keep the same values of 14.79 Ω and 3.07 Ω up to 100 MHz respectively for circuits CCII with passive and active resistance compensation (Figure 9). The main characteristics of the proposed second generation current conveyor circuit without and with resistance compensation are grouped in Table 3.

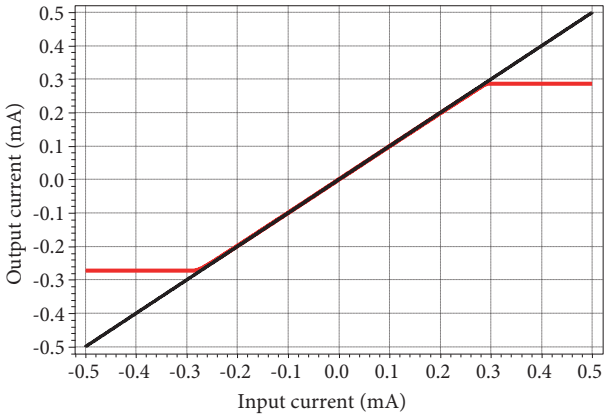

Figure 6. Output current variation as function of input current.

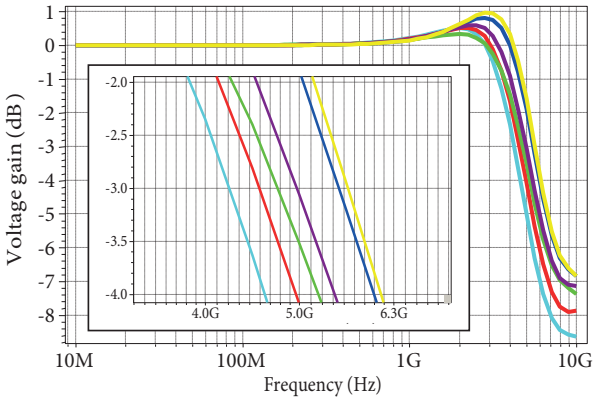

Figure 7. Voltage gain variation according to frequency.

3. Proposed mixed mode four-quadrant multiplier circuit

The proposed four-quadrant mixed mode multiplier is presented in Figure 10. This circuit is composed of three second generation current conveyor circuits, two N-Channel MOSFETs transistors, and four passive resistances.

The transistors M1 and M2 have the same drain and source terminals. Assuming that Eq. (15) is verified, the two NMOS transistors are operated in the linear region and the expression current drains are given in (16) and (17).

$$V_{GS} > \ V_{TH},\ V_{DS} < \ V_{GS} - V_{TN} \tag{15}$$

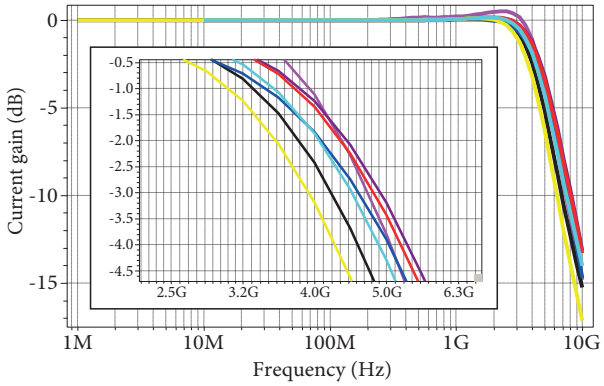

Figure 8. Current gain variation according to frequency.

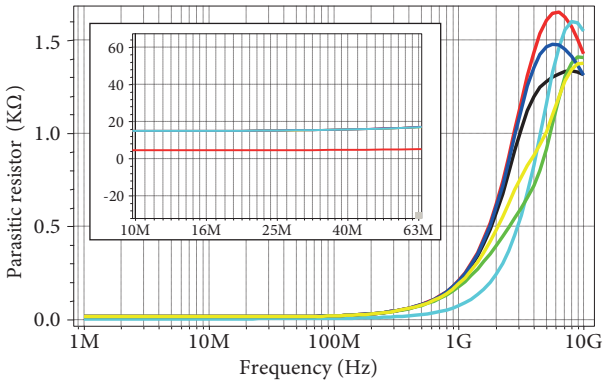

Figure 9. Parasitic resistance variation according to frequency.

Table 2. Bandwidth variation according to different resistance compensation values.

	Passive resistance R_N (kΩ)						Active resistance (μm/μm)
	0	5	10	20	30	40	R_P (30 μm/0.18 μm) R_N (5 μm/0.18 μm)
Bandwidth FCv (GHz)	4.22	4.54	4.98	5.52	5.64	5.66	5.18
Bandwidth FCi (GHz)	3.91	4.20	4.49	4.81	4.91	4.95	4.62
Parasitic resistance (Ω)	14.79	14.79	14.79	14.79	14.79	14.79	3.07

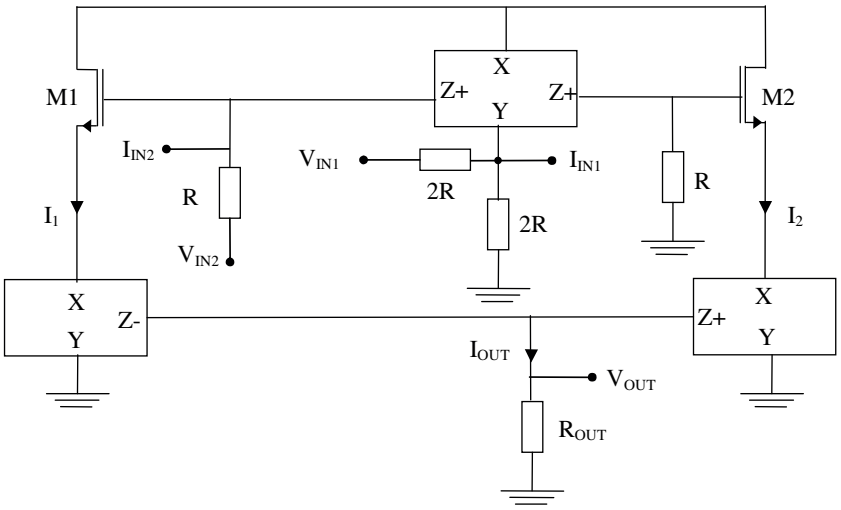

Figure 10. Proposed mixed mode four-quadrant analogue multiplier.

$$I_1 = K_1 \left(V_{GS1} - V_{TH1} - \frac{V_{DS1}}{2} \right) V_{DS1} \tag{16}$$

$$I_2 = K_2 \left(V_{GS2} - V_{TH2} - \frac{V_{DS2}}{2} \right) V_{DS2}, \tag{17}$$

where

Table 3. The comparison table.

Characteristics	Unit	Proposed CCII circuit		
		Without compensation	With compensation	
			Passive resistance R= 40 kΩ	Active resistance
Technology	CMOS	0.18 μm TSMC	0.18 μm TSMC	0.18 μm TSMC
Bias voltage	V	±0.8	±0.8	±0.8
Power consumption	mW	0.29	0.29	0.29
Voltage gain	—	1	1	1
Current gain	—	1	1	1
DC voltage range	V	–0.8 to 0.8	–0.8 to 0.8	–0.8 to 0.8
DC current range	mA	–0.28 to 0.28	–0.28 to 0.28	–0.28 to 0.28
Bandwidth FCi	GHz	3.9	4.95	4.62
Bandwidth FCv	GHz	4.23	5.66	5.18
THD at 10 kHz @ 0.3 V	%	0.023	0.03	0.026
THD at 10 kHz @ 10 μA	%	0.025	0.028	0.028
Node X parasitic impedance R_X	Ω	14.79	14.79	3.07
Node Y parasitic impedance R_Y, C_Y	kΩ//fF	∞//75	∞//77	∞//80
Node Z parasitic impedance R_Z, Cz	kΩ//fF	48.5// 16.59	50//17.3	52//18.6

- $K = \mu_n\ C_{ox}$ (W/L) is trans-conductance parameter,
- μ_n is the effective surface mobility,
- C_{ox} is the gate oxide capacitance per unit area,
- V_{TH} is the threshold voltage of the MOS transistor and W/L is the transistor aspect ratio.

Supposing that M1 and M2 are homogeneous ($K_1 = K_2 = K$ and $V_{TH1} = V_{TH2} = V_{TH}$), the voltage mode operation of the multiplier circuit can be obtained when the input currents I_{IN1} and I_{IN2} are null. The current drain expressions of M1 and M2 are given as

$$I_1 = K\left(V_{gs1} - V_{TH} - \frac{V_{IN1}}{4}\right)\frac{V_{IN1}}{2} \tag{18}$$

$$I_2 = K\left(V_{gs2} - V_{TH} - \frac{V_{IN1}}{4}\right)\frac{V_{IN1}}{2} \tag{19}$$

Based on (18) and (19), the output voltage of multiplier circuit can be expressed by

$$V_{out} = R_{OUT}\,(I_1 - I_2) = \frac{K}{2}R_{OUT}\,V_{IN1}\,(V_{gs1} - V_{gs2}) \tag{20}$$

$$V_{out} = \frac{K}{2}R_{OUT}\,V_{IN1}V_{IN2} \tag{21}$$

The current mode operation of the multiplier circuit can be verified when the input voltages V_{IN1} and V_{IN2} are connected to the ground. The current drains of transistors M1 and M2 are respectively given by

$$I_1 = K \left(V_{gs1} - V_{TN} - R\frac{I_{IN1}}{2} \right) R\, I_{IN1} \tag{22}$$

$$I_2 = K \left(V_{gs2} - V_{TN} - R\frac{I_{IN1}}{2} \right) R\, I_{IN1} \tag{23}$$

The output current (I_{out}) of the proposed multiplier is given by

$$I_{out} = I_1 - I_2 = KR\, I_{IN1} (V_{gs1} - V_{gs2}) \tag{24}$$

$$I_{out} = I_1 - I_2 = KR^2\, I_{IN1} I_{IN2} \tag{25}$$

The performances of the four-quadrant CMOS mixed mode multiplier circuit are verified with the same simulation conditions of the second generation current conveyor CCII. The dimensions of transistors M1 and M2 are W = 20 μm and L = 0.7 μm. The passive resistance values R and R_{out} are equal to 10 kΩ.

The DC voltage mode characteristic curves of the proposed multiplier circuit are shown in Figure 11. The input voltage V_{IN1} varies from –0.4 V to 0.4 V and the input voltage V_{IN2} is changing from –0.20 V to 0.20 V with 0.04 V steps. The proposed circuit has a dynamic range extended from –0.25 V to 0.25 V with THD less than 0.114%.

Figure 12 shows simulated DC current mode transfer characteristics of the proposed multiplier, when input current I_{IN1} swept continuously from –300 μA to 300 μA while I_{IN2} varied from –100 μA to 100 μA with 30 μA steps. It can be observed that the linear range of output current is approximately $\pm$150 μA, where the maximum value of total harmonic distortion (THD) is about 0.083%.

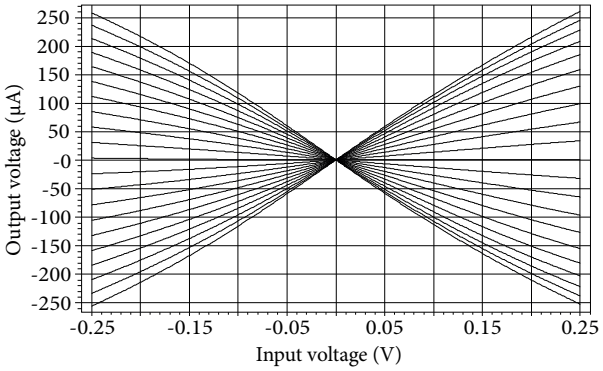

Figure 11. DC voltage mode transfer characteristics.

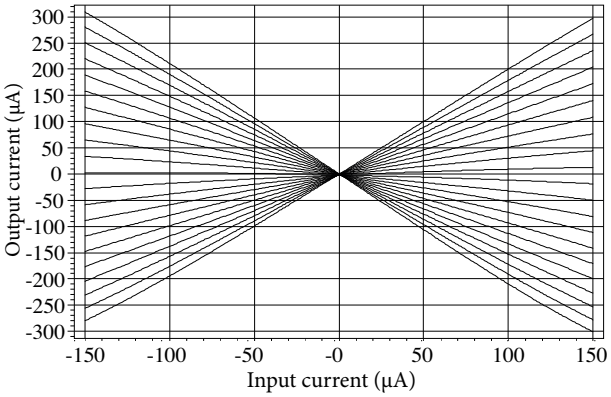

Figure 12. DC current mode transfer characteristics of four-quadrant analogue multiplier.

AC simulations have been carried out in order to verify the effects of the resistive compensation technique at the level of multiplier circuit. The voltage mode and current mode bandwidths are extended from 3.42 GHz to 4.1 GHz and from 2.67 GHz to 3.12 GHz, respectively, with resistance compensation values varied from 0 Ω to 40 kΩ, as shown in Figure 13.

The proposed multiplier is compared with several recently multiplier configurations existing in the literature, as shown in Table 4.

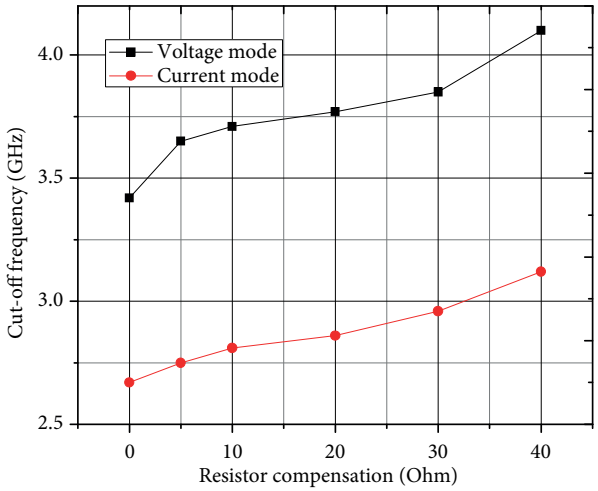

Figure 13. Bandwidth variation according to the resistance compensation values.

Table 4. Comparison between proposed multiplier and others reported in the literature.

	Public. years	Type	Supply voltage (V)	Power cons. (μW)	Dyn. range (μA, mV)		–3dB Freq. (GHz)	THD (%)	Tech. (μm)
[26]	2008	Voltage mode	±1	588	±100		3.98	—	0.18
[27]	2011	Voltage mode	1.2	192	±100		4.14	—	0.35
[28]	2014	Voltage mode	±1.25	402	—		—	1.62	0.25
[29]	2014	Current mode	1.5	700	±20		0.23	—	0.18
[30]	2008	Versatile dual mode	±1.5	460	VM	±300	0.019	—	0.5
					CM	±20			
Proposed work		Mixed mode	±0.8	527	VM	±200	4.1	0.114	0.18
					CM	±150	3.12	0.083	

4. Conclusion

This work presents a four-quadrant mixed mode multiplier circuit composed of three second generation current conveyor circuits, two NMOS transistors operating in linear region, and four passive resistances. It can be operated in either current mode or voltage mode without changing the circuit topology. In the order to improve the bandwidth of the proposed multiplier, the resistive compensation technique has applied by adding a resistance between the gate and drain of each primary transistor pair of all the current mirrors of the CCII. The performances of the proposed circuits were verified by TSPICE simulator based on the BSIM3v3 transistor model (level 49) for the TSMC 0.18 μm CMOS process available from MOSIS at 25 °C. The CCII circuit shows wide dynamic range, high output impedance at Z and Y terminals, excellent input impedance at X terminal ($R_X = 14.79\Omega$), and unity voltage and current gains. According to the different resistance compensation values, the voltage and current bandwidths are extended from 4.23 GHz to 5.66 GHz and from 3.91 GHz to 4.95 GHz, respectively, with 290 μW power consumption. The proposed multiplier has good voltage mode responses, where the dynamic range is ±0.25 V with THD less than 0.114% and the bandwidth values are extended from 3.42 GHz to 4.1 GHz. The current mode responses show wide dynamic range (±150 μA) with maximum value of THD of about 0.083% and the bandwidth values are expanded from 2.67 GHz to 3.12 GHz.

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