

Analysis and design of a converter based on noncascading structure

Sunil KUMAR^{1,*}, Kanwar Pal Singh RANA², Vineet KUMAR²

¹Department of Electronics and Communication Engineering, Bhagwant University, Ajmer, Rajasthan, India

²Division of Instrumentation and Control Engineering, Netaji Subhas Institute of Technology, Dwarka, New Delhi, India

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Abstract: In the present work, a converter employing two noncascading structures, combined in a single circuit, is presented. The power stored by the storage element is transferred to two subconverters by means of two storage capacitors that complement each other. The stress on the main power switch is of interest as it reduces as the load falls, which in turn reduces the power loss. By means of the storage elements, the input power factor as well as the load transient response can be improved simultaneously. The overall efficiency is high because the amount of power processed twice decreases. There is no need for tradeoff between the input power factor and load transient response because both the capacitors can serve two purposes. The important feature of the circuit is that the capacitor voltages remain almost constant and reduce as the load decreases, which results in small variation in duty ratio with a fall in load and hence better utilization of the switch. As an illustration, a 65-W, 18.5-V circuit is presented.

Key words: Noncascading structure, isolation transformer, half line period, PI controller, power factor correction

1. Introduction

A noncascading structure of converters is attaining wide popularity as an alternative to the cascaded ones as the former are of much importance to improve the overall efficiency of a circuit. In this category, numerous configurations have been suggested as well as developed. In such a scheme, in general, an inductor, a capacitor, and a switch are used to divert the path of the power drawn from the main source. A series capacitor on the AC supply side of the converter was used in [1]. It, however, suffered from the drawback of large variation of the intermediate capacitor voltage with the load that increased the stress on the power switch drastically. Many noncascading structures are possible, as suggested in [2], by means of which a large number of new converters have been derived and are still being developed. A flyback cell, popularly known as a flyboost cell, can be successfully combined with various other configurations to develop new converters as suggested in [3]. It improves the efficiency as well as the input power factor of the converter. For lower input voltage as in the case of photovoltaic cells the output power and voltage can be stepped up as described in [4] by employing a flyback-forward converter, with the outputs combined in series. For simplifying the configurations of noncascading structures, as in [5], these are divided into different categories, which were given in [2]. In [6–8], various combinations of different topologies were presented. Employing these combinations, various new converters can be developed for different requirements. On the basis of noncascading structures, converters having high efficiency were presented in [9,10]. A signal flow graph, a new approach, was suggested in [11]

*Correspondence: sunilkumar5593@gmail.com

for deriving a model for a noncascading structure. In [12], a family of step-up converters was suggested using the noncascading structure. The work was further carried out in [13–15], mostly in continuous conduction mode. The outcome of all these studies was improvement in overall efficiency as compared to cases where the power is processed fully, i.e. the cascaded scheme. For a noncascading structure, the input power factor and load transient are to be addressed and a compromise is to be maintained between the two depending upon a particular case. In the present circuit the idea is to employ two storage elements in such a way as to achieve both the power factor as well as improved load transient. Furthermore, the ratio of power processed by the intermediate stages is independent of the variations in the load. Thus, for all values of the load, both of the elements behave in the same way. This means that the variation of the load does not lead to any variation in the stresses on the storage capacitors and thus on the main switch. The power factor and load transient response of the converter are almost the same. Such advantages of the present converter make the present scheme more suitable in many cases. Thus, there is a need to elaborate on this scheme that is achieved in the present work.

The rest of the paper is organized as follows. Following the introduction and survey in Section 1, the proposed converter and its operation are described in Section 2, while its complete analysis is presented in detail in Section 3. A mathematical model has been presented and the associated performance parameters are also defined in this section. The performance of the converter is evaluated through intensive simulation and results are presented in Section 4. Finally, the conclusions are drawn in Section 5.

2. Circuit description and its working

The proposed circuit, an extension of [1], is shown in Figure 1. Rectified output supplies the power to two subconverters through two storage capacitors, C_1 and C_2 . The power to the load is transferred by output inductance L_o and magnetizing inductor L_{m2} of transformer T_2 . Magnetizing inductor L_{m1} of transformer T_1 supplies the energy to C_1 and C_2 . The number of turns in the windings of T_1 is N_{11} , N_{21} , and N_{31} , while those in T_2 are N_{12} and N_{22} . A large output capacitor, C_o , removes the line frequency ripples in the output voltage. The complete operation of the circuit consists of the following six main stages:

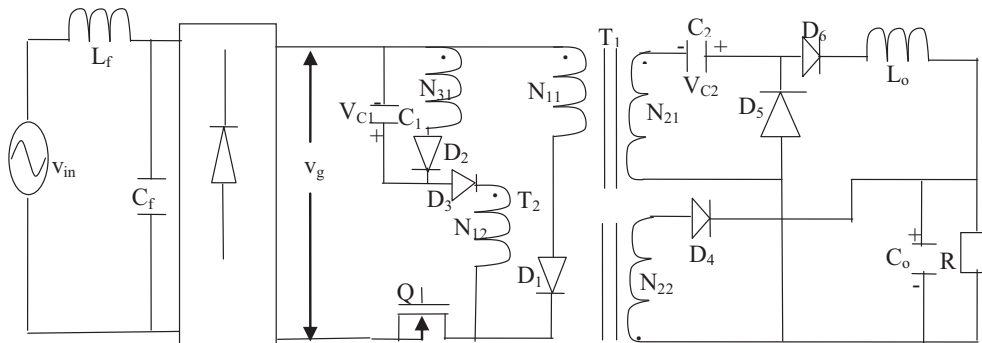


Figure 1. The proposed converter.

Stage 1 ($t_0 \leq t \leq t_1$): The main power switch Q turns on at $t = t_0$. As a consequence, all the inductors draw power from the input AC mains supply. At $t = t_1$, Q_1 turns off. The paths of the currents are v_g - C_1 - D_3 - N_{12} - Q - v_g , v_g - N_{11} - D_1 - Q - v_g , and N_{21} - C_2 - L_o -load- N_{21} .

Stage 2 ($t_1 \leq t \leq t_2$): L_o and L_{m2} discharge their energies to the load while L_{m1} discharges through C_1 . The current through C_1 decreases while that through C_2 increases. At $t = t_2$, the current through C_1 stops flowing. L_o is still discharging through the load. The paths of the currents are N_{31} - D_2 - C_1 - N_{31} , L_o -load- D_5 - L_o , and N_{22} - D_4 -load- N_{22} .

Stage 3 ($t_2 \leq t \leq t_3$): L_{m1} discharges through C_2 while L_{m2} transfers the power to the load. The current through L_{m2} stops at $t = t_3$. The currents follow the paths N_{21} - D_5 - C_2 - N_{21} , L_o -load- D_5 - L_o , and N_{22} - D_4 -load- N_{22} .

Stage 4 ($t_3 \leq t \leq t_4$): L_o supplies power to the load while L_{m1} discharges through C_2 . At $t = t_4$, L_o is completely discharged. The currents follow the paths N_{21} - D_5 - C_2 - N_{21} and L_o -load- D_5 - L_o .

Stage 5 ($t_4 \leq t \leq t_5$): At $t = t_5$, L_{m1} discharges its entire energy through C_2 through the path N_{21} - D_5 - C_2 - N_{21} .

Stage 6 ($t_4 \leq t \leq t_5$): The load draws power from C_o through C_o -R- C_o .

The main waveforms for the converter in a switching cycle are depicted in Figure 2.

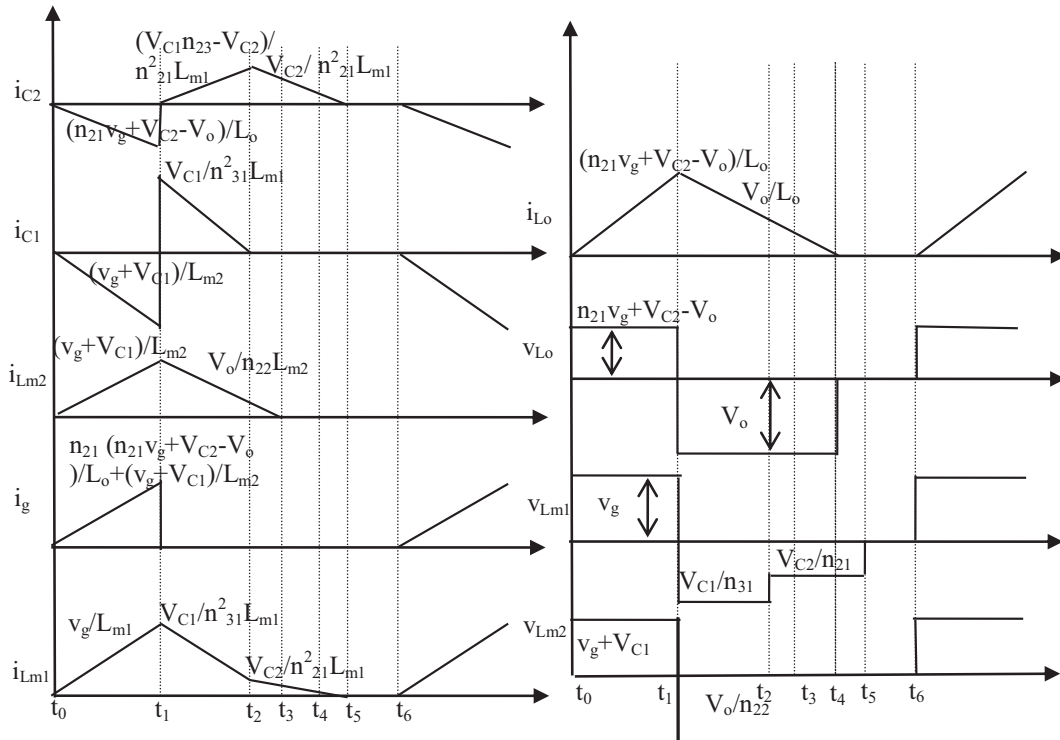


Figure 2. Associated waveforms.

3. Analysis of the circuit

Referring to Figure 2, the currents through the inductors, as Q is turned on, are given as:

$$i_{L_{m1}} = \frac{v_g}{L_{m1}}(t-t_0), \tag{1}$$

$$i_{L_o} = \frac{n_{21}v_g+V_{C2}-V_o}{L_o}(t-t_0), \tag{2}$$

where $n_{21} = N_{21}/N_{11}$ and

$$i_{L_{m2}} = \frac{v_g + V_{C1}}{L_{m2}}(t-t_0). \tag{3}$$

The peak values of currents given by Eqs. (1)–(3) are given as:

$$i_{L_{m_1pk}} = \frac{v_g}{L_{m_1}} (t_1 - t_0) = \frac{v_g}{L_{m_1}} d_1 T_s, \quad (4)$$

$$i_{L_{opk}} = \frac{n_{21}v_g + V_{C_2} - V_o}{L_o} d_1 T_s, \quad (5)$$

$$i_{L_{m_2pk}} = \frac{v_g + V_{C_1}}{L_{m_2}} d_1 T_s. \quad (6)$$

T_s is the switching period of Q. As it turns off at $t = t_1$, L_o and L_{m_2} discharge through the load while L_{m_1} discharges through C_1 . The currents are given as:

$$i_{L_{m_1}} = i_{L_{m_1pk}} - \frac{V_{C_1}}{n_{31}L_{m_1}} (t - t_1) - \frac{n_{23}V_{C_1} - V_{C_2}}{n_{21}L_{m_1}} (t - t_1), \quad (7)$$

$$i_{L_o} = i_{L_{opk}} - \frac{V_o}{L_o} (t - t_1). \quad (8)$$

L_{m_2} discharges through the load. Referring to the secondary side of T_2 ,

$$i_{L_{m_2s}} = \frac{i_{L_{m_2pk}}}{n_{22}} - \frac{V_o}{n_{22}^2 L_{m_2}} (t - t_1). \quad (9)$$

$n_{22} = N_{22}/N_{12}$. At $t = t_2$, the current through C_1 stops flowing. The average value of current through it in a switching period is given as:

$$\langle i_{C_1} \rangle_{T_s} = \left(-\frac{v_g + V_{C_1}}{2L_{m_2}} d_1^2 T_s + \frac{V_{C_1}}{2n_{31}^2 L_{m_1}} d_2^2 T_s \right). \quad (10)$$

The power transferred to C_1 in a half line period is given by:

$$\langle P_{C_1} \rangle_{T_L} = \frac{1}{\pi} \int_0^\pi \langle i_{C_1} \rangle_{T_s} V_{C_1} d(\omega t). \quad (11)$$

C_1 is lossless. Hence, from Eqs. (10) and (11),

$$d_2 = n_{31} d_1 \sqrt{\frac{L_{m_1} (\pi V_{C_1} + 2V_m)}{L_{m_2} \pi V_{C_1}}}. \quad (12)$$

The average current through C_2 in a switching period is given by:

$$\langle i_{C_2} \rangle_{T_s} = \left(-\frac{n_{21}v_g + V_{C_2} - V_o}{2L_o} d_1^2 + \frac{n_{23}V_{C_1} - V_{C_2}}{2n_{21}^2 L_{m_1}} d_2^2 + \frac{V_{C_2}}{2n_{21}^2 L_{m_1}} (d_3 + d_4 + d_5)^2 \right) T_s. \quad (13)$$

The power transferred to C_2 in a half line period is given as:

$$\langle P_{C_2} \rangle_{T_L} = \frac{1}{\pi} \int_{\theta_1}^{\pi - \theta_1} \langle i_{C_2} \rangle_{T_s} V_{C_2} d(\omega t). \quad (14)$$

In Eq. (13), the middle term is very small. Neglecting it and as C_2 is lossless, one gets

$$d_3 + d_4 + d_5 = n_{21}d_1\sqrt{\frac{(2n_{21}^2V_m^2 + (V_o - V_{C_2})(V_o - V_{C_2} - \pi n_{21}V_m))L_{m_1}}{L_oV_{C_2}\pi n_{21}V_m}}. \quad (15)$$

Volt-second balance for L_{m_1} yields

$$v_gd_1 = \frac{V_{C_1}}{n_{31}}d_2 + \frac{V_{C_2}}{n_{21}}(d_3 + d_4 + d_5). \quad (16)$$

From Eqs. (12), (15), and (16), under worst-case conditions,

$$V_m \cong \sqrt{\frac{(\pi V_{C_1} + 2V_m)L_{m_1}V_{C_1}}{\pi L_{m_2}}} + \sqrt{\frac{(2n_{21}^2V_m^2 + (V_o - V_{C_2})(V_o - V_{C_2} - \pi n_{21}V_m))L_{m_1}V_{C_2}}{\pi L_o n_{21}V_m}}. \quad (17)$$

The powers drawn by the storage capacitors from the main supply are transferred to the load as the switch turns on, which is given as:

$$\frac{d_1^2T_s}{\pi} \left(\frac{(\pi V_{C_1} + 2V_m)V_{C_1}}{2L_{m_2}} + \frac{(2n_{21}^2V_m^2 + (V_o - V_{C_2})(V_o - V_{C_2} - \pi n_{21}V_m))V_{C_2}}{2L_o n_{21}V_m} \right) = \frac{d_1^2T_s\pi V_m^2}{4\pi L_{m_1}}. \quad (18)$$

From Eqs. (17) and (18), equating the values of V_m ,

$$\frac{(\pi V_{C_1} + 2V_m)V_{C_1}}{L_{m_2}} = \frac{(2n_{21}^2V_m^2 + (V_o - V_{C_2})(V_o - V_{C_2} - \pi n_{21}V_m))V_{C_2}}{L_o n_{21}V_m}. \quad (19)$$

From Eqs. (17) and (19),

$$V_m = 2\sqrt{\frac{(\pi V_{C_1} + 2V_m)L_{m_1}V_{C_1}}{\pi L_{m_2}}} = 2\sqrt{\frac{(2n_{21}^2V_m^2 + (V_o - V_{C_2})(V_o - V_{C_2} - \pi n_{21}V_m))L_{m_1}V_{C_2}}{\pi L_o n_{21}V_m}}. \quad (20)$$

The total power drawn from the input AC supply is given as:

$$P_{in} = \frac{d_1^2T_s}{\pi} \left[\int_0^\pi \frac{v_g + V_{C_1}}{2L_{m_2}} + \int_{\theta_1}^{\pi - \theta_1} \frac{n_{21}(n_{21}v_g + V_{C_2} - V_o)}{2L_o} \right] v_g d(\omega t), \quad (21)$$

where $\theta_1 = \sin^{-1}(V_o - V_{C_2})/n_{21}V_m$. On simplifying Eq. (21),

$$P_{in} = \frac{d_1^2T_s}{4\pi} \left(\frac{\pi V_m^2 + 4V_mV_{C_1}}{L_{m_2}} + \frac{4\pi n_{21}^3V_m^3 - 26n_{21}^2V_m^2(V_o - V_{C_2}) + (V_o - V_{C_2})^3}{4n_{21}V_mL_o} \right). \quad (22)$$

3.1. Discontinuous conduction mode (dcm)

For the inductors to conduct in discontinuous mode, the conditions are

$$d_1 + d_2 + d_3 < 1; \quad d_1 + d_2 + d_3 + d_4 < 1 \text{ and } d_1 + d_2 + d_3 + d_4 + d_5 < 1. \quad (23)$$

Equating the volt-second product for L_{m2} , L_o , and L_{m1} ,

$$(v_g + V_{C1})d_1 = \frac{V_o(d_2 + d_3)}{n_{22}}, \quad (24)$$

$$(n_{21}v_g + V_{C2} - V_o)d_1 = V_o(d_2 + d_3 + d_4), \quad (25)$$

$$v_g d_1 = \frac{V_{C1}d_2}{n_{31}} + \frac{V_{C2}(d_3 + d_4 + d_5)}{n_{21}}. \quad (26)$$

From Eqs. (23)–(25),

$$n_{22} < \frac{(1 - d_1)V_o}{d_1(v_g + V_{C1})}, \quad (27)$$

$$n_{21} < \frac{(V_o - d_1V_{C2})}{d_1v_g}. \quad (28)$$

From Eqs. (12), (15), (20), and (23),

$$\frac{1}{d_1} \geq \frac{(n_{31}V_m + V_{C1})V_{C2}}{(2V_{C2} - V_o)V_{C1}}. \quad (29)$$

It is evident from Eq. (29) that $V_{C2} > V_o/2$.

3.2. Selection of inductors

For L_o to operate in dcm, the condition is given by

$$L_o \leq (1 - d_{1max})R_{fw}T_s/2. \quad (30)$$

R_{fw} is the resistance equivalent to the power transferred to the load by the subconverter through transformer T_1 and d_{1max} is the maximum duty ratio of the main switch. Other inductors are selected by Eqs. (18) and (19).

3.3. Mathematical modeling

The model of the converter is developed for the switching cycle and half line cycle. As the inductors operate in dcm, the inductor currents are not the state variables. Thus, only three state variables, the capacitor voltages, exist. From the current waveforms of C_1 , its average current in a switching cycle is given as:

$$\langle I_{C1} \rangle_{T_s} = \frac{1}{T_s} (\text{total area}) = \frac{1}{T_s} \left(-\frac{(v_g + V_{C1})d_1T_s}{2L_{m2}}d_1T_s + \frac{V_o(d_2 + d_3)T_s}{2n_2^2L_m}(d_2 + d_3)T_s + d_4T_s \cdot 0 + d_5T_s \cdot 0 \right). \quad (31)$$

From Eqs. (20), (24), and (31),

$$C_1 \langle \frac{dv_{C1}}{dt} \rangle_{T_s} = \left(\frac{V_m^2}{8L_{m1}V_{C1}} - \frac{v_g + V_{C1}}{2L_{m2}} \right) d_1^2 T_s. \quad (32)$$

The average current in a half line period is

$$C_1 \langle \frac{dv_{C1}}{dt} \rangle_{T_L} = \frac{d_1^2 T_s}{\pi} \int_0^\pi \left(\frac{V_m^2}{8L_{m1}V_{C1}} - \frac{v_g + V_{C1}}{2L_{m2}} \right) d(\omega t). \quad (33)$$

Simplifying Eq. (33),

$$\left\langle \frac{dv_{C_1}}{dt} \right\rangle_{T_L} = \frac{d_1^2 T_s}{\pi C_1} \left(\frac{\pi V_m^2}{8L_{m_1} V_{C_1}} - \frac{2V_m + \pi V_{C_1}}{2L_{m_2}} \right). \quad (34)$$

In a similar manner, the average current in the switching period through C_2 is given by:

$$C_2 \left\langle \frac{dv_{C_2}}{dt} \right\rangle_{T_s} = \left(\frac{V_m^2}{8L_{m_1} V_{C_2}} - \frac{n_{21} v_g + V_{C_2} - V_o}{2L_o} \right) d_1^2 T_s. \quad (35)$$

From Eq. (35), the average current in a half line period is given by:

$$C_2 \left\langle \frac{dv_{C_2}}{dt} \right\rangle_{T_L} = \frac{d_1^2 T_s}{\pi} \left[\int_0^\pi \left(\frac{V_m^2}{8L_{m_1} V_{C_2}} - \int_{\theta_1}^{\pi-\theta_1} \frac{n_{21} v_g + V_{C_2} - V_o}{2L_o} \right) d(\omega t) \right]. \quad (36)$$

Simplifying Eq. (36),

$$\left\langle \frac{dv_{C_2}}{dt} \right\rangle_{T_L} = \frac{d_1^2 T_s}{\pi C_2} \left(\frac{\pi V_m^2}{8L_{m_1} V_{C_2}} - \frac{2n_{21}^2 V_m^2 + (V_o - V_{C_2})(V_o - V_{C_2} - \pi n_{21} V_m)}{2L_o n_{21} V_m} \right). \quad (37)$$

The current averaged over a switching cycle through output filter capacitor C_o is given as:

$$C_o \left\langle \frac{dv_{C_o}}{dt} \right\rangle_{T_s} = \frac{n_{21} v_g + V_{C_2} - V_o}{2L_o} d_1^2 T_s + \frac{V_o}{2L_o} (d_2 + d_3 + d_4)^2 T_s + \frac{V_o}{2n_{22}^2 L_{m_2}} (d_2 + d_3)^2 T_s - \frac{V_o}{R}, \quad (38)$$

$$C_o \left\langle \frac{dv_{C_o}}{dt} \right\rangle_{T_s} = -\frac{V_o}{R} + \frac{d_1^2 T_s}{2V_o} \left(\frac{(n_{21} v_g + V_{C_2} - V_o)(n_{21} v_g + V_{C_2})}{L_o} + \frac{v_g^2}{L_{m_2}} \right). \quad (39)$$

The current through C_2 in a half line period is given as:

$$C_o \left\langle \frac{dv_{C_o}}{dt} \right\rangle_{T_L} = -\frac{V_o}{R} + \frac{d_1^2 T_s}{2V_o \pi} \left[\int_{\theta_1}^{\pi-\theta_1} \frac{(n_{21} v_g + V_{C_2} - V_o)(n_{21} v_g + V_{C_2})}{L_o} + \int_0^\pi \frac{v_g^2}{L_{m_2}} \right] d(\omega t). \quad (40)$$

Simplifying Eq. (40),

$$\begin{aligned} \left\langle \frac{dv_{C_o}}{dt} \right\rangle_{T_L} &= -\frac{V_o}{RC_o} + \frac{d_1^2 T_s}{2\pi V_o C_o} \left(\frac{(\pi n_{21} V_m - 2(V_o - V_{C_2}))(n_{21}^2 V_m^2 - 2V_{C_2}(V_o - V_{C_2}))}{2n_{21} V_m L_o} \right. \\ &\quad \left. + \frac{(2n_{21}^2 V_m^2 - (V_o - V_{C_2})^2)(8.5V_{C_2} - 4.5V_o)}{2n_{21} V_m L_o} + \frac{\pi V_m^2}{4L_{m_2}} \right). \end{aligned} \quad (41)$$

By introducing small perturbations in all the variables $v_m, d_1 = d, V_{C_1} = x_1, V_{C_2} = x_2, V_{C_o} = x_3,$ and $V_o = x_3:$

$$v_m = \tilde{v}_m + V_m, d = \tilde{d} + D, x_1 = \tilde{x}_1 + X_1, x_2 = \tilde{x}_2 + X_2, x_3 = \tilde{x}_3 + X_3, v_o = \tilde{v}_o + V_o \text{ such that } \tilde{v}_m \ll V_m \text{ etc.} \quad (42)$$

The capital letters denote DC or constant values of the variables. By Taylor series expansion of Eqs. (34), (37), and (41):

$$\begin{bmatrix} \dot{\tilde{x}}_1 \\ \dot{\tilde{x}}_2 \\ \dot{\tilde{x}}_3 \end{bmatrix} = \begin{bmatrix} a_{11} & a_{12} & a_{13} \\ a_{21} & a_{22} & a_{23} \\ a_{31} & a_{32} & a_{33} \end{bmatrix} \begin{bmatrix} \tilde{x}_1 \\ \tilde{x}_2 \\ \tilde{x}_3 \end{bmatrix} + \begin{bmatrix} b_{11} & b_{12} \\ b_{21} & b_{22} \\ b_{31} & b_{32} \end{bmatrix} \begin{bmatrix} \tilde{d} \\ \tilde{v}_m \end{bmatrix}. \quad (43)$$

In Eq. (43),

$$\begin{aligned}
 a_{11} &= \frac{D^2 T_s}{2L_{m_2} C_1}; a_{12} = 0; a_{13} = 0; a_{21} = 0; a_{22} = \frac{D^2 T_s (X_2 - X_3 + n_{21} \pi V_m)}{2\pi C_2 L_o n_{21} V_m}; a_{23} \\
 &= \frac{-D^2 T_s (X_2 - X_3 + n_{21} \pi V_m)}{2\pi C_2 L_o n_{21} V_m}; a_{31} = 0; a_{32} = \frac{D^2 T_s (2n_{21}^2 V_m^2 + X_2 X_3 - 5X_2^2)}{4\pi n_{21} V_m C_o V_o L_o}; a_{33} \\
 &= \frac{D^2 T_s (5X_3^2 + 2X_2^2 - 11X_2 X_3 - 2n_{21}^2 V_m^2)}{4\pi n_{21} V_m C_o V_o L_o}; b_{11} = \frac{D T_s}{4\pi C_1} \left(\frac{\pi V_m^2}{X_1 L_{m_1}} - \frac{8V_m + X_1}{L_{m_2}} \right); b_{12} \\
 &= \frac{D^2 T_s}{8\pi C_1} \left(\frac{2\pi V_m}{X_1 L_{m_1}} - \frac{8}{L_{m_2}} \right); b_{21} = \frac{2D T_s}{\pi C_2} \left(\frac{\pi V_m^2}{8X_2 L_{m_1}} - \frac{2n_{21}^2 V_m^2 + (X_3 - X_2)(X_3 - X_2 - \pi n_{21} V_m)}{2L_o n_{21} V_m} \right); b_{22} \\
 &= \frac{D^2 T_s}{\pi C_2} \left(\frac{2\pi V_m}{8X_2 L_{m_1}} - \frac{4n_{21}^2 V_m - \pi n_{21} (X_3 - X_2)}{2L_o n_{21} V_m} \right); b_{31} \\
 &= \frac{D T_s}{4\pi C_o V_o} \left(\frac{n_{21}^2 V_m^2 (2\pi n_{21} V_m + 22X_2 - 14X_3) - 4\pi n_{21} V_m X_2 (X_3 - X_2) + (X_3 - X_2)^2 (5X_3 - X_2)}{L_o n_{21} V_m} + \frac{\pi V_m^2}{L_{m_2}} \right); b_{32} \\
 &= \frac{D^2 T_s}{4\pi C_o V_o} \left(\frac{\pi n_{21}^3 V_m^2 - 2\pi n_{21} X_2 (X_3 - X_2) + 2\pi n_{21}^2 V_m^2 - 4n_{21} V_m (X_3 - X_2) - 2n_{21}^2 V_m (5X_3 - 9X_2)}{L_o n_{21} V_m} + \frac{\pi V_m}{L_{m_2}} \right). \tag{44}
 \end{aligned}$$

The output voltage is given as:

$$[\tilde{v}_o] = [0 \quad 0 \quad 1] \begin{bmatrix} \tilde{x}_1 \\ \tilde{x}_2 \\ \tilde{x}_3 \end{bmatrix}. \tag{45}$$

By taking the Laplace transform of Eq. (43), and simplifying the expressions afterwards,

$$\tilde{x}_3(s) = \frac{((s - a_{22})b_{31} + a_{32}b_{21})\tilde{d} + ((s - a_{22})b_{32} + a_{32}b_{22})\tilde{v}_m}{(s - a_{22})(s - a_{33}) - a_{32}a_{23}}. \tag{46}$$

From Eq. (46), the control to output transfer function is given by

$$\left. \frac{\tilde{v}_o(s)}{\tilde{d}(s)} \right|_{\tilde{v}_m=0} = \frac{(s - a_{22})b_{31} + a_{32}b_{21}}{(s - a_{22})(s - a_{33}) - a_{32}a_{23}}. \tag{47}$$

The input to output transfer function is given by

$$\left. \frac{\tilde{v}_o(s)}{\tilde{v}_m} \right|_{\tilde{d}(s)=0} = \frac{(s - a_{22})b_{32} + a_{32}b_{22}}{(s - a_{22})(s - a_{33}) - a_{32}a_{23}}. \tag{48}$$

As a design example, a 65-W, 18.5-V converter is considered and the component values for the same are as given in Table 1. By substituting their values, the following expression is obtained for open loop gain:

$$\left. \frac{\tilde{v}_o(s)}{\tilde{d}(s)} \right|_{\tilde{v}_m=0} = \frac{111s - 46287}{s^2 - 415s - 459}. \tag{49}$$

Table 1. Component value selection.

Symbol	Value and units	Description
V_{inrms}	220 V	Input voltage
f_s	50 k Hz	Switching frequency
D	0.38	Duty ratio
n_{21}	0.1:1	N_{21}/N_{11}
n_{31}	0.5:1	N_{31}/N_{11}
C_1	66 μ F	Intermediate capacitor
C_o	17600 μ F	Output capacitor
C_f	100 nF	Input filter capacitor
C_2	100 μ F	Intermediate capacitor
L_{m1}	2942 μ H	Magnetizing inductor
L_{m2}	3342 μ H	Magnetizing inductor
n_{22}	0.062:1	N_{22}/N_{12}
L_f	8 mH	Input filter inductor
L_o	30 μ H	Output filter inductor

The Bode diagram for Eq. (49) is depicted in Figure 3a. A controller, as defined below, is designed for regulating the output of the converter:

$$G_c(s) = (0.055 + \frac{2.2}{s}). \tag{50}$$

The Bode diagram of open loop gain of the converter including the controller is depicted in Figure 3b.

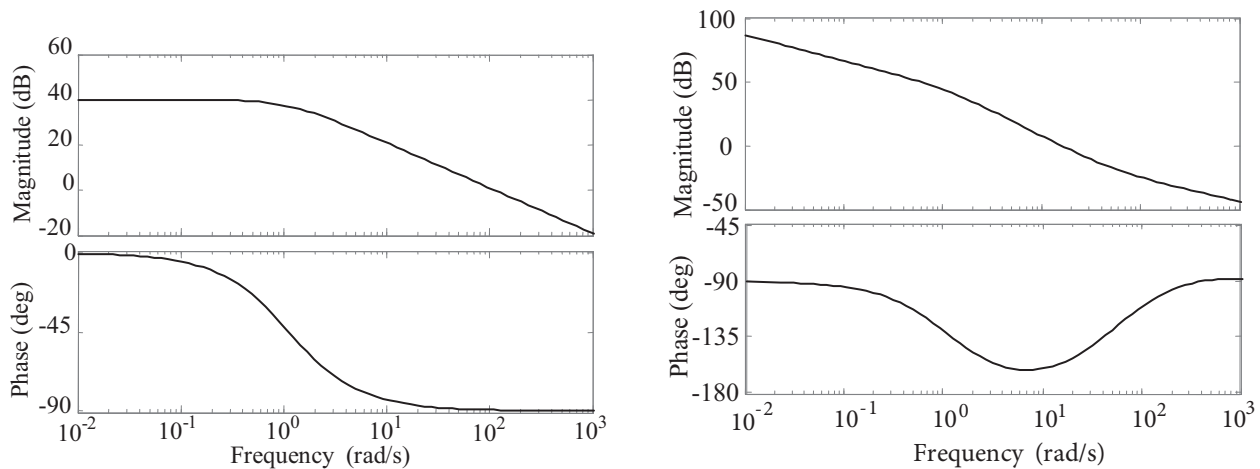


Figure 3. a) Bode diagram of control to output transfer function. b) Bode diagram of open loop gain of the converter with the controller.

3.4. Power transfer ratio

The input power is shared between the storage capacitors and the two subconverters. The energy stored in the magnetizing inductor of transformer T_1 is shared between C_1 and C_2 . Total input power drawn by L_{m1} from the input supply is given by Eq. (18). The ratios of power transferred to C_1 and C_2 are, respectively

$$\frac{P_{C_1}}{P_{L_{m_1}}} = \frac{\frac{d_1^2 T_s}{\pi} \left(\frac{(\pi V_{C_1} + 2V_m) V_{C_1}}{2L_{m_2}} \right)}{\frac{d_1^2 T_s \pi V_m^2}{4\pi L_{m_1}}} = \frac{2L_{m_1} (\pi V_{C_1} + 2V_m) V_{C_1}}{\pi L_{m_2} V_m^2} \quad (51)$$

and,

$$\frac{P_{C_2}}{P_{L_{m_1}}} = \frac{\frac{d_1^2 T_s (2n_{21}^2 V_m^2 + (V_o - V_{C_2})(V_o - V_{C_2} - \pi n_{21} V_m)) V_{C_2}}{2\pi L_o n_{21} V_m}}{\frac{d_1^2 T_s \pi V_m^2}{4\pi L_{m_1}}} = \frac{(2n_{21}^2 V_m^2 + (V_o - V_{C_2})(V_o - V_{C_2} - \pi n_{21} V_m)) 2L_{m_1} V_{C_2}}{n_{21} L_o \pi V_m^3}. \quad (52)$$

The ratio of power shared between the storage capacitors is

$$\frac{P_{C_2}}{P_{C_1}} = \frac{(2n_{21}^2 V_m^2 + (V_o - V_{C_2})(V_o - V_{C_2} - \pi n_{21} V_m)) L_{m_2} V_{C_2}}{n_{21} L_o V_m (\pi V_{C_1} + 2V_m) V_{C_1}}. \quad (53)$$

From Eq. (53), it is inferred that the ratio of powers transferred to the storage capacitors remains constant and is independent of variation in the load.

4. Simulation results

Through a resistive network of 7.5 k Ω and 2 k Ω , the output is controlled by using a reference of 3.89 V. The simulation results for the same are presented in Figures 4a–4j, employing MATLAB/Simulink. The input power is shared between the storage capacitors equally, which is suitable for both the input power factor and the load transient improvement. The storage capacitor voltages do not vary by large amounts as the load varies, achieving a high power factor as well as improved load transient. Both of the subconverters are equally important as far as power handling capability and input power factor are concerned. The storage capacitor voltages remain almost constant for all values of loads. Thus, the stress on the main switch remains almost constant. It has high efficiency.

5. Results

The performance parameters of the converter are given in Table 2. It can be inferred from Table 2 that a high power factor is maintained throughout the entire range of the load. The storage capacitor voltages decrease as the load decreases. This means that the stress on the main switch reduces with a decrease in the load. No separate controller is required for regulating the storage capacitor voltages. The output voltage, however, varies with the load, which is regulated by means of a variation in duty ratio. As the input power is shared between the storage capacitors independently of the variation in the load, this converter is suitable for enhanced power transfer capability. Since the capacitor voltages reduce at low load, its efficiency is not low even at low loads.

6. Conclusions

The presented converter based on a noncascading scheme was proposed for improved power factor and load transient. As the capacitor voltages decrease when the load decreases, the duty ratio does not vary by large amounts with reduction in the load. This helped reduce stress on the main power switch, which, in turn, improves the efficiency by means of reduction in switching power losses. It thus maintains high efficiency even at low loads. By choosing proper values of inductors, the desired storage capacitor voltages can be chosen. Both the capacitors improve input power factor. The efficiency of the converter, as expected, is high compared with that presented in [1]. The improved efficiency is due to the presence of the forward subconverter that transfers

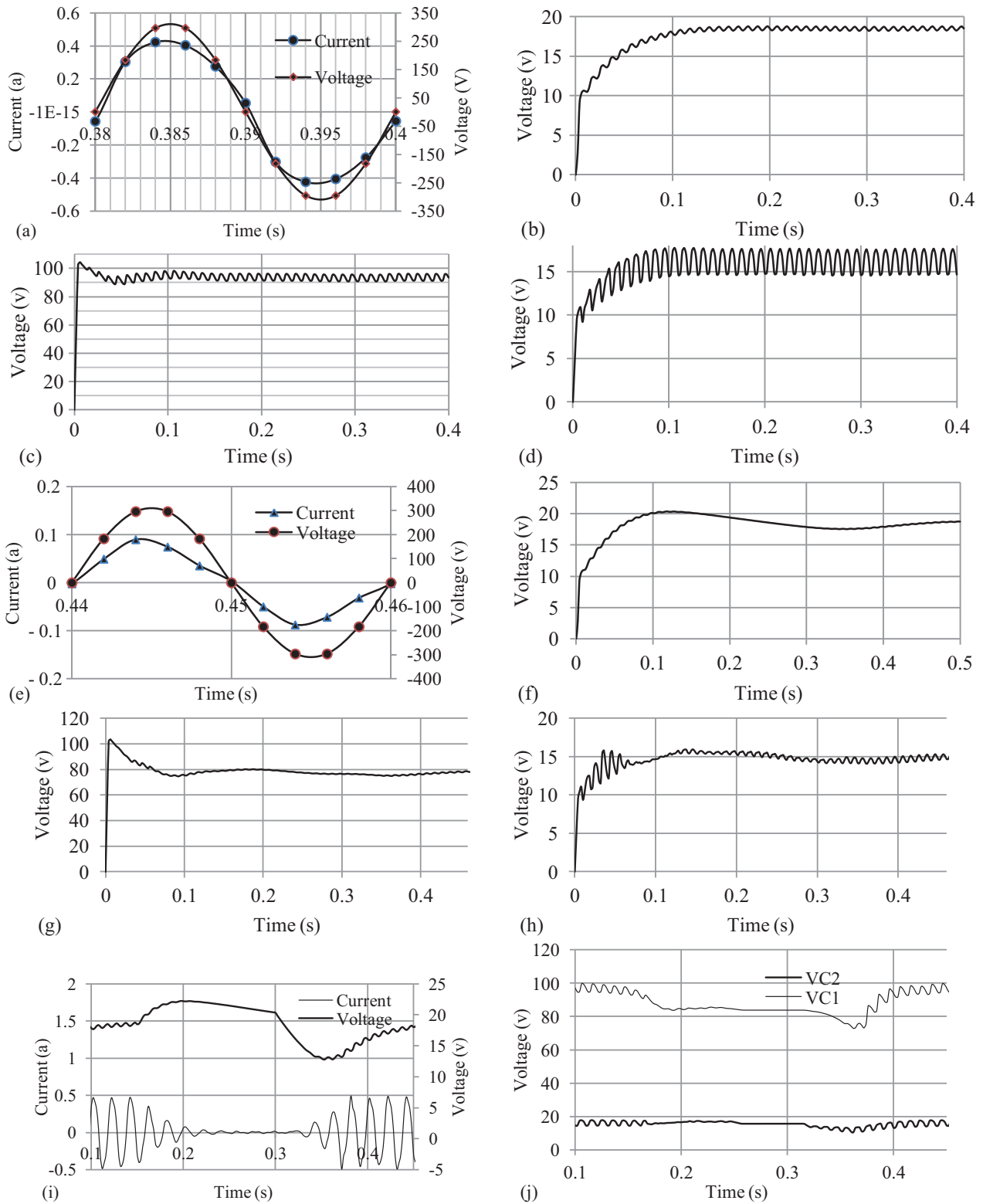
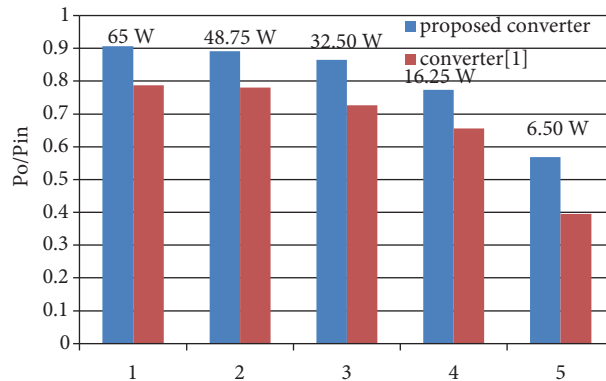


Figure 4. a) Input current and voltage waveforms at full load. b) Output voltage at full load. c) Capacitor C₁ voltage at full load. d) Capacitor C₂ voltage at full load. e) Input current and voltage at 10% load. f) Output voltage at 10% load. g) Capacitor C₁ voltage at 10% load. h) Capacitor C₂ voltage at 10% load. i) Output voltage and input current with the load transient. j) Variations of storage capacitors' voltages with the load transients.

Table 2. Performance evaluation parameters of the converter.

Output, power P_o (W)	Power factor (PF)	Capacitor C_1 voltage, V_{C1} (V)	Capacitor C_2 voltage, V_{C2} (V)	Input, current proposed converter (A)	Input current converter in [1] (A)	P_o/P_{in} for proposed converter	P_o/P_{in} for converter in [1]
65.00	0.9974	96.92	16.46	0.3258	0.3752	0.9068	0.7875
48.75	0.9960	86.08	13.37	0.2486	0.2839	0.8914	0.7805
32.50	0.9923	74.24	13.40	0.1707	0.2034	0.8654	0.7262
16.25	0.9948	77.18	14.29	0.0955	0.1127	0.7737	0.6554
6.50	0.9835	78.78	14.91	0.0520	0.0747	0.5682	0.3955

power to the load directly. As compared to one capacitor employed in [1], two capacitors have been used. This resulted in improved efficiency. By means of simulation, the comparative performance of the two converters is shown by Figure 5. A simple PI controller is employed for the regulation of the output voltage of the converter. No separate controller is required to control the capacitor voltages.

**Figure 5.** Comparison of performance of proposed converter with previous one.

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