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Electronically tunable grounded/floating inductance simulators using Z-copy CFCCC

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Abstract: In this paper, new electronically tunable grounded and floating inductance simulators employing a Z-copy current follower current controlled conveyor (CFCCC) and one grounded capacitor have been proposed and their workability has been demonstrated by PSPICE simulations in 0.18-μm TSMC CMOS technology.

Key words: Analog circuits, current-mode circuits, current conveyors, current followers, inductance simulators, analog filters

1. Introduction

Over the past several years, many new analog building blocks (ABBs) have been used to implement various signal processing/generation functions including the simulation of inductors, realization of universal biquadratic filters, sinusoidal oscillators, and nonsinusoidal waveform generators [1–10]. The various building blocks that have been prominently employed in the past for simulating the inductors include the operational transresistance amplifier (OTRA) [11,12], differential voltage current conveyor (DVCC) [13], current differencing buffered amplifier (CDBA) [14], current differencing transconductance amplifier (CDTA) [15], voltage differencing differential input buffered amplifier (VD-DIBA) [16,17], voltage differencing transconductance amplifier (VDTA) [18,19], voltage differencing current conveyor (VDCC) [20,21], voltage differencing buffered amplifier (VDBA) [22], current controlled current conveyor transconductance amplifier (CCCCTA) [23], current controlled current differencing transconductance amplifier (CCCDTA) [24,25], current controlled current feedback amplifier (CC-CFA) [26], current follower transconductance amplifier (CFTA) [27], current controlled current follower transconductance amplifier (CCCFTA), [28] and current backward transconductance amplifier (CBTA) [29].

In the following, we present new electronically tunable grounded/floating inductance simulators realized with the ABB named the Z-copy current follower controlled current conveyor (ZC-CFCCC). To the best knowledge of the authors, ZC-CFCCC has not been put to use yet for the realization of electronically controllable simulated inductors.

2. Electronically tunable grounded inductor

A current follower multiple-output current conveyor (CF-MOCC) was introduced in [1]. In the present work, we have modified its structure by taking out an additional Z copy of the input current and used a current controlled

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conveyor in its second stage to realize a ZC-CFCCC. Thus, the ZC-CFCCC is a five-port active building block characterized by the following terminal equation:

$$\begin{bmatrix} V_p \\ V_i \\ I_z \\ I_{zc} \\ I_x \end{bmatrix} = \begin{bmatrix} R_p & 0 & 0 & 0 & 0 \\ 0 & -R_i & 1 & 0 & 0 \\ 1 & 0 & -Y_z & 0 & 0 \\ 1 & 0 & 0 & -Y_{zc} & 0 \\ 0 & 1 & 0 & 0 & -Y_x \end{bmatrix} \begin{bmatrix} I_p \\ I_i \\ V_z \\ V_{zc} \\ V_x \end{bmatrix} \tag{1}$$

Here, R_p represents the input resistances of port p while R_i represents the output resistance of the voltage buffer implemented between port z and port i. Y_z, Y_{zc}, and Y_x each constitute a parallel combination of a resistor and a capacitor and represent the parasitic admittances associated with the ports z, zc, and x. When implemented in CMOS hardware such as that shown in Figure 1, the values of R_p and R_i are given by:

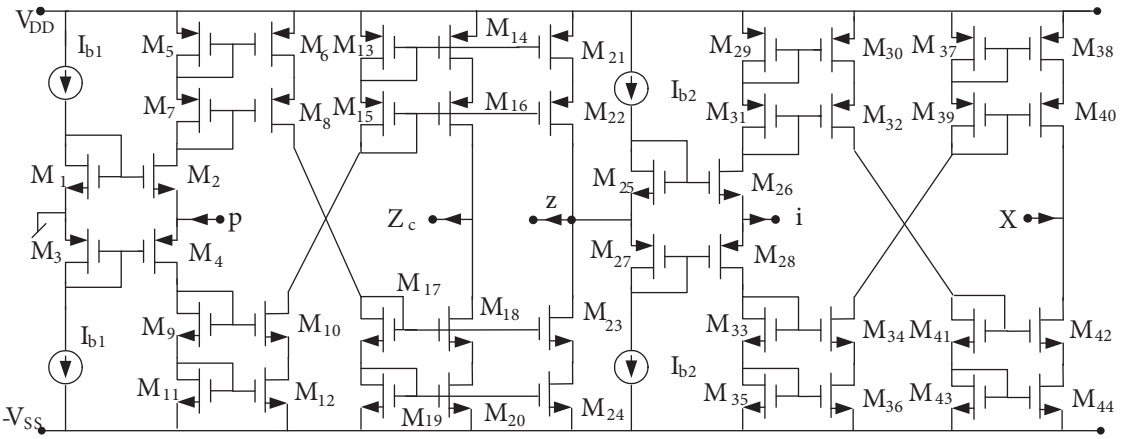

Figure 1. An exemplary CMOS implementation of the ZC-CFCCC.

$$R_p = \frac{1}{\sqrt{8\mu_n C_{ox}\left(\frac{W}{L}\right) I_{b1}}}, R_i = \frac{1}{\sqrt{8\mu_n C_{ox}\left(\frac{W}{L}\right) I_{b2}}} \tag{2}$$

Thus, R_p, and R_i can be controlled by external DC bias currents I_{b1} and I_{b2} [23,24,28].

Consider now the proposed new realization of the electronically tunable grounded inductor shown in Figure 2. A straightforward analysis of this circuit, using the port relationships of the ZC-CFCCC given in Eq. (1), gives the input impedance of the circuit as (when Y_z, Y_{zc}, and Y_x, the parasitic admittances at ports z, zc, and x, are taken to be zero):

$$Z_i = sR_pR_iC \tag{3}$$

where

$$R_p = \frac{1}{\sqrt{8\mu_n C_{ox}\left(\frac{W}{L}\right) I_{b1}}} \text{ and } R_i = \frac{1}{\sqrt{8\mu_n C_{ox}\left(\frac{W}{L}\right) I_{b2}}}$$

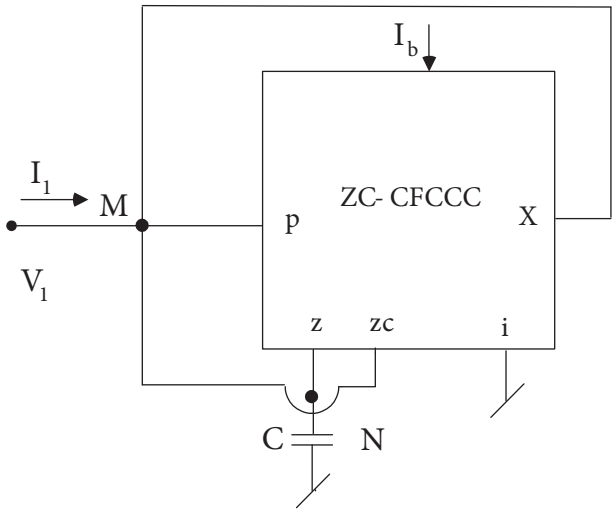

Figure 2. The proposed new electronically tunable grounded inductor.

If $I_{b1} = I_{b2} = I_b$, then the simulated inductance value is given by:

$$L_s = C\frac{1}{\left(8\mu_n C_{ox}\left(\frac{W}{L}\right) I_b\right)} \tag{4a}$$

It may be noted here that R_p and R_i need not be equal. Availability of two external currents for realization of a given value of inductance results in more flexibility in selecting these current sources. If only one current is available to control the value of the simulated inductor then the other resistor required will be a fixed-valued resistor. Therefore, the realized inductance can be varied electronically over a wider range.

On the other hand, if these parasitic elements are taken into consideration, then the impedance Z_{in} is given by:

$$Z_{in}(j\omega) = R_s + j\omega L_s \tag{4b}$$

$$R_s(\omega) = \frac{\omega^2(a_1b_1 - a_0b_2) + a_0b_0}{\omega^4 b_2^2 + \omega^2(b_1^2 - 2b_0b_2) + b_0^2} \tag{4c}$$

$$L_s(\omega) = \frac{-a_1b_2\omega^2 + (a_1b_0 - a_0b_1)}{\omega^4 b_2^2 + \omega^2(b_1^2 - 2b_0b_2) + b_0^2} \tag{4d}$$

The quality factor is:

$$Q(\omega) = \frac{\omega\left[-a_1b_2\omega^2 + (a_1b_0 - a_0b_1)\right]}{\omega^2(a_1b_1 - a_0b_2) + a_0b_0} \tag{4e}$$

where

$$\begin{aligned} &a_1 = R_pR_iR_xR_zR_{zc}(C + C_z);\quad a_0 = R_pR_iR_xR_{zc};\quad b_2 = R_pR_iR_xR_zR_{zc}(C + C_z)(C_x + C_{zc});\\ &b_1 = [R_pR_iR_z(C + C_z)(R_x + R_{zc}) + R_pR_iR_xR_{zc}(C_x + C_{zc})];\quad b_0 = R_pR_i(R_x + R_{zc}) + R_xR_zR_{zc}. \end{aligned} \tag{4f}$$

3. Electronically tunable floating inductor

From the circuit of the proposed electronically tunable grounded inductor it is observed that the configuration implements an active gyrator with its input port being node M and the output port being node N. A straightforward analysis of this gyrator circuit results in the following short circuit admittance matrix:

$$[Y] = \begin{bmatrix} 0 & \frac{1}{R_i} \\ -\frac{1}{R_p} & 0 \end{bmatrix} \tag{5}$$

Therefore, using two such active gyrators and one grounded capacitor embedded between them, an electronically tunable floating inductor (FI) can be realized as shown in Figure 3, for which the short-circuit admittance matrix is found to be:

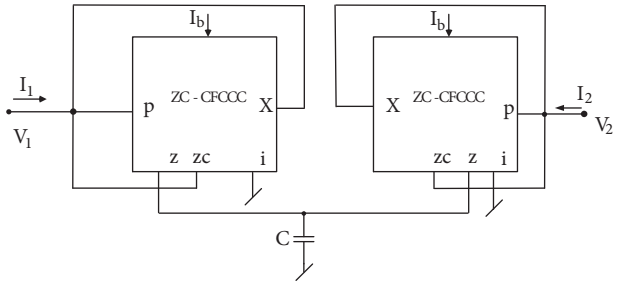

Figure 3. The proposed new electronically tunable floating inductor.

$$[Y] = \frac{1}{sC}\begin{bmatrix} \frac{1}{R_i R_p} & -\frac{1}{R_i^2} \\ -\frac{1}{R_p^2} & \frac{1}{R_i R_p} \end{bmatrix} = \frac{1}{sCR^2}\begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \tag{6}$$

where

$$R_p = R_i = R = \frac{1}{\sqrt{8\mu_n C_{ox}\left(\frac{W}{L}\right) I_b}}$$

Thus, the value of the realized floating inductance can be varied by changing external bias current I_b. It may be noted that this can be implemented quite easily by supplying equal DC bias currents to the two ZC-CFCCCs, unlike the constraints imposed by passive component matching as prevalent in many of the classical floating inductance simulation circuits using op-amps. If the parasitic admittances associated with ports z, zc, and x are taken into account then the nonideal short-circuit admittance parameters (for $\mathrm{I}_{b1} = \mathrm{I}_{b2} = \mathrm{I}_b$, $\mathrm{R}_i = \mathrm{R}_p = \mathrm{R}$) are found to be:

$$y_{11} = \frac{\left(\frac{1}{R_{EQ}^2} + \frac{1}{R_{EQ}R_z} + \frac{1}{R^2}\right) + \left(2\frac{C_P}{R_{EQ}} + \frac{C}{R_{EQ}} + \frac{C_P}{R_z} + \frac{C_z}{R_{EQ}}\right)s + \left(C_P^2 + C_P C + C_P C_z\right)s^2}{\left(\frac{1}{R_{EQ}} + \frac{1}{R_z} + \left(C_P + C_z + C\right)s\right)} \tag{7}$$

$$y_{12} = \frac{-\frac{1}{R^2}}{\left(\frac{1}{R_{EQ}} + \frac{1}{R_z} + \left(C_P + C_z + C\right)s\right)} = y_{21} \tag{8}$$

$$y_{22} = \frac{\left(\frac{1}{R_z^2} + \frac{1}{R_{EQ}R_z} + \frac{1}{R^2}\right) + \left(2\frac{C_z}{R_z} + \frac{C}{R_z} + \frac{C_P}{R_z} + \frac{C_z}{R_{EQ}}\right)s + \left(C_z^2 + C_zC + C_PC_z\right)s^2}{\left(\frac{1}{R_{EQ}} + \frac{1}{R_z} + \left(C_P + C_z + C\right)s\right)} \tag{9}$$

where

$$R_{EQ} = R_{zc}||R_x, C_P = C_{zc} + C_x, R_s = \frac{R_pR_i}{R_z} \; and \; L_s = R_pR_i\left(C + C_z\right) \tag{10}$$

The expressions for the y-parameters, as above, appear to be quite formidable and do not lend themselves to meaningful interpretations directly. We therefore measure the y-parameters of the circuits using PSPICE simulations and plot their frequency responses along with the theoretical plot of Eqs. (7)–(9) in MATLAB in the next section.

4. SPICE simulations, application examples, and results

The CMOS implementation of the proposed ZC-CFCCC using 0.18-μm TSMC process technology parameters has been used to verify the workability of the circuits presented in this paper. Measured values of the characterizing parameters of the ZC-CFCCC given in Eq. (1) at DC bias voltage $\pm$2.5 V and DC bias currents 40 μA are given in Table 1, whereas the aspect ratios of the various MOSFETs are shown in Table 2. The measured value of THD of an amplifier configured with ZC-CFCCC when the input current was varied between 20 and 80 μA was found to vary between 0.75% and 3.5% at 1 MHz (when z and i terminals are terminated with equal resistance of 10 kΩ).

Table 1. Characteristic parameters of ZC-CFCCC.

S. no.	Parameter	Value
1	R_p	591 Ω
2	R_z	4.9178 MΩ
3	C_z	6.3234×10^{-14} F
4	R_{zc}	4.9178 MΩ
5	C_{zc}	7.2123×10^{-15} F
6	R_x	4.79990 MΩ
7	C_x	7.3772×10^{-15} F
8	R_i	591 Ω
9	Power consumption	2.47 mW
10	Linear range of current transfers I_p/I_z, I_p/I_{zc}, and I_i/I_x (mA)	–0.8 to +0.75 with gain 1.00049
11	Linear range of voltage transfers (V) V_z/V_i	–3.0 to +3.0 with gain 0.9882
12	3 dB bandwidth (MHz) (i) I_p/I_z,and I_p/I_{zc} (ii) I_x/I_i (iii) V_i/V_z	 527 1215.8 2860

Table 2. Aspect ratios of MOSFETs used in ZC-CFCCC realization.

MOSFETs	W/L (μm/μm)
M_1, M_2, M_{25}, M_{26}	25/0.25
M_3, M_4, M_{27}, M_{28}	50/0.25
M_5–M_{24}, M_{29}–M_{44}	2.5/0.25

The proposed grounded inductor circuit was simulated with C = 1 nF for different values of bias current I_b starting from 0.01 μA to 200 μA. The variation of inductance with bias current is shown in Figure 4, which is similar to the variation of inductance with bias current for other electronically tunable lossless grounded inductance circuits, such as the one given in [20]. It was found that inductance value could be varied from 998 H to 135 μH, over the above range. The typical value of inductance for a bias current of 40 μA was found to be 350 μH while the power consumption was 2.47 mW.

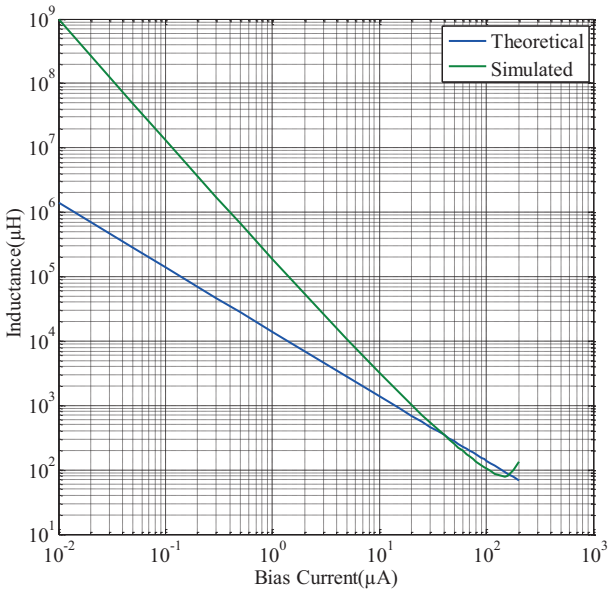

Figure 4. Variation of inductance with bias current.

The frequency response of the simulated inductor was also determined in PSPICE (for I_b = 40 μA) and is shown in Figure 5 (L = 350.04 μH at a frequency of 35.3 KHz). Independent simulations have shown that the value of the inductance remains within a tolerance value of 10% up to a frequency of 2.99 MHz. We have also superimposed on the frequency response the theoretical plots as obtained from Eqs. (4c) and (4d). From the frequency response plots it is observed that the inductance value remains nearly constant only up to a particular frequency. This is corroborated by the behavior of simulated lossless grounded inductors realized with other active building blocks [15–18]. Though the parasitic resistance associated with the simulated inductor becomes negative at higher frequencies, the application circuits have not shown any unstable behavior. The quality factor of the simulated grounded inductor (for bias current of 40 μA) was also measured and found to be 335 at 10 kHz. Figure 6 shows the variation of quality factor with frequency. The simulated results agree quite well with the theoretical ones. The discrepancy between theoretical and simulated results mainly stems from nonideal gain and parasitic impedance effects of the ZC-CFCCC.

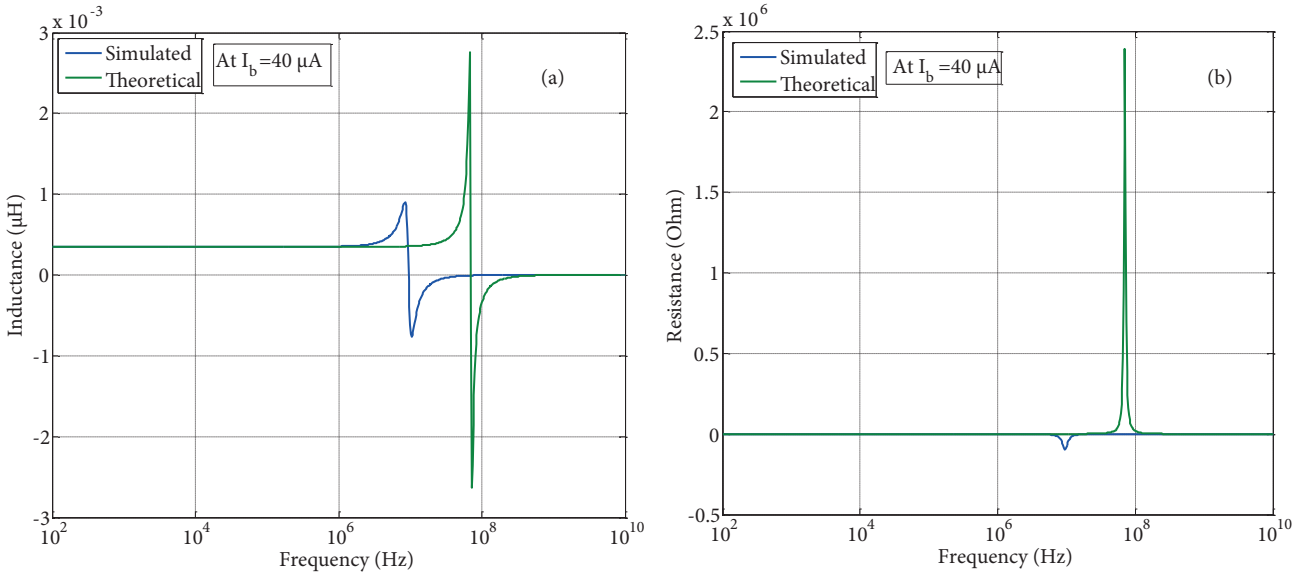

Figure 5. Frequency response of simulated lossless grounded inductor: a) variation of inductance value with frequency; b) variation of parasitic resistance with frequency.

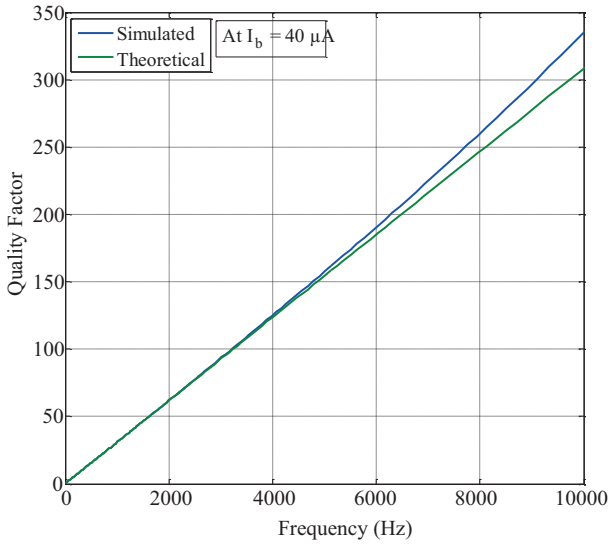

Figure 6. Variation of quality factor with frequency.

An input current with a triangular waveform (20 μA amplitude and 1 kHz frequency) was applied to the proposed inductor (46.45 μH). The output voltage, a square wave (22 μV at 1 KHz) as shown in Figure 7, was obtained, which further confirmed the workability of the electronically tunable grounded inductor.

The second-order band-pass filter shown in Figure 8 was used to verify the tunability of the pole frequency with bias current. The pole frequency and the bandwidth of the filter are given by pole frequency $f_o = \frac{1}{2\pi\sqrt{LC_1}}$ and bandwidth $BW = \frac{1}{2\pi RC_1}$.

The band-pass filter was designed with the following component values: R = 3 kΩ, C = 1 nF, C_1 = 10 pF, and bias current varied from 35 μA to 70 μA to vary the pole frequency without affecting the bandwidth.

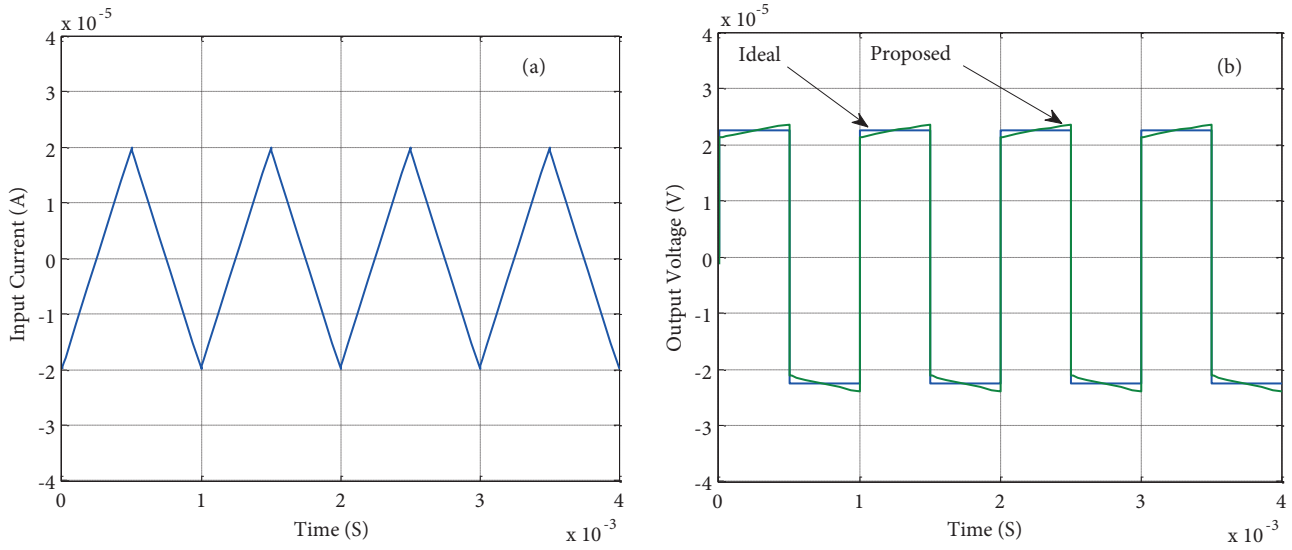

Figure 7. Time domain analysis of the proposed grounded inductor: a) input current waveform; b) output voltage waveform.

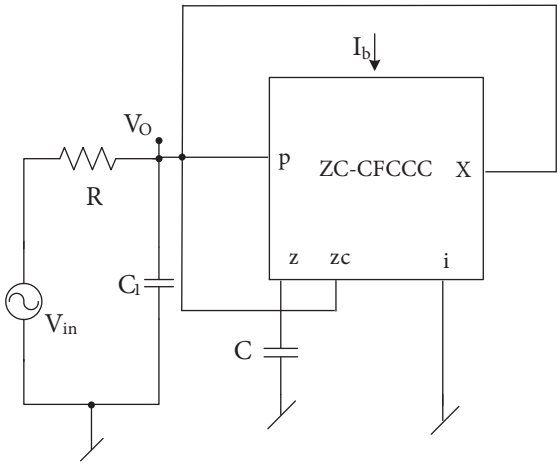

Figure 8. Tunable second-order RLC band-pass filter.

Figure 9 shows the frequency response of the band-pass filter with different values for the pole frequency. These results are in close agreement with the theoretical values ($f_0 \propto \sqrt{I_b}$) with the maximum error in the pole frequency being less than 10%. The maximum error in bandwidth has been found to be about 2%. The THD in the output was also measured and found to lie within 0.3%–2.4% when the input amplitude was varied in the range of 10–150 mV.

The frequency response of the floating inductor was determined through PSPICE simulations to find its usable frequency range. Figure 10 shows the frequency response of the short-circuit admittance parameters. We have also superimposed the frequency response as computed from Eqs. (7)–(9). There is a very close agreement between these three plots. Independent simulations have indicated that the floating inductor can be used up to a frequency of 2.94 MHz (at $I_b = 40$ μA); the simulated inductance was within 10% of the designed value of 350 μH while the associated resistance was varying between less than 142 mΩ to –579.20 Ω up to a frequency of 2.94 MHz.

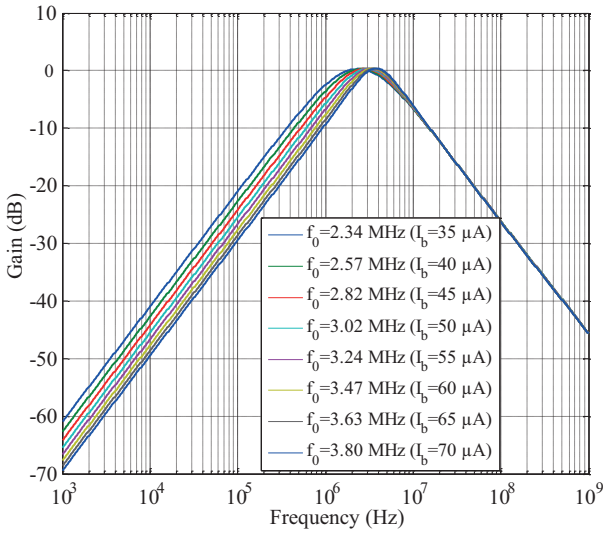

Figure 9. Frequency response second-order BPF for different values of bias current.

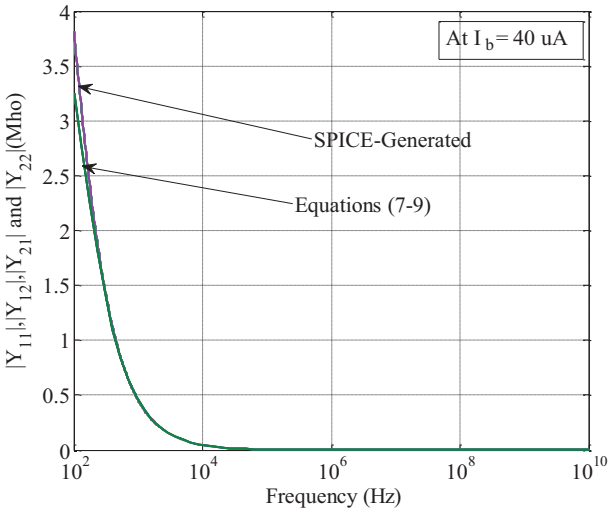

Figure 10. Frequency response of the y parameters of the simulated floating inductor.

We have used the proposed floating inductor to implement a fourth-order Butterworth low-pass filter as shown in Figure 11. Starting from the nominal values of the components for the normalized low-pass filter at 1 Hz as $R_s = R_L = 1\ \Omega$, $L_1 = 0.7654$ H, $L_2 = 1.8478$ H, $C_1 = 1.8478$ F, and $C_2 = 0.7654$ F [30], after appropriate frequency and impedance scaling we get the following values of passive components for the filter cut-off frequency of 500 kHz: $R_S = R_L = 1$ KΩ, $L_1 = 0.2437$ mH (C =1 nF, $I_b = 51.46\ \mu$A), and $L_2 = 0.5884$ mH (C = 1 nF, $I_b = 28.37\ \mu$A). This finally resulted in a fourth-order active filter structure using all grounded capacitors, as preferred for IC implementation. Frequency response of the resulting fourth-order low-pass Butterworth filter is shown in Figure 12. The value of the cut-off frequency found from the simulation was 500.50 kHz, showing a very close agreement with the theoretical value of 500 kHz. The THD in the output

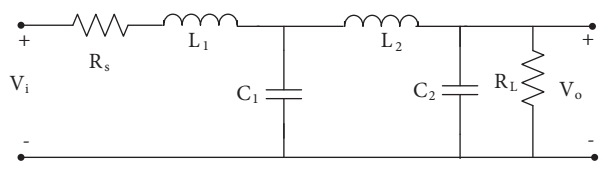

Figure 11. Prototype fourth-order low-pass Butterworth filter.

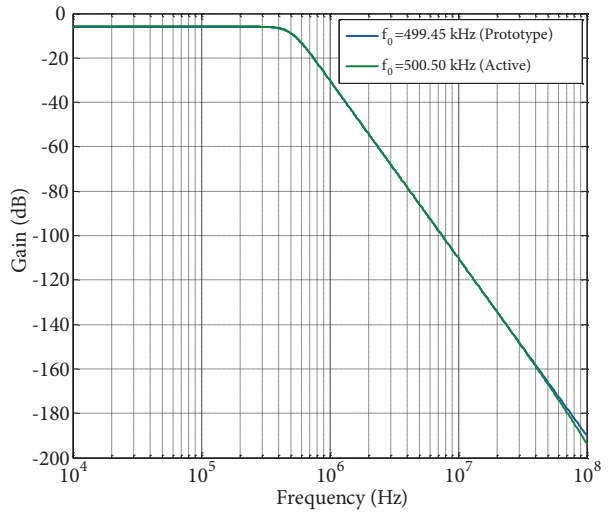

Figure 12. Frequency response of the fourth-order low-pass Butterworth filter.

was also measured when the amplitude of the input voltage was varied between 10 mV and 150 mV and found to vary between 0.2% and 7%.

To study the effect of mismatches in the component values within the floating inductors on the performance of the circuit of the fourth-order low-pass Butterworth filter, Monte Carlo simulations have been carried out by allocating 1% tolerances to the component values (capacitors C = 1 nF) within both of the floating inductors and performing 100 runs. The results for the 1% tolerance are shown in Figure 13. The value of the simulated cut-off frequency was found to be 500.50 kHz and Monte Carlo analysis shows that the median value

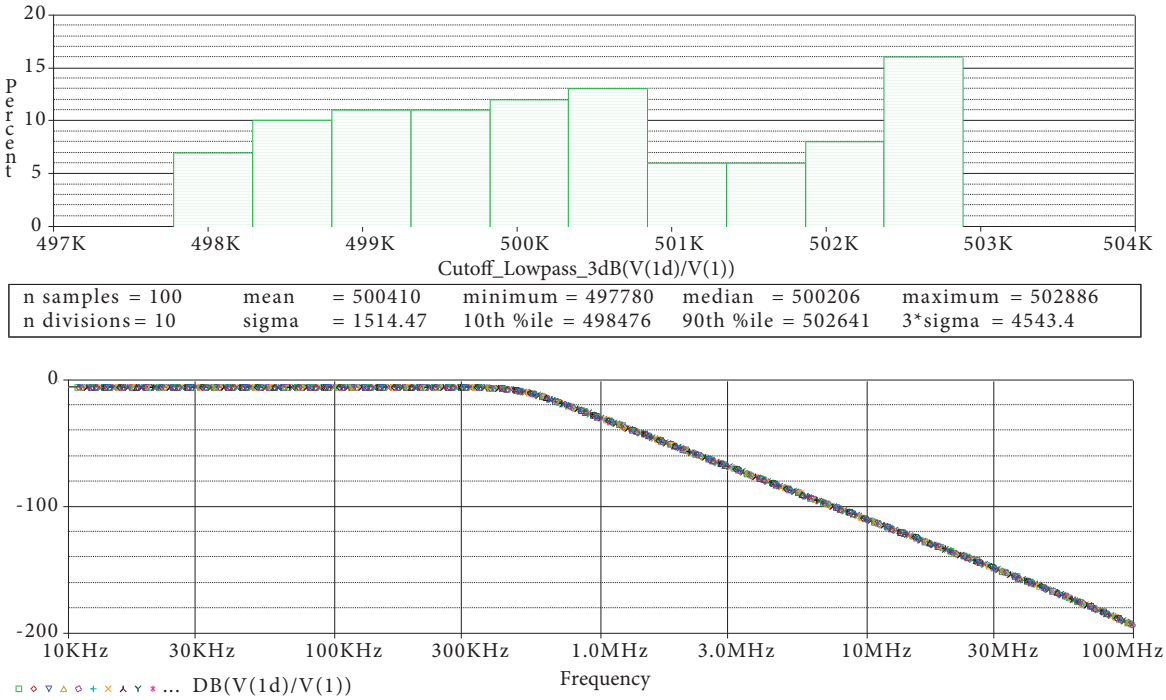

Figure 13. Simulation results of Monte Carlo analysis for fourth-order low-pass Butterworth filter.

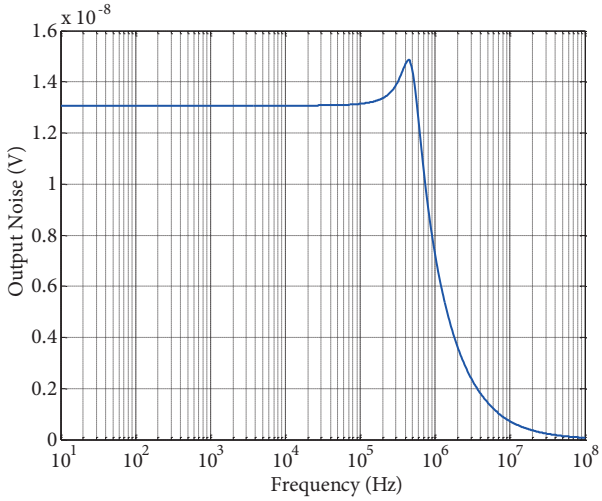

Figure 14. Output noise variation for fourth-order low-pass Butterworth filter.

Table 3. Comparison with other previously published lossless grounded and floating inductors realized with synthetic active building blocks.

Ref.	Type*	Number of ABBs	Number of resistors	Number of capacitors	Free from component passive matching?	Tunability	Technology	Power supply	Power dissipation
[11]	G	2: OTRA	5	1F	No	No	Discrete (AD844)	±10 V	NA
[12]	G	1: OTRA	3	2F	No	No	0.5 μm/AD844	±1.5 V/±5 V	0.809/260 mW
[13]	F	2: DVCC	2	1G	Yes	No	0.18 μm	±1.25 V	NA
[14]	F	3/4: CDBA	4 [VCR]	1G	Yes	Yes	0.5 μm	±2.5 V	NA
[15]	G	2: CDTA	0	1G	Yes	Yes	0.5 μm	±2.5 V	NA
	F	3: CDTA	0	1G	Yes	Yes	0.5 μm	±2.5 V	NA
[16]	G	2: VD-DIBA	0	1G	Yes	Yes	Discrete ((AD844) + CA3080))	±1 V	62.5 mW
	F	3: VD-DIBA	0	1G	Yes	Yes	Discrete ((AD844) + CA3080))	±1 V	62.5 mW
[17]	G	1: VD-DIBA	1	1G	Yes	Yes	0.35 μm	±2 V	NA
	F	2: VD-DIBA	1	1G	No	Yes	0.35 μm	±2 V	NA
[18]	G	1: VDTA	0	1G	Yes	Yes	0.18 μm	±0.9 V	NA
	F	2: VDTA	0	1G	Yes	Yes	0.18 μm	±0.9 V	NA
[19]	F	1: ZC-VDTA	0	1G	Yes	Yes	0.18 μm	±0.9 V	1.25 mW
[20]	G	1: VDCC	1	1G	Yes	Yes	0.18 μm	±0.9 V	0.869 mW
[21]	F	1: VDCC	1	1G	Yes	Yes	0.18 μm	±0.9 V	NA
[22]	G	1: VDBA	1	1F	Yes	Yes	Discrete (OPA860)	±5 V	NA
[23]	G	1: CCCCTA	0	1G	Yes	Yes	0.35 μm	±1.5 V	899 μW
[24]	F	1: CCCDTA, 2: VB	0	IG	Yes	Yes	0.35 μm	±1.5 V	1.48 mW
[25]	F	1: CCCDTA, 2: VB	0	1G	Yes	Yes	Bipolar ALA400	±1.5 V	1.23 mW
[26]	G	2: CC-CFA	0	1G	Yes	Yes	(ALA400 + 0.35 μm)	±1.5 V	4.16 mW
[27]	F	3: CFTA	0	1G	Yes	Yes	Bipolar ALA400	±1.5 V	NA
[28]	G	1: CCCFTA	0	1G	Yes	Yes	0.5 μm	±2.0 V	NA
[29]	F	2: CBTA	2	1G	Yes	Yes	0.25 μm	±2.5 V	NA
[45]	F	1: MCFOA	2	1G	Yes	No	0.35 μm	±1.5 V	NA
[46]	G	1: New CFOA	2	1F	Yes	No	Discrete	±15 V	NA
[47]	G	1: CFOA–	2	1F	Yes	No	0.13 μm	±6 V/0.75 V	890 μW
[48]	G	1: MICCII–	2	1F	No	No	0.35 μm	±2.5 V	17.6 mW
Proposed	G	1: ZC-CFCCC	0	1G	Yes	Yes	0.18 μm	±2.5 V	2.47 mW
Proposed	F	2: ZC-CFCCC	0	1G	Yes	Yes	0.18 μm	±2.5 V	4.94 mW

*F: Floating, G: grounded.

of cut-off frequency is f_0 = 500.41 kHz, which indicates that the mismatch in the component values within the proposed floating inductors does not have a large effect on the realized cut-off frequency.

PSPICE noise analysis has also been performed on the fourth-order low-pass Butterworth filter and variations in the output noise are shown in Figure 14.

The PSPICE simulation results presented in this section thus establish the workability and applications of the proposed new inductance simulators using ZC-CFCCC.

5. Comparison with previously published circuits

A comparison of the various salient features of the proposed configurations as compared to other previously known lossless grounded and FI simulators realized with synthetic active building blocks is now in order, presented in Table 3. It is observed from the table that the proposed circuits, with the exceptions of the circuits given in [18,19,28], are the only circuits that realize an electronically tunable lossless grounded inductor employing a single active building block, no passive resistors, and a single grounded capacitor and do not require any passive component matching constraint. It may be mentioned here that because of the terminal equations of the ZC-CFCCC, CC-CDTA, and CC-CCTA being somewhat similar, the proposed inductance simulation circuits may appear to be somewhat similar to the circuits proposed in [23,25], where CC-CCTA and CC-CDTA were used as ABBs. On the other hand, yet another building block proposed in [1], namely the CDCC [31–33], can also be configured as a ZC-CFCCC if we do not use one of its input current terminals and use a current-controlled conveyor (instead of CCII) in the second stage. The grounded inductance simulators used here can directly be used in the simulation of LC ladders in contrast to the lossy inductance simulators realized with other active building blocks of recent origin [34–44].

6. Concluding remarks

In this paper, new electronically tunable, lossless grounded and floating inductance simulation circuits using the ZC-CFCCC as an active element were proposed. The proposed circuits employ only a single ZC-CFCCC for grounded inductance simulation and two ZC-CFCCCs for floating inductance simulation along with a single grounded capacitor as preferred for IC implementation. Thus, the new circuits provide a number of advantageous features simultaneously, such as use of a canonic number of active and passive elements, electronic tunability by means of external bias currents, complete absence of passive component matching, and employment of a single grounded capacitor, as preferred for IC implementation. For simulation of floating inductance, the only constraint required is the equality of the two bias currents, which can be easily met by using current copier cells. The workability of the new propositions as well as their two typical application circuits has been verified through PSPICE simulations using 0.18-μm TSMC CMOS technology parameters. It is believed that the proposed ZC-CFCCC-based electronically tunable inductance simulators add new alternatives to the existing repertoire of synthetic ABB-based inductance simulators, as shown in Table 3. This table also contains modified CFOAs and modified inverting second-generation current conveyor-based inductance simulators [45–48] but does not include circuits based upon traditional current conveyors (see those in [49–52] and the references cited therein).

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