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A novel efficient TSV built-in test for stacked 3D ICs

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Abstract: A through-silicon via (TSV) is established as the main enabler for a three-dimensional integrated circuit (3D IC) that increases system density and compactness. The exponential increase in TSV density led to TSV-induced catastrophic and parametric faults. We propose an original architecture that detects errors caused by TSV manufacturing defects. The proposed design for testability is a built-in technique that detects errors in an early manufacturing stage and is hence very economically attractive. The proposal is capable of testing each and every TSV in the network. The technique achieves high fault coverage and high observability.

Key words: 3D IC, through-silicon via, built-in current sensor, built-in self-test, design for testability, test access mechanism

1. Introduction

Stacking 3D integrated circuits (ICs) is a promising technology that enables computing power to continue following Moore's law. Stacked 3D ICs allow taking advantage of the high bandwidth offered by through-silicon vias (TSVs), offering, by the same token, a wide range of new system-on-chip applications.

A TSV is an interconnection that allows connecting layers of 3D integrated circuits [1]. The advantage of TSVs is an enhanced electrical performance and an increased integration density [2]. On the other hand, during the various stages of manufacturing of 3D circuits, defects may occur at the TSV [3]. Defects can arise from unique processing steps such wafer thinning, alignment, and bonding [4]. These defects may affect the performance of circuits. Test strategies have to be used to detect these defects. Nevertheless, 3D circuits have many test challenges, especially in prebond tests. Challenges in this step of testing are related to the small dimensions of TSVs (TSVs are too small for the test probe and their diameter may vary between 4 and 10 μm [5]) and their densities, which can reach from several thousands to millions per square centimeter [6]. To overcome the challenges related to probe testing, postbond tests and specifically built-in self-test (BIST) architectures can be used to detect defective TSVs [7]. Many works regarding postbond testing have been done. The majority of research concerns catastrophic defects, while less consideration has been given to weak defects [7]. To be effective, postbond architectures have to take the analog proprieties of the TSV into consideration [8]. Delay characterization techniques are required to test a TSV's parametric faults during postbond testing and especially in the case of weak open and shorts defects, which can cause delay faults in the circuit [9].

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One of the essential issues of postbond tests is the test access mechanism (TAM). After bonding, intermediate chips become unobservable unless an access mechanism is introduced. TSVs' pads are completely covered and the inner layers of circuits are not designed to have external pins [10]. Access to TSVs of intermediate levels is only possible through the master die, which comprises the external input/output pins [11].

In this context, the testing of TSVs is a key challenge for designers due to the test access problems [12]. To achieve an effective test, some requirements of the TAM have to be met:

1) The 3D design for testability (DFT) architecture needs to be scalable with the number of dies of the circuit.

2) The test of the 3D IC has to be modular: circuits and TSV must be tested separately.

3) The TAM has to allow the possibility of testing the internal chip connections.

Among studies that have been done in the field of 3D postbond testing, Paska proposed a concept based on boundary scan architecture [13]. The concept was used to test the interconnections of 3D integrated circuits. It offers several advantages, including reducing the test pin number and the elimination of external testers, since test vectors are generated on the chip. The drawback of this method is that it treats exclusively digital test signals. In the case of weak defects, the BIST circuit must consider the analog properties of the TSV.

Another architecture based on the use of a ring oscillator and intended for the postbond test was presented in [14]. The test is based on the monitoring of the frequency of the TSV output signal to detect possible defects. Such a method requires a substantial test time. Moreover, no test access mechanism has been presented to access the inner layer. A BIST scheme for the postbond testing of a TSV was presented in [15]. However, such BIST structures cause a significant increase in the area overhead in consequence of the high number of required buffers and logic gates in the transportation and evaluation circuit.

In this paper, we propose a postbond test architecture. The BIST architecture is composed by a TAM that allows access to the TSVs of the inner layers of 3D ICs and a diagnostic block allowing the test of TSVs and the distinction between the defective and the defect-free ones. The BIST architecture is able to test each TSV in the network. The technique achieves high fault coverage due to the consideration of weak short and open defects and the high observability offered by the designed test access mechanism. The BIST architecture can detect defaults caused by catastrophic and parametric defects. A delay characterization technique is proposed to detect weak open and short defects, which can cause delay faults in the circuit.

This paper is organized as follows: Section 2 presents the background and the design concept. Section 3 presents the system description of the proposed DFT test technique. Section 4 gives the simulation results. Finally, we conclude in Section 5.

2. Background

The manufacturing process of 3D ICs leads to the appearance of a test flow different from that of conventional circuits and to the arising of a new type of defects.

2.1. 3D IC testing

The test flow of 3D ICs (Figure 1a) is different than that of 2D circuits (Figure 1b). Classical ICs are tested at the end of the production cycle. In contrast, 3D ICs have multiple phases of production; the chips (layers) are manufactured separately.

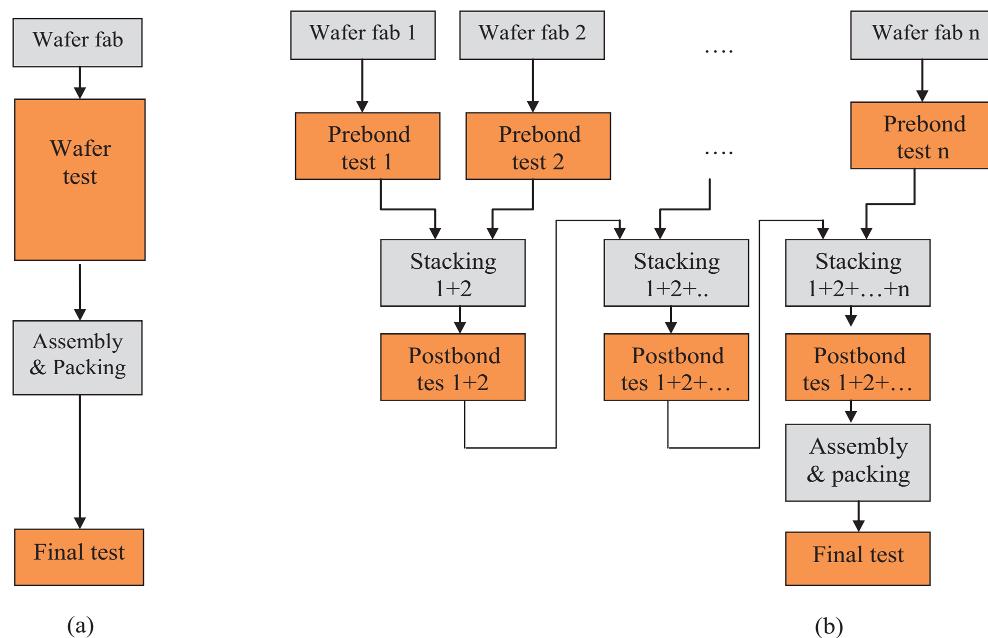

Figure 1. 3D vs 2D testing flow: a) 3D testing flow, b) 2D testing flow.

A joint strategy should be applied, involving testing each chip before bonding (prebond test). At the end of the process, a final test of the circuit is performed. Intermediate tests are performed before the final 3D IC test. Circuits are tested before assembling and packing in the 3D prebond test. The stack is retested after stacking in the postbond stack test. This can check if the dies that have been stacked are damaged during the stacking process. If the faulty stacked dies are identified, then the remaining dies will not be used. The outgoing product quality is guaranteed by the final test [16]. Performing all these tests allows the manufacturer to distinguish the functional circuits from the failed ones. The flow of the 3D integrated circuits test and a comparison between 2D circuits test flow and 3D circuits test flow are presented in Figure 1.

2.2. TSV defect classification

TSVs are critical elements in 3D integration. However, some defects can occur at these elements, which may damage the operation of 3D integrated circuits. These defects are summarized in the following 5 categories.

2.2.1. Misalignment defects

For alignment, there are 2 types of defects: alignment shifts and total misalignment. An alignment shift (Figure 2a) induces an increase in the resistance, whereas total misalignment causes a major fault represented by an open circuit between the TSV and the microbump [17].

2.2.2. Defects of Cu-pillar

This failure comes from the empty portion of the TSV, which should normally be filled with copper (Figure 2b). This type of defect can be caused by electromigration [17]. Voids can also be produced in Cu deposits due to improper TSV filling during electroplating processes, which cause the increase of the internal resistance of the TSV [18].

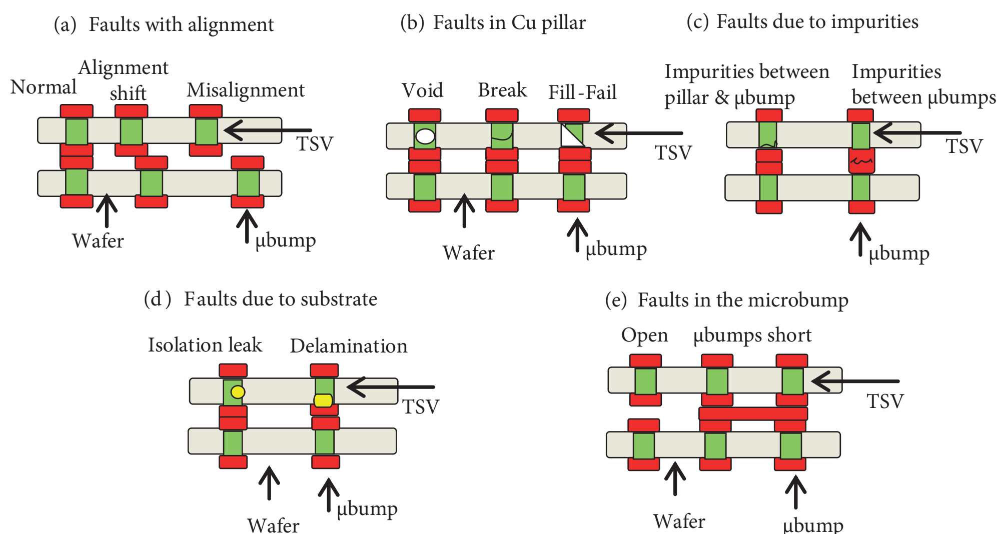

Figure 2. TSV defect classification: a) Defects due to misalignment, b) defects in Cu-pillar, c) defects due to impurities, d) defects in the substrate, e) defects in the microbumps.

2.2.3. Defects due to impurities

Voids and cracks can occur in the joints of microbumps. This is due to electromigration [19]. Figure 2c shows an example of this type of defect. The circuit is put under a stress test with a current of 0.13 A for the TSV and microbump. The test result is an increase of internal resistance of the TSV to a value greater than 20% compared to the original resistance [20].

2.2.4. Defects in the substrate

Nonuniformity of the insulating protective layer can cause a leakage path between the TSV and the substrate, thereby causing insulation failure (Figure 2d). One of the most common failures in TSVs is delamination caused by thermal stress processes. Delamination can cause open-type defects [17].

2.2.5. Defects in microbumps

Open defects between microbumps are due to deformation of the microspheres, where the deformation of the wafer and the break between 2 microbumps cause a discontinuity (Figure 2e). Short defects between 2 microbumps are due to a short circuit between them [17].

3. Design of the proposed DFT test

In this section we describe and detail the DFT technique designed for testing TSVs.

The testing technique consists of 2 main parts:

✓ A test access mechanism allowing individual access to each TSV.

✓ A block designed to test TSVs' signals and detect the defects.

3.1. Test access mechanism

Figure 3 presents an architecture designed to access the TSVs of inner dies, thereby allowing the observability and the testing of TSV signals.

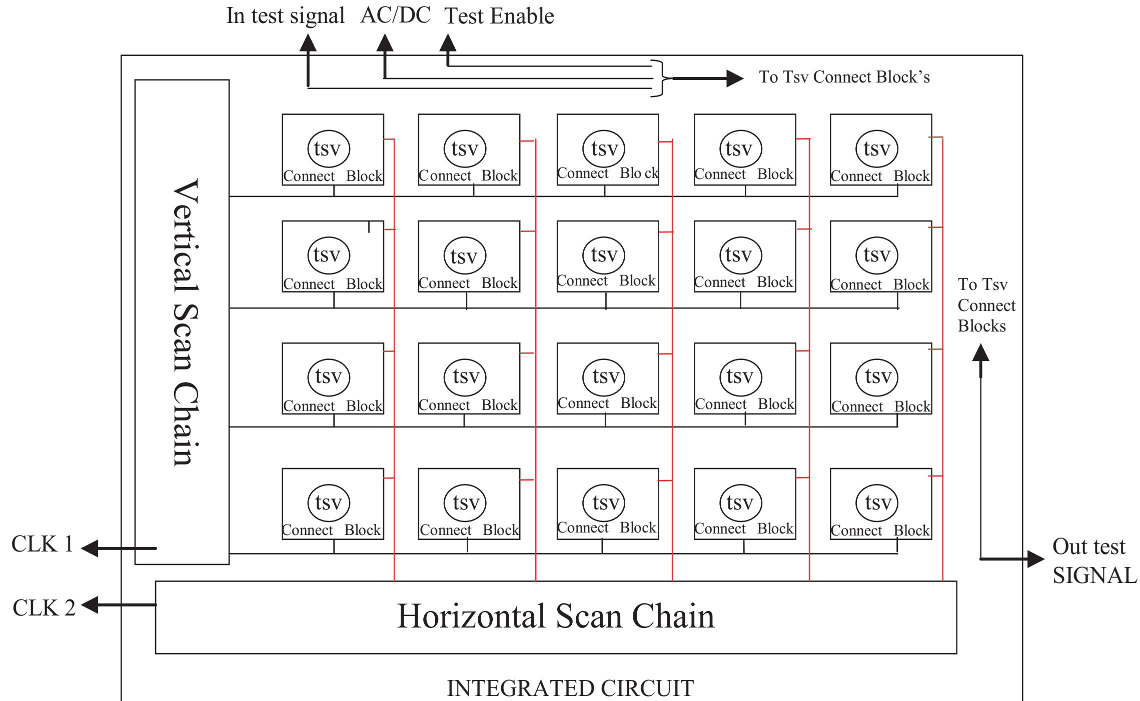

Figure 3. TSV test structure.

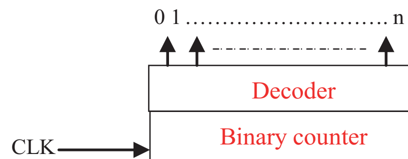

Figure 4. Internal structure of the scan chain (horizontal and vertical).

The horizontal and the vertical scan chains are composed of a latch-based binary counter and a decoder. The scanning frequency is controlled by CLK1 and CLK2 clocks. A binary counter is connected to a decoder. The decoder receives the binary address of the column or the line to be activated, converts it, and enables the correspondent output. The test mode is activated by enabling the test-enable signal. The counter and the decoder are selected according to the number of TSVs of the circuit.

The multiplexing approach described in Figure 3 allows the control of a large number of TSVs. For example, if we have a horizontal scan chain composed of a decoder having 512 outputs and a vertical scan chain identical to the horizontal scan chain, we can control the testing of 262,144 TSVs. During each test cycle, only one line and one column are activated, thereby allowing the control of only one TSV at one time.

In a 3D IC that contains many layers, each layer of a TSV is tested separately. The same test structure is used to test TSV connecting dies of upper layers. Test controls and signals are transmitted to upper layers through test elevators.

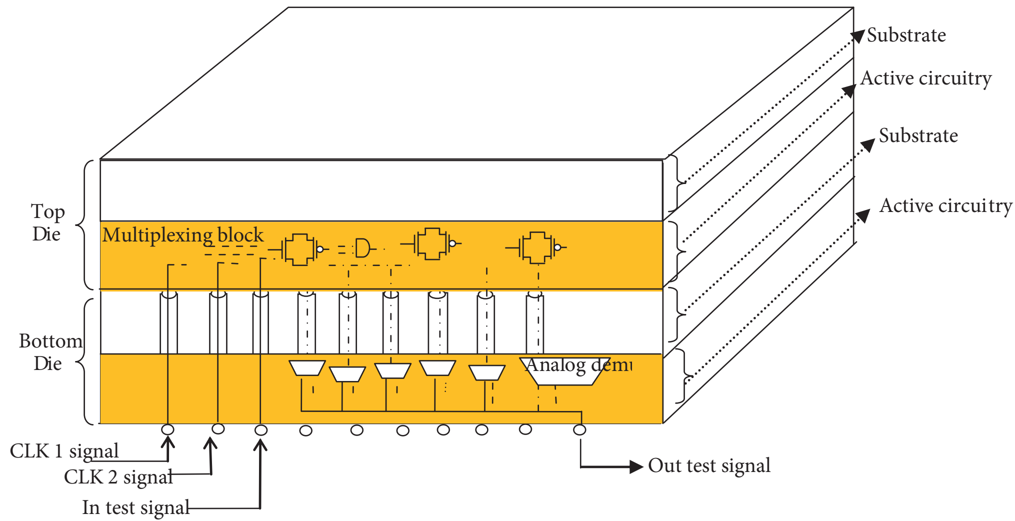

Figure 5. Structure of 3D IC with face to back stacking.

3.2. TSV connection block

Figure 6 describes the internal structure of the TSV connection block.

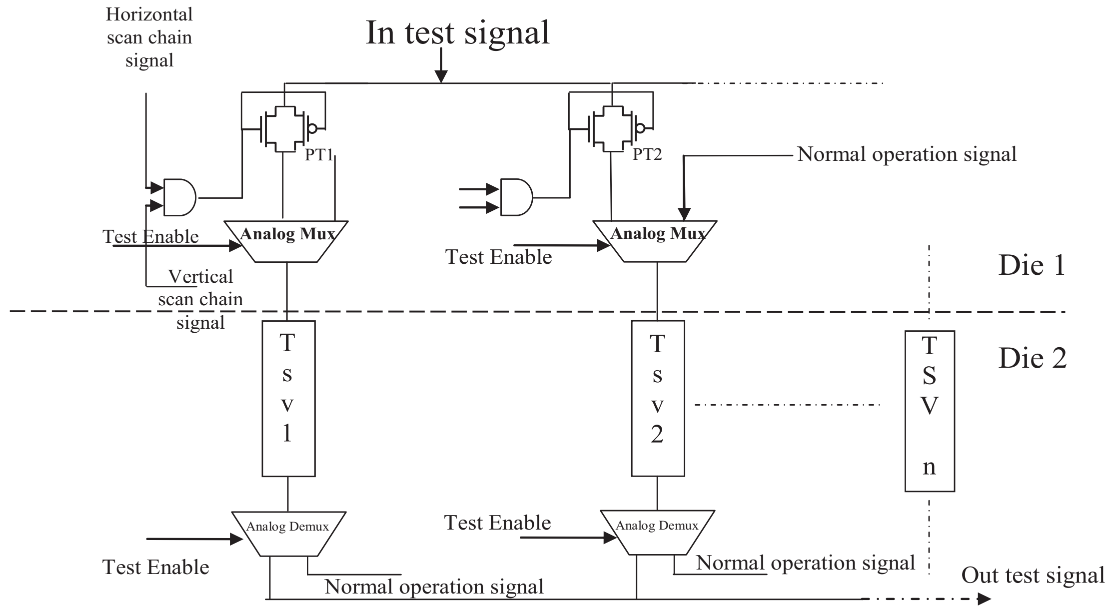

Figure 6. Internal structure of TSV connection block.

The TSV connection block is composed of transfer gates, analog multiplexers, and analog demultiplexers. Enabling the test-enable signal allows the connection of the lower terminal of PTi transfer gates to the upper terminal of the TSVs. Once the transfer gate is activated, the test signal is injected and transmitted through the correspondent TSV. Enabling the transfer gate depends on the activation of the connected AND gate. The transfer gate is activated upon receipt of activation signals (row enable and column enable) from the horizontal and vertical scan chain.

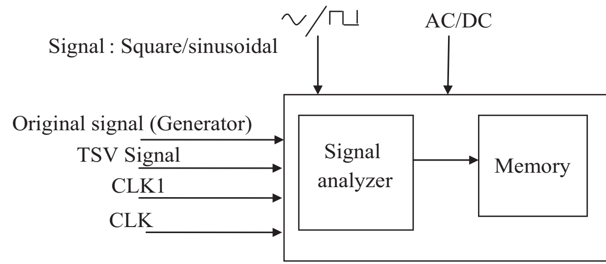

Figure 7. The diagnostic unit.

3.3. Diagnostic unit

The diagnostic unit analyzes signals crossed via TSVs to detect prospective defects.

AC/DC allows changing the test mode. The enabling of AC/DC input activates the AC signal test mode; on the other side the disabling of the input activates the continuous signal test mode. Continuous test mode (DC) is used to test TSVs crossed by continuous signals (power signals (DC) or ground signal (GND)). Alternative test mode (AC) is used to test TSVs crossed by dynamic signals (square or alternative signals). A defective TSV can modify the shape and the characteristics of an alternating signal crossing the TSV. The same defective TSV can allow the crossing of a DC signal without modifying it characteristics. Some TSV defects reduce the bandwidth and can change the characteristics of an alternating signal during its propagation through the TSV without affecting the characteristics of a continuous signal. In AC test mode, the type of injected signal can be a square or a sinusoidal signal according to the test requirements.

Figure 8 shows the detailed architecture of the signal analyzer.

The enabling of the DC test mode allows the crossing of the injected test signal through 2 comparators. Each comparator has a well-defined reference voltage (Vref1 for the first comparator and Vref2 for the second comparator with Vref1 $>$ Vref2, and Vref1 is set according to the degree of the selectivity of the test). If the voltage observed at the TSV is above Vref1, the outputs of both comparators will switch to the high state indicating the absence of defects. If the voltage received by the comparators is between Vref1 and Vref2, the first comparator output will switch to the low state while the output of the second comparator will maintain its high state indicating that the TSV is defective but repairable. If the voltages received at the comparators are below Vref1 and Vref2, the outputs of both comparators will switch to the low state, indicating that the TSV is defective and irreparable. If the AC test mode is enabled, we have the choice to activate either the square test mode or the sinusoidal test mode. If the square test mode is selected, the TSV output voltage is connected to the inverters via analog multiplexers (Figure 8). The 2 inverters are used for the recovery and reconstruction of the signal in the case that the received signal is attenuated, distorted, or modified. If the received signal is emanating from a defective TSV, which can induce a signal propagation delay, the reconstructed signal through the gates will be delayed from the injected signal. In turn the recovered signal is connected to a capacitor and a resistor. The current at the terminals of a capacitor is defined by the following formula:

$$i(t) = Cdu/dt. \quad (1)$$

The current is assumed to be zero for all the DC components of the signals. For a square wave, the current is present only during transitions. An RC circuit is then connected to a TSV. The RC circuit is connected in turn to a built-in-current sensor (BICS) to signal each transition by intercepting induced current by the capacitor.

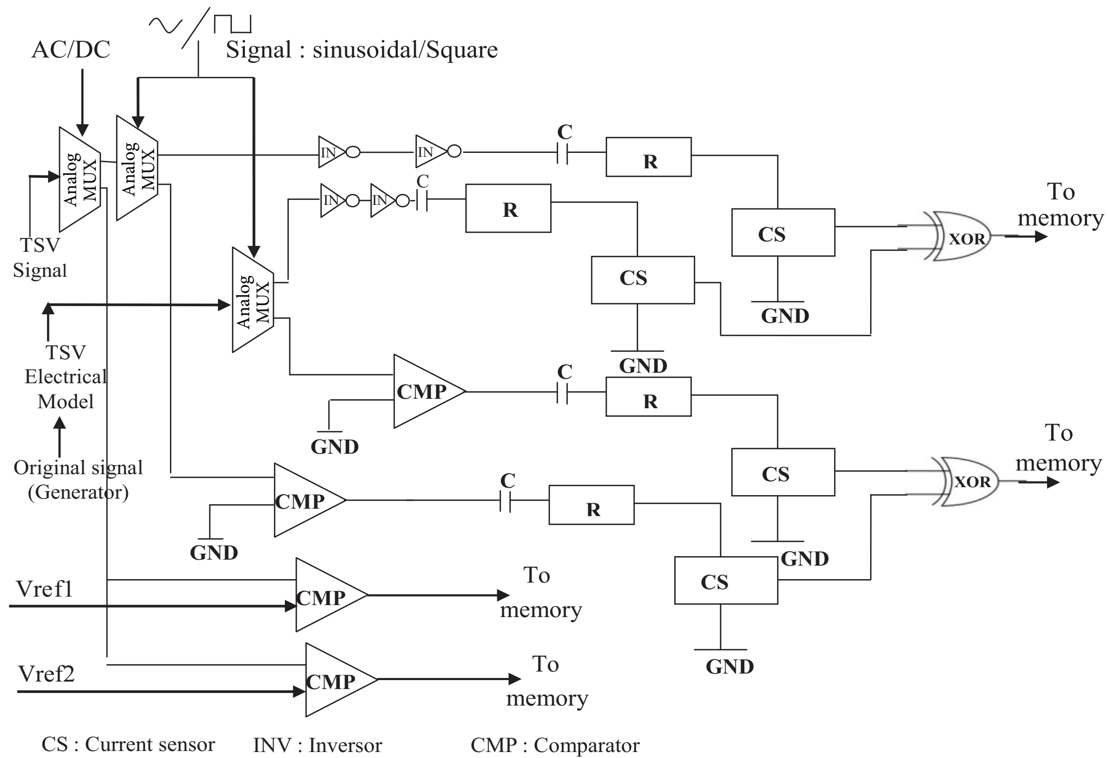

Figure 8. Internal structure of the signal analyzer.

The signal injected by the generator is in turn connected to an RC circuit and a BICS to signal transitions. A phase difference between the outputs of the 2 BICS indicates the presence of a defect. If the sinusoidal mode is selected, the signal observed at the TSV is connected to a comparator in order to turn the sinusoidal signal into a square signal. The signal delivered by the comparator is connected to an RC circuit and a BICS to detect transitions. The signal injected by the generator is in turn connected to a comparator, an RC circuit, and a BICS. The BICS signals are compared with respect to time. The simultaneous signaling of BICS signals (presence of a current) indicates the absence of defects. A time lag at the BICS signaling indicates the presence of a defect.

4. Simulation of the proposed testing technique

4.1. TSV electrical model

To study the impact of TSV defects on the signal quality, Spice simulations have been performed on a TSV represented by its equivalent circuit model. Simulations of the proposed test technique have been also performed. Simulations have been done to demonstrate the impact of the TSV defects on the quality of alternating signals and the capability of the diagnostic unit to detect these defects.

The electrical model of the TSV is represented by an RLC network as shown in Figure 9 [21]. The model was successfully validated by measurements and simulations [21].

The TSV model is selected to perform simulations. We use the values of TSV components reported in [21].

The Table details the parameters (diameter, resistance, and capacitance) of a functional TSV on which simulations have been performed.

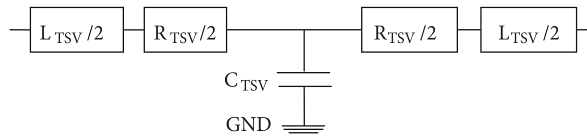

Figure 9. Electrical model of TSV.

Table. TSV settings chosen to perform simulations.

D (μm)	Ltsv (Ph)	Rtsv (mΩ)	Ctsv (ff)
5	34.47	18.6	69.98

4.2. System response following injection of a sinusoidal signal in a functional TSV

Figure 10 shows the Spice diagram used in the simulations.

Figure 11 presents the shape of the injected signal, the signal observed at the out terminal of a functional TSV, the BICS signal, and (pass/fail) signal.

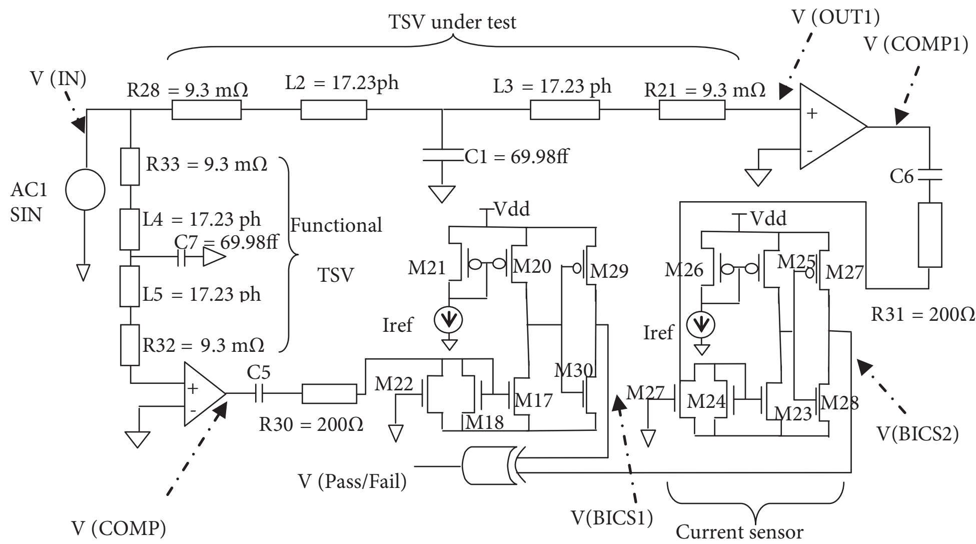

Figure 10. Diagram used to perform Spice simulations.

We can notice that the signal observed at the output of the TSV is identical to the injected signal. The BICS output moves to the high state at the same time, indicating the absence of defects. The pass/fail signal remains in the low state throughout the simulation, indicating the absence of defects.

4.3. System response after the injection of a sinusoidal signal in a defective TSV

A sinusoidal signal with a frequency of 4.0 GHz is injected into a defective TSV. The defect is caused by the increase of the value of the R28 and R21 resistors (Figure 9). The value of the R28 and R21 resistors used during the simulation is 500 Ω. The shapes of the injected signal V (IN) and the signal observed at the output of the defective TSV V (OUT1) are shown in Figure 12.

According to Figure 12, we can see that the signal observed at the output of the defective TSV has been modified compared to the original signal. The changes are seen as a difference in the signal amplitude as well as a time shift.

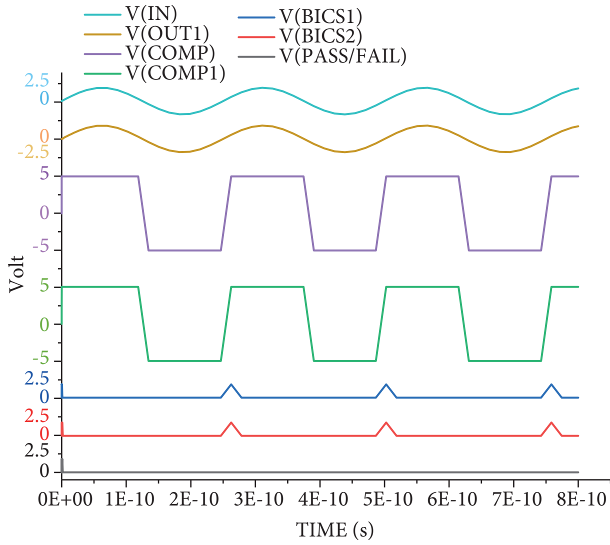

Figure 11. System response after the injection of a sinusoidal signal in a functional TSV.

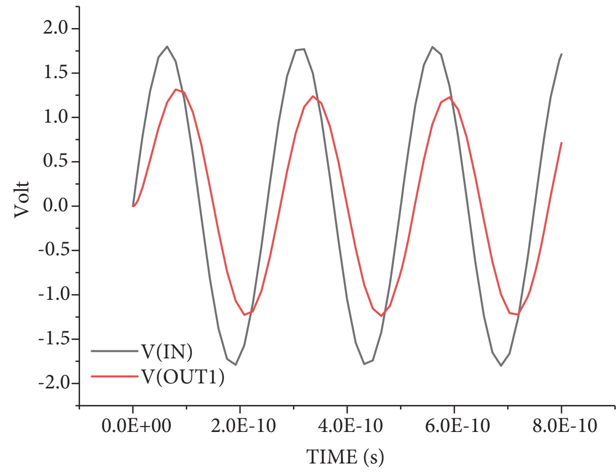

Figure 12. V (IN) and V (OUT) signals after the provocation of the defect.

Figure 13 shows the response of the system through the various signals observed upon injection of a sinusoidal signal at a defective TSV.

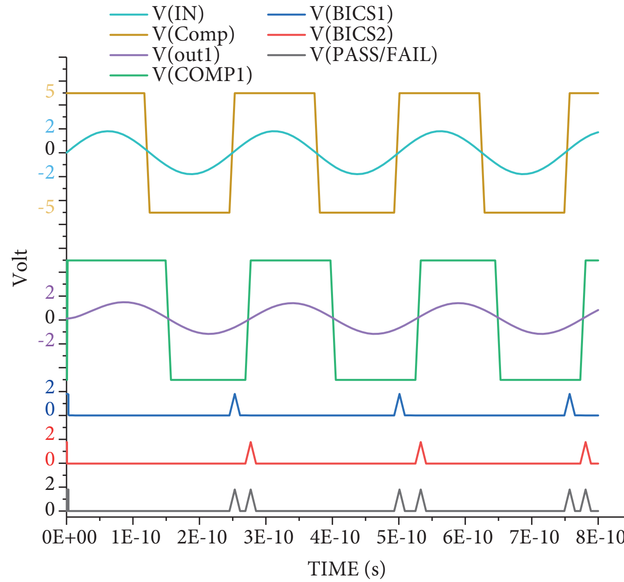

Figure 13. System response after the injection of a fault in the TSV.

According to Figure 13, we can notice that the defect injected at the TSV has been detected by the analyzer. The time shift at the output signals of BICS has been detected. The pass/fail signal switches to the high state, indicating the presence of a defect.

4.4. System response following injection of a square signal in a defective TSV

Figure 14 shows the Spice model of the circuit used to perform simulations.

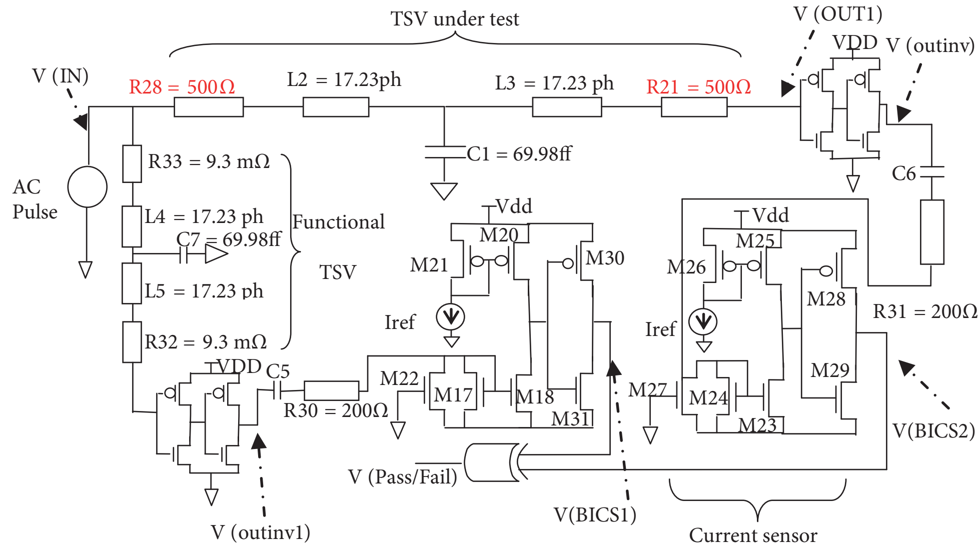

Figure 14. Diagram used to perform Spice simulations.

A square signal with a frequency of 4.0 GHz is injected into the defective TSV. The defect is caused by the increase in resistance values R28 and R21 (Figure 14).

The value of the R28 and R21 resistors used during the simulation is 500 Ω.

Figure 15 represents the waveforms of the injected signal V (IN), the TSV's output voltage V (OUT1), and the output signal of the 2 inverters V (OUTINV) after the injection of the defect.

According to Figure 15 we can see that the injection of the defect causes a change in the shape of the signal. After the reconstruction of the signal through inverters, we can notice that the reconstructed signal has roughly the same shape as the original signal but shifts in time. We can also notice an increase in the rise time and the fall time of the signal.

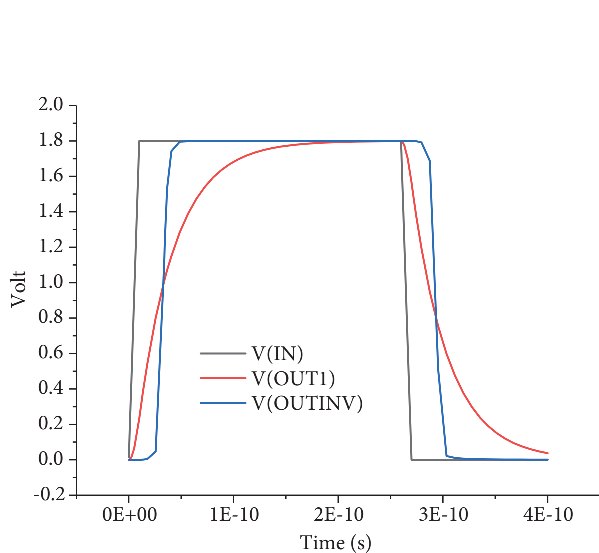

Figure 15. Signal waveform after the injection of a defect in the TSV.

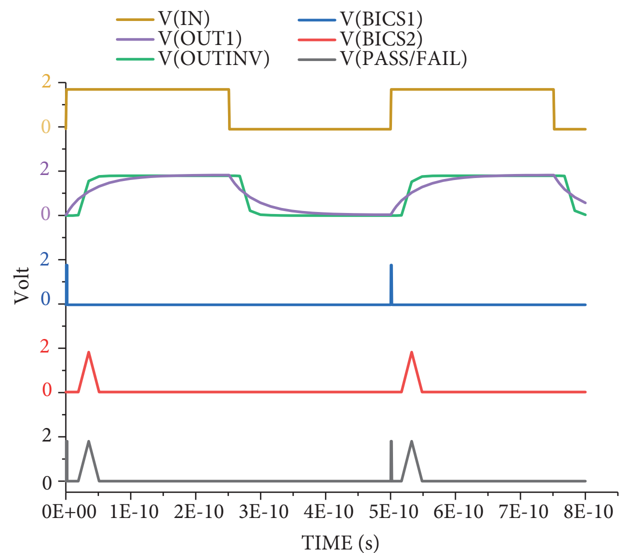

Figure 16. System response after the provocation of a defect in the TSV.

Figure 16 shows the response of the system through the various signals observed upon injection of a square signal at a defective TSV.

From Figure 16 we can see that the fault injection leads to a time shift in the signaling of the 2 BICS. The defect is detected and the XOR gate output signal (pass/fail) goes to the high state each time there is an anomaly.

5. Conclusion

In this paper, we presented a technique for accessing the inner layers of integrated circuits and 3D TSV testing. The access is realized through a multiplexing approach based on a matrix architecture. The test is performed by a diagnostic unit placed outside the circuit under test. The effectiveness of the proposed technique is proved by Spice simulations. The simulation results are conclusive and satisfactory.

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