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An efficient structure for T-CNTFETs with intrinsic-n-doped impurity distribution pattern in drain region

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Abstract: In this paper, by using impurity distribution engineering of drain region, an efficient structure is proposed for tunneling carbon nanotube field-effect transistors (T-CNTFETs). The drain region of the proposed structure consists of two parts. The impurity density of the part close to the channel is intrinsic and the other is n-type with constant density of 1 nm^{-1}. In conventional T-CNTFETs, heavily doped drain causes a spiky drop of potential energy around the channel to drain junction resulting in a pathway for carriers in the valence band to tunnel to the conduction band which means ambipolar behavior and large leakage current. The proposed structure expands the longitudinal distance between the bands at this junction and reduces the band-to-band tunneling (BTBT) and improves leakage current and ambipolar behavior. Moreover, current ratio, delay time, power delay product, cut-off frequency, and subthreshold swing as important characteristics are enhanced so that the proposed structure can be more attractive for circuit designers. Also, design considerations for intrinsic region length were done and mentioned. To simulate the devices, self-consistent solution of Schrodinger and Poisson equations and nonequilibrium Green's Function method were employed.

Key words: Tunneling carbon nanotube field-effect transistor, off current, current ratio, band to band tunneling, nonequilibrium Green's function

1. Introduction

Metal-oxide-semiconductor field-effect transistor's (MOSFET) channel length continues to shrink rapidly toward very small dimensions. Due to the reduction in size of the devices based on silicon and the claim of enhancing the switching and reducing the power consumption, the tendency to use new materials such as carbon nanotubes to replace the conventional Si in nanometer devices has increased [1–3]. Carbon nanotube field-effect transistor (CNTFET) is one of the possible choices to replace silicon-based transistors. They are especially interesting because their one-dimensional band structure suppresses backscattering and makes near-ballistic operation a possibility [4]. CNTs are interesting materials for nanoelectronic applications in terms of ballistic conduction for their long mean free path [5], which is of the order of a micrometer [6–8]. Because of these features, a considerable high-frequency performance for CNTFETs is expected. Researchers have been studying and developing the CNTFET device behavior and its applications [8]. They divided the transistors based on carbon nanotubes into two groups: Schottky-Barrier CNTFETs (SB-CNTFETs) with metallic source/drain regions and MOS-like CNTFETs (MOS-CNTFETs) in which source and drain regions are heavily doped CNTs instead of the metallic parts [9–11]. Most CNT devices operate as SB-CNTFETs due to formation of barrier at border

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of CNT to metal contacts. However, their large subthreshold swings, small On/Off current ratio, large power consumption, and strong ambipolar behavior are among the factors which limit their performance in applications like logic circuits [11–13]. MOS-CNTFETs, due to heavily doped source and drain regions, show advantages over SB-CNTFETs. In this type of transistors, subthreshold swing is reduced and On/Off current ratio is increased. Also, lower power consumption and better ambipolar behavior are their other advantages in comparison with SB-CNTFETs [9,12]. The MOS-like structure has better performance but it does not mean that all of its characteristics are ideal. Similar to other structures and technologies, MOS-CNTFETs need to be improved to obtain more reliable devices.

One of the sources for power dissipation is the static power consumption that originates from the leakage current when the transistor is at Off regime. In fact, leakage current is caused by the ambipolar behavior and band-to-band tunneling (BTBT). Ambipolar behavior and BTBT which occur at gate reverse voltages (i.e., at high leakage current) are among the important issues for MOS-CNTFETs [12,14], and should be well addressed in simulations. Some researchers examined these issues and suggested several methods [11,12,15–24]. These methods include the change in impurity concentration [11,15–17], bandgap engineering [12], use of linearly and lightly doped impurity injection in source and drain regions [11], underlap engineering [18,20], and use of gate insulators with asymmetrical thicknesses [19], and so on. To improve power consumption and save energy, the T-CNTFETs were proposed [14,24,25]. The subthreshold swing theoretical limit for MOS-CNTFETs is 60 mV/dec at room temperature, but T-CNTFETs have much better subthreshold swing than the MOS-like structure; therefore, these devices are proper candidates for applications with very low power consumption [2–9,26]. Despite desirable characteristics such as low power consumption, T-CNTFETs suffer from drawbacks such as small current ratio [9,24]. To benefit from the advantages of T-CNTFETs and improve their drawbacks, in this paper, a new T-CNTFET whose drain region contains two parts with different impurity distributions is proposed. Impurity density of the drain part close to the channel is zero and the other part is heavily doped. This structure is called tunneling carbon nanotube field-effect transistor with intrinsic-n-doped impurity distribution pattern in the drain region (p-i-i-n T-CNTFET). To study and simulate the proposed device specifications, the self-consistent solution of Poisson–Schrodinger equations and nonequilibrium Green's function (NEGF) were applied. Tight binding approximation with only p_z-orbital was employed. The results of the simulation show that the proposed structure has lower Off current than the conventional structure (T-CNTFET). Moreover, the new structure has better On/Off current ratio and subthreshold swing. Furthermore, frequency analysis reveals improvement in device characteristics.

The rest of this paper is presented as follows. After Introduction, Section 2 provides the method and applied simulation model for T-CNTFET. In Section 3, a proposed device structure is introduced with related details. Section 4 provides the electronic features of the transistor using the results of simulation and the required comparisons. Each section contains results and discussion of its own. Finally, Section 5 presents the conclusions.

2. Simulation process

For simulation of nano-scale devices, the nonequilibrium Green's function method is widely used. This method provides an excellent framework for analysis and simulation of these devices and includes a self-consistent process between the electrostatic potential and charge distribution [14,26]. A self-consistent Schrodinger–Poisson solver that utilizes the finite difference (FD) method to convert the Schrodinger and Poisson equations into matrices was developed. To simulate these devices, it is necessary to solve the Poisson and transport equations. The

Poisson equation was solved by means of Newton–Raphson method. Poisson equation provides the potential for a given charge density and transport (Schrodinger) equation was solved to obtain the density within the device for a certain potential [10,26]. In the semiclassical simulation, Boltzmann transport equation is used to calculate the transfer in the carbon nanotube for one-dimensional ballistic transport but in quantum simulation, the Schrodinger equation is solved [10,27]. The nonequilibrium Green's function (NEGF) method is used to solve the Schrodinger equation and to calculate the density of states, charge density, and finally the current. There are some stages in the NEGF method that are described in brief here. Primarily, the proper basis set and Hamiltonian matrix are determined for an isolated channel, and then the self-consistent potential is obtained to complete the Hamiltonian matrix. Then the self-energy matrices are calculated which describe how to couple the ballistic channel to the source and drain extensions. After calculating the Hamiltonian matrices and self-energies, the Green's function will be evaluated. Green's function is determined as follows [26,27]:

$$G_q(E) = [(E + i\eta^+)I - H - \sum S - \sum D]^{-1}. \quad (1)$$

In the above equation, I is the unit matrix, E is Energy, $\sum$S and $\sum$D are the drain and source self-energy matrices, η^+ is a positive infinitesimal value and H is the Hamiltonian matrix of the carbon nanotube. Poisson equation calculates nanotube potential distribution due to boundary conditions (such as gate voltage) and the charge density on the nanotube (electrostatic solution of the problem). This potential distribution is used as the input for the transport equation. Transport equation obtains a new charge density in the nanotube and provides it as an input for the Poisson equation. These repetitions between the two equations continue until a self-consistency is created. In fact, a loop between the Poisson equation and quantum transport is created and this loop continues until convergence is achieved. Finally, current is calculated by the following equation [10,14]:

$$I = \frac{2q}{h}\int T(E)[F(E - E_{FS}) - F(E - E_{FD})]dE, \quad (2)$$

where, E_{FS} and E_{FD} are the source and drain Fermi levels, q is the quantum charge, h is Planck's constant, and T(E) is the transport coefficient calculated by the following equation [1,10]:

$$T(E) = trace(\Gamma_S G \Gamma_D G^+), \quad (3)$$

where G is the Green's function and $\Gamma_{S\,(D)}$ is the energy level expansion due to source and drain junctions obtained from the following equation [10,14]:

$$\Gamma_{S(D)} = i(\sum_{S(D)} - \sum_{S(D)}^{+}) \quad . \quad (4)$$

More details can be found in [4,9,15–23].

3. Device structure

The two-dimensional views of the proposed device and the conventional structure are shown in Figure 1. In these structures, a zigzag-type carbon nanotube (13,0) with a hafnium dioxide (HfO_2) as dielectric material with thickness of 2 nm and dielectric constant of 16 is considered for this gate all around the structure. The device operates at room temperature (300 °K). The gate length is 20 nm and the drain (source) length is 30

nm. In case of change in the length of regions, it will be clearly mentioned in the descriptions. The impurity in the source side is P-type at the fixed value of 1 nm^{-1}. The drain region consists of two parts: the area of the drain near the channel is intrinsic and the other side is n-type with fixed density of 1 nm^{-1}. The length of the drain intrinsic region is 20 nm and the doped region length is 10 nm. The doping distribution at each part is uniform.

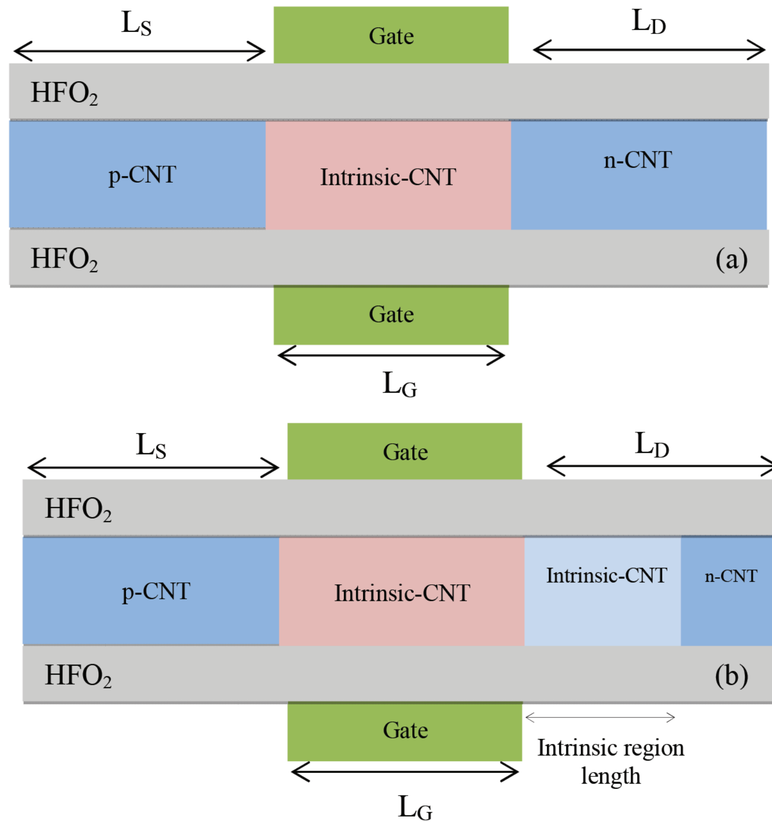

Figure 1. A 2-D cross-sectional view of a) the conventional and b) the proposed structure.

4. Simulation results and discussion

4.1. Simulation results

To prove the accuracy of our model, we simulated a CNTFET with the same configuration as that reported in [28]. Figure 2 illustrates the simulated (stars) drain current versus gate-source voltage characteristic and compares it with the experimental result (dashed line) in [28]. The CNT diameter is about 1.5 nm and gate oxide is 8 nm thick HfO_2 with dielectric constant of ε_r=16. Good agreement between the experimental and modelling results verifies the reliability and accuracy of our model. In this section, the electrical characteristics of T-CNTFET with p-i-i-n doping distribution pattern versus conventional T-CNTFET will be discussed. It is worth mentioning that the total areas of the compared structures are equal and there is no area penalty associated with our proposed structure. Comparison between the two structures is done along the same source, drain and channel lengths, and under the same bias conditions. Drain current diagram versus drain-source voltage in three different voltages, V_{GS} = 0.4 V, V_{GS} = 0.5 V, and V_{GS} = 0.6 V, is shown in Figure 3 for both structures. Drain-source current diagram versus drain-source voltage is plotted for fixed channel length of

20 nm. According to Figure 3, it can be seen that for the given gate-source voltages, the saturation current of p-i-i-n and conventional structures are nearly the same for drain-source voltages between 0.3 and 0.5 V or in other words, their current capability for sensing applications are similar at saturation regime.

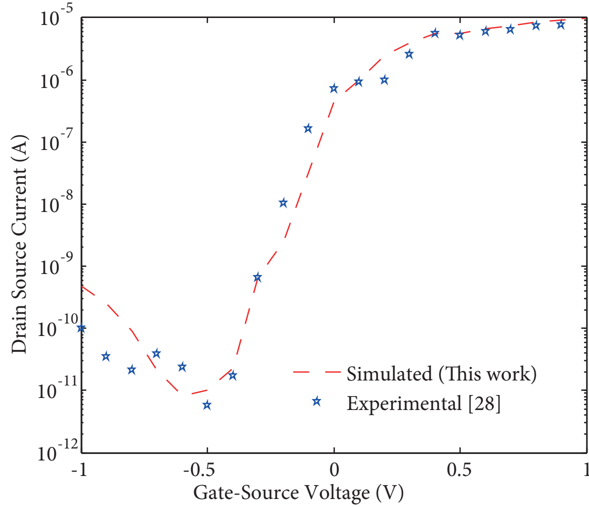

Figure 2. Comparison of the simulated drain-source current versus gate-source voltage characteristic (dashed line) with that obtained experimentally in [28] at the same bias of V$_{DS}$ = 0.5 V.

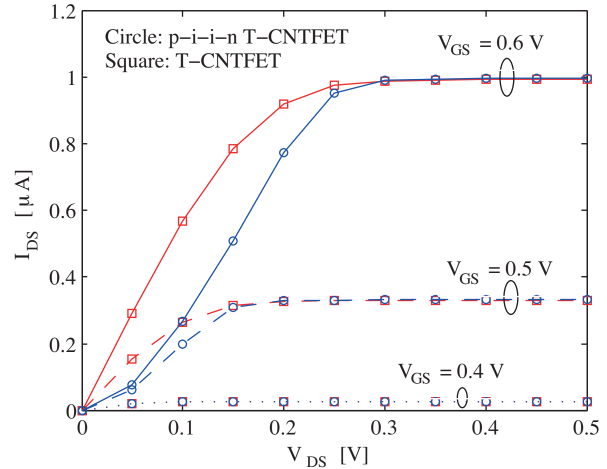

Figure 3. $I_D - V_{GS}$ diagram output feature of p-i-i-n T-CNTFET and T-CNTFET structures at different source-gate voltages.

In nano devices, since the drain-source voltage (V$_{DS}$) at small scales is not reduced similar to the channel length scaling, their power density increases. As a result, in MOS-CNTFETs with small sizes, the Off state leakage current is significantly increased at these approximately high drain-source voltages due to tunneling at the source/drain to channel junctions. In fact, the leakage current is generated due to ambipolar behavior of the device resulting from band-to-band tunneling at off regime [11–13]. This issue increases the regional charge mass in the channel and prevents the gate to change the state of the device from On to strong Off mode. As a result of reducing the size (i.e., increased leakage current), these devices are faced with challenges because of restrictions on power consumption. Figure 4 presents the drain current in terms of gate-source voltage for the studied structures at three different voltages of V$_{DS}$ = 0.2 V, 0.4 V, and V$_{DS}$ = 0.5 V. The results of simulation show that the Off current and ambipolar behavior in p-i-i-n are significantly better than those of the conventional structure; therefore, in terms of power consumption at off regime, our proposed structure shows better performance. In the p-i-i-n T-CNTFET structure, because of the intrinsic part at the drain region near the channel, the tunneling barrier at the junction between channel and drain is modified and widened. Thus, band-to-band tunneling probability is reduced and consequently the leakage current suppressed. For the studied channel length and applied biases, p-i-i-n has smaller leakage current compared to its conventional counterpart. Heavily doped extensions create a spiky drop in the energy diagram around the gate, which results in a pathway for electrons in the valence band to tunnel to the conduction band and makes larger leakage current. To illustrate the coverage of the tunneling barrier between the channel-drain region, Figure 5 presents the energy band diagram along the CNT for p-i-i-n and basic structures both biasing at V$_{GS}$ = −0.2 V and V$_{DS}$ = 0.4 V. Longer horizontal distance between conduction and valance bands at drain side of the channel is apparent for p-i-i-n structure which demonstrates stronger tunneling barrier for this structure. BTBT results from the discrete quasi-bound states in the channel that can create the tunneling path between the occupied states on

one side and the unfilled states on the other side. In the proposed structure, longer horizontal distance between conduction and valance bands reduces the number of these quasi-bonds and their effectiveness in creation of tunneling current. Positions of these energy levels and the edges of the corresponding source and drain bands as well as their numbers conclude the amount of the tunneling current.

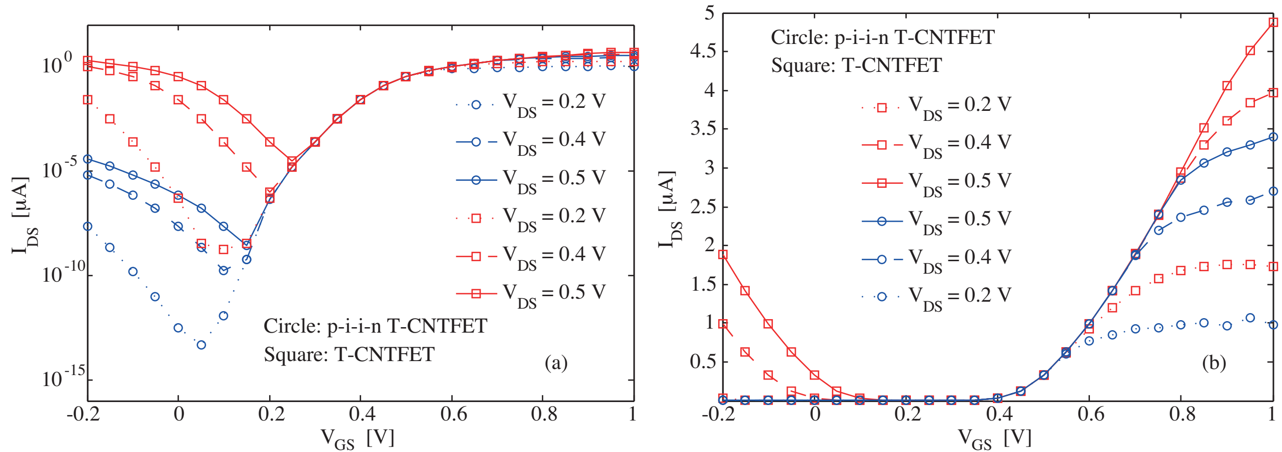

Figure 4. $I_D - V_{GS}$ curves for both structures at different drain-source voltages; a) logarithmic scale, b) linear scale.

Figure 6 presents the On/Off current ratio based on the leakage current in the logarithmic scale for both structures under study. Two channel lengths, 10 and 20 nm, are studied. According to the figure, at channel length of 20 nm, it can be observed that maximum current ratio in the conventional structure is about 10^6 while this value for the p-i-i-n T-CNTFET structure is roughly more than 10^9. Thus, our proposed structure outperforms its conventional counterpart in terms of current ratio and off current. The proposed structure has desired current ratio features due to reduced probability of band-to-band tunneling. In other words, in Figure 6, it is obvious that the conventional structure results in higher leakage currents than the p-i-i-n structure at equal current ratios.

One of the most important parameters while reducing the size of transistors is subthreshold swing. This

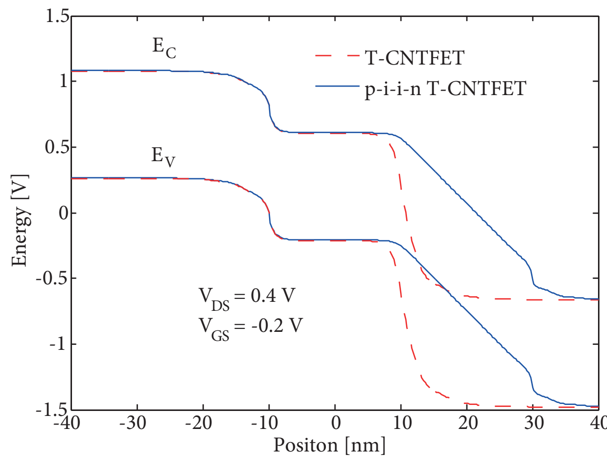

Figure 5. Energy band diagram along the device for both structures.

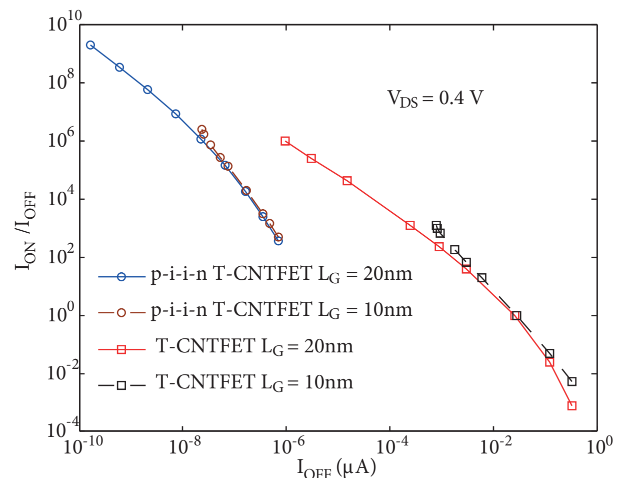

Figure 6. On/Off current diagram versus Off current for both structures.

parameter indicates the power consumption at subthreshold state for short-channel devices. The subthreshold swing theoretical limit for MOS-CNTFETs is 60 mV/dec at room temperature. Tunneling CNTFETs result in a subthreshold swing smaller than the theoretical limit; thus, these devices are attractive for applications with low power dissipation. Subthreshold swing is calculated by the following formula [10]:

$$SS = \Delta V_{GS}/\Delta \log(I_{DS})(mV/dec). \tag{5}$$

Subthreshold swing diagram in terms of applied gate-source voltage where the channel length is 20 nm and V_{DS} = 0.04 V and 0.4 V for the proposed and the conventional structures is shown in Figure 7. As it can be observed in Figure 7, the proposed structure has a lower subthreshold swing than the conventional structure. The least amount of subthreshold swing for p-i-i-n T-CNTFET and T-CNTFET structures at V_{DS} = 0.4 V and V_{GS}= 0.15 V are 28.9 mV/dec and 41.3 mV/dec, respectively. This significant difference in the subthreshold swings of the studied structures is a consequence of the differences observed in the corresponding band structures shown in Figure 5 due to the p-i-i-n distribution pattern. As mentioned in Eq. 5, subthreshold swing is the inverse of current-voltage variation slope at subthreshold regime. Figure 5 illustrates the band structure of both devices at subthreshold regime. It can be seen that in the proposed structure, the horizontal distance between valance and conduction bands at junctions is longer than the conventional structure and consequently the probability of tunneling current in the proposed structure is lower than its conventional counterpart. Also, Figure 4a shows that the proposed structure moves from subthreshold to saturation regime with higher slope than the conventional structure because the difference in their leakage current is higher than the difference in their saturation current. Thus, subthreshold swing is improved in the proposed structure.

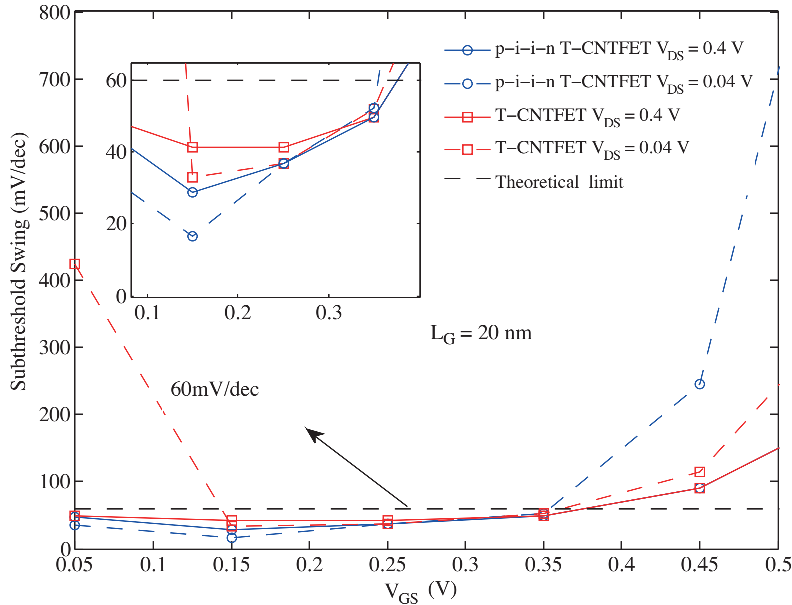

Figure 7. Subthreshold swing diagram versus V_{GS} for p-i-i-n T-CNTFET and T-CNTFET.

Two other key parameters in the study of On-Off switching behavior for digital applications of T-CNTFETs are delay time (τ) and power delay product (PDP). These two parameters are calculated by the following equations [11,25]:

$$\tau = (Q_{ON} - Q_{OFF})/I_{ON}, \tag{6}$$

$$PDP = (Q_{ON} - Q_{OFF})V_{DD}. \tag{7}$$

Figure 8 presents power delay product and the delay time diagrams against saturation current at $V_{DS} = 0.4$ V for p-i-i-n and conventional T-CNTFET structures. According to the simulation results, it can be seen that the suggested structure has better switching characteristics than the conventional structure. In other words, the delay time and power delay product in the p-i-i-n T-CNTFET structure are less than the T-CNTFET structure at equal saturation currents. It should be noted that simulations were evaluated for Off current mode at $V_{DS} =$ 0.4 V and $V_{GS} = 0$ V and On current at $V_{DS} = 0.4$ V and $V_{GS} = 0.4$ V. Figure 9 reproduces those comparisons in terms of current ratio. It can be seen that p-i-i-n T-CNTFET structure has better performance in comparison with the conventional structure at equal current ratio, making it more attractive to device and circuit designers for digital applications. Therefore, the proposed structure is a suitable candidate for applications with high speed and low power consumption. To study the high frequency and RF behavior of nano-scale transistors, obtaining the intrinsic cut-off frequency is mandatory. The cut-off frequency is calculated by the following equation [24]:

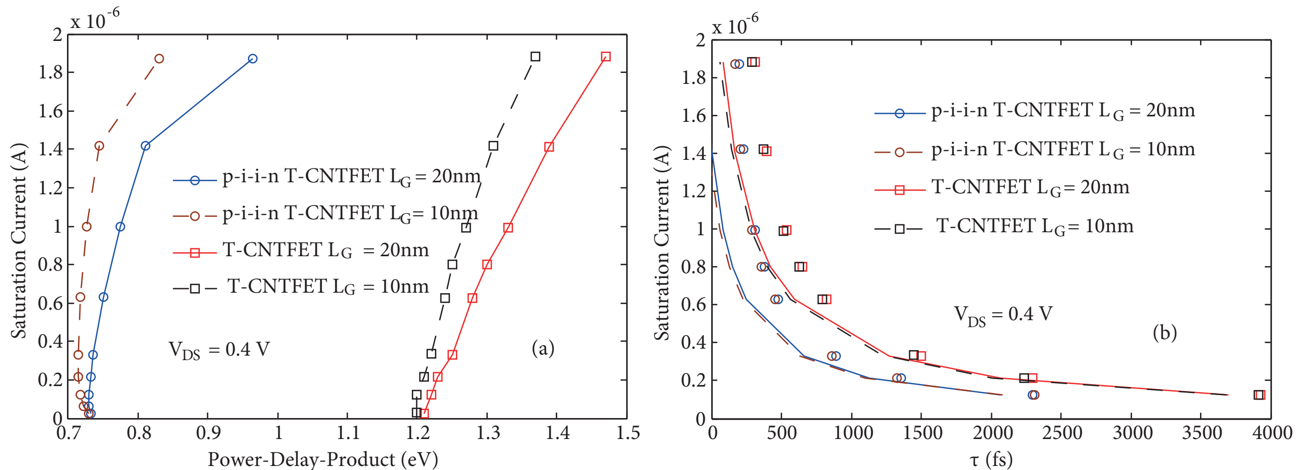

Figure 8. Saturation current versus a) power delay product and b) delay time of the p-i-i-n T-CNTFET and T-CNTFET structures in $V_{DS} = 0.4$ V.

$$f_T = \frac{g_m}{2\pi C_g}. \tag{8}$$

The cut-off frequency parameter is calculated after calculating transconductance (g_m) and gate capacitance (C_g) by the following equations, where Q_g is the total charge in the channel region [24]:

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} |_{V_{ds}} , \tag{9}$$

$$C_g = \frac{\partial Q_g}{\partial V_{gs}} |_{V_{ds}} . \tag{10}$$

Transconductance and gate capacitance diagrams in terms of applied gate-source voltages where the channel lengths are 10 and 20 nm and $V_{DS} = 0.5$ V for the proposed and the conventional structures are shown in Figure 10. Simulation results demonstrate that the transconductance of the p-i-i-n structure is approximately equal to

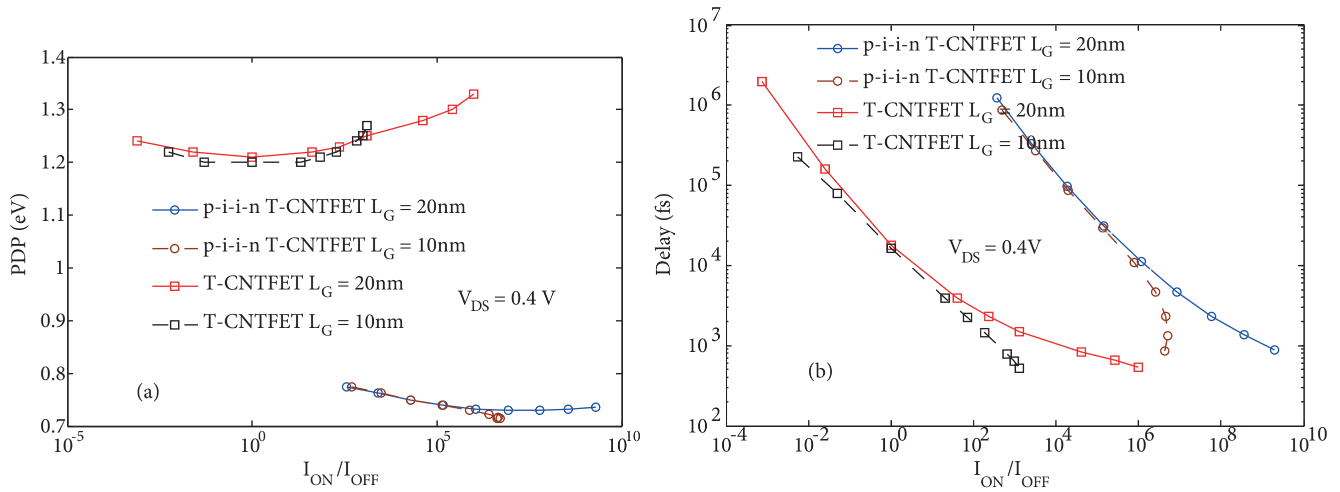

Figure 9. Current ratio versus a) power delay product and b) delay time of the p-i-i-n T-CNTFET and T-CNTFET structures in $V_{DS} = 0.4$ V.

its conventional counterpart while the proposed structure has lower gate capacitance than the conventional T-CNTFET with similar configuration. It should be mentioned that in the experimental approach, g_m is directly obtained from I_D-V_{GS} characteristics which show I_D-V_{GS} slope. In the experimental approach, it is assumed that at saturation regime, this slope is constant and just a constant value is reported as g_m or sometimes different slopes are extracted and an average value is reported as g_m. It is obvious that at saturation regime, the I_D-V_{GS} slope is not constant; thus, we reported different slopes at different V_{GS} and Figure 10 shows gm dependence to gate voltage. Cut-off frequency diagram versus gate-source voltage is shown in Figure 11 for both structures. According to Figure 11, it can be observed that increasing the gate-source voltage leads to increase in cut-off frequency and also the proposed structure has higher cut-off frequency than the conventional structure. As an example, the numerical value of cut-off frequency for the p-i-i-n T-CNTFET and T-CNTFET structures for the channel length of 20 nm and $V_{DS} = 0.5$ V, $V_{GS} = 0.6$ V are 1.31 THz and 800 GHz, respectively, which shows more than 60 percent improvement. The reason for increase in f_T of the proposed structure is the significant reduction in gate capacitance. Increasing the cut-off frequency proves that in addition to the pre-mentioned improvements, the proposed structure can be considered as a good candidate for high-frequency applications.

4.2. Intrinsic region length effect

In our simulations, we fixed the length of drain at 30 nm, its intrinsic region length at 20 nm, and the length of the doped part of drain at 10 nm. To study further and obtain better insight into the proposed device performance, in this section, the total drain length is kept at 30 nm and by variation in the length of the intrinsic part of the drain region, the important characteristics of the proposed device are evaluated. The results of the simulation are shown in the Table. For 5, 10, 15, 20, and 25 nm length, current ratio, subthreshold swing, cut-off frequency, delay, and PDP are evaluated. All the studied p-i-i-n structures outperform their conventional counterpart. The overall obtained results show that as the length of the intrinsic part of the drain increases, the device has better performance in terms of all evaluated characteristics. Thus, the designer should choose the longer length for the intrinsic region as much as possible. Nevertheless, in increasing the intrinsic region, an important issue should be considered. This issue is the connection of the doped CNT to drain metal. Source and drain leads are

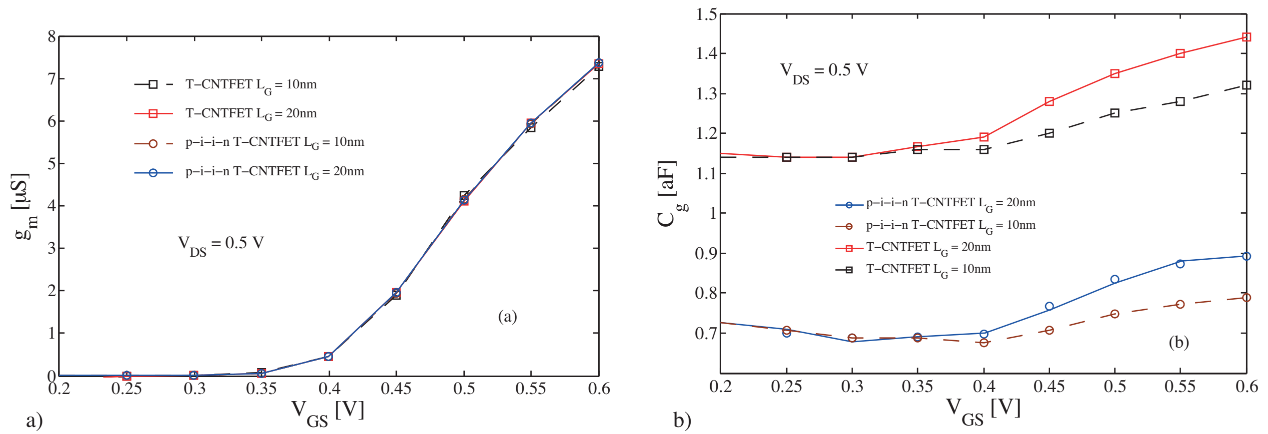

Figure 10. a) Transconductance versus gate-source voltage, b) gate capacitance versus gate-source voltage.

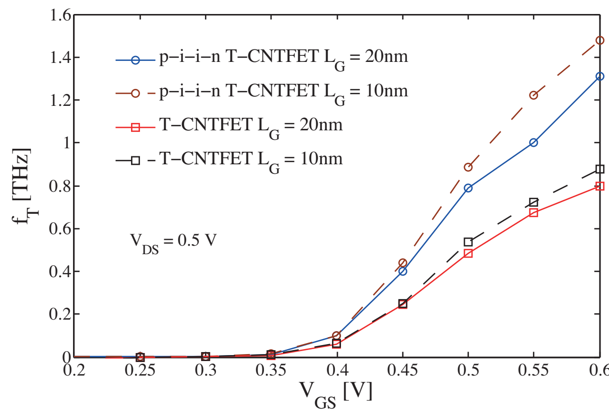

Figure 11. Cut-off frequency versus gate-source voltage in $V_{DS} = 0.5$ V.

connected directly to CNT interconnects or other CNTFETs, which means that both leads are of ohmic type contacts. Schottky barriers add additional resistances which make it harder for the carriers to transport into the contacts via thermal emission or tunneling. For the proposed structure, this connection should be ohmic, and Schottky junction must be avoided. The existence of the region with high impurity at the end of the drain makes the energy barrier at CNT to metal connection very narrow such that the carriers can tunnel through this barrier easily creating a connection with the ohmic characteristics and preventing the creation of Schottky barrier. If this region is very small, ohmic contact would be weak and the connection becomes Schottky type. Thus, the device designer should take this issue into account and keep the intrinsic length of the drain region not too long. It is worth mentioning that by selection of a metal with proper work function, the Schottky barrier can be avoided, too. From all simulations and investigated lengths, for 30 nm drain length, it seems that the p-i-i-n structure with 20 nm intrinsic part for the drain region is an appropriate selection.

5. Conclusion

In this paper, for the tunneling carbon nanotube field-effect transistors, a new structure which uses the drain region with intrinsic-n-doped impurity distribution pattern is proposed. To study and simulate the characteristics of the proposed device, self-consistent solution of the Schrodinger and Poisson equations and

Table. Device characteristics at different lengths of the intrinsic area of the drain.

Parameters	Drain side intrinsic region length of the p-i-i-n structure (total drain length is 30 nm and channel length is 20 nm)					Conventional
	Li = 5 nm	Li = 10 nm	Li = 15 nm	Li = 20 nm	Li = 25 nm	
Current ratio	5.43×10^3	2.61×10^5	2.13×10^7	2×10^9	1×10^{11}	1.3×10^3
SS (mV/dec)	38.15	36.67	36.63	28.90	19.27	41.34
Delay (fs)	1166	1005	931	889	864	1500
PDP (eV)	0.965	0.832	0.770	0.735	0.715	1.25
f_T (THz)	1.07	1.21	1.28	1.31	1.29	0.8

nonequilibrium Green's function method were used. The drain side intrinsic-n-doped impurity distribution widens the tunneling barrier at the channel to drain junction. This engineering in the impurity distribution improves leakage current and band-to-band tunneling. Simulation results indicate that the Off current of the proposed structure experiences a significant reduction compared with the conventional structure. Moreover, the new structure has higher current ratio and lower subthreshold swing. Due to the reduced delay time and power delay product and also higher cut-off frequency, it can be concluded that the proposed device structure is appropriate for the applications with low power consumption and high speed. Design considerations demonstrate that longer intrinsic part of the drain region results in better device characteristics by taking the potential barrier at the interface of CNT and metals into account.

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