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A data-aware write-assist 10T SRAM cell with bit-interleaving capability

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Abstract: Cell stability is becoming an important design concern as process technology continues to scale down. In this paper, we present a single-ended 10T SRAM cell that improves simultaneously both read static noise margin (RSNM) and write static noise margin (WSNM) by employing separate read buffer and power gating transistors, respectively. The cross-point write structure of the proposed cell facilitates bit-interleaved architecture to enhance soft-error immunity. Simulation is done on 65-nm CMOS technology on Cadence. Simulation results show that the RSNM of the proposed SRAM cell is 2.78 times and 1.47 times higher than those of the conventional 6T and Schmitt trigger-based 10T (ST-2) cells, respectively, at 0.4 V. The WSNM of the proposed design is 5.14 times larger than that of the two-port disturb-free 9T (TPDF9T) cell (without write assist) at 0.4 V. Write delay of the proposed cell is 77.56% less than that of the TPDF9T cell at 0.4 V. Leakage power dissipation of the proposed SRAM cell is 0.89 times that of the ST-2 cell at 0.4 V. The proposed cell occupies 1.34 times more area than the conventional 6T cell.

Key words: Bit interleaving, leakage power, SRAM, write ability

1. Introduction

SRAM is one of the major blocks in modern portable devices such as smart phones, laptops, and biomedical instruments. Battery-operated portable devices need to consume low power to prolong the battery life. Since SRAM occupies a large portion of the silicon die, it consumes a significant portion of the total power of today's VLSI circuits and hence the design of a SRAM with low power consumption is desirable. Down-scaling of supply voltage is considered an effective method to reduce power consumption. Supply voltage scaling reduces dynamic power quadratically and leakage power exponentially [1]. However, the static noise margin (SNM), which reflects the cell stability, is degraded when the supply voltage is reduced. Technology scaling has enabled enhanced integration density; however, process variation in submicron regimes severely degrades the cell stability under low-voltage operation [2]. Besides, for scaled technology, SRAMs are more susceptible to radiation-induced soft errors due to reduced charge at cell storage nodes. Due to higher integration density, a single particle strike upsets multiple cells; thus, soft errors also pose a challenge in the design of low-power SRAMs. At the circuit level, the radiation-hardened SRAM cell presented in [3] mitigates soft errors. At the system level, bit interleaving with an error correcting code (ECC) is an effective technique to mitigate soft errors. The conventional 6T (hereafter referred to as conv 6T) cell shown in Figure 1a offers a simple structure but suffers from read disturb and conflicting read versus write design requirements on access transistors. It consists of two cross-coupled inverters (M1–M2 and M3–M4) with two access transistors (M5 and M6), which connect the

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internal storage nodes (Q and QB) with the bit lines (BL and BLB). During read operations, a nonzero voltage developed at '0' storing node QB caused due to voltage division action between transistors M4 and M6 may turn on transistor M2, which results in an unintentional bit flip if not addressed properly. This is referred to as a read disturb problem. To avoid read disturb and to achieve high read stability, pull-down transistor M2 (or M4) must be stronger than access transistor M5 (or M6). However, for reliable write operation, access transistor M5 must be able to pull down the voltage of '1' storing node Q below the switching threshold of right inverter M3–M4. This requires that access transistor M5 (M6) be stronger than pull-up transistor M1 (M3). Thus, due to conflicting design requirements for the access transistor of the conv 6T cell, it is difficult to achieve high read stability and strong write ability simultaneously, particularly in the subthreshold region. Besides, in a bit-interleaved 6T SRAM array, half-selected cells (row-selected but column-unselected) undergo dummy reads during write operations. Therefore, the conv 6T cell does not support a bit-interleaved structure because of half-select disturbance [4].

Several configurations have been introduced recently to overcome the problems of the conv 6T cell. The design in [5] (Figure 1b) employs a separate read buffer that isolates the read bit line from the internal storage node. Thus, the cell achieves read SNM (RSNM) almost equal to hold SNM (HSNM). However, the 8T SRAM array also does not support bit interleaving because of its conv 6T-like write operation. Moreover, additional read bit line (RBL) leads to higher bit line leakage. The ST-2 SRAM cell [6], as shown in Figure 1c, employs two cross-coupled Schmitt trigger-based inverters. In this cell, positive feedback (because of Schmitt-trigger action) increases the switching threshold of the inverter storing logic '1' and therefore the cell preserves the logic '1' state. Thus, the cell offers enhanced read stability as compared to a conventional 6T cell. During write operations, Schmitt-trigger action is absent, which enables easy writing of the data. However, the ST-2 cell suffers from bit line leakage as it does not employ any mechanism to reduce leakage. The TPDF9T cell [7] (Figure 1d) employing a data-aware write scheme forces WBL to logic '0' during write operations. Write-wordline WLA (or WLB) is enabled to write a '0' (or '1') in the cell. Read disturb-free operation is performed through a separate read buffer. A cross-point addressing scheme enables bit interleaving to improve immunity to soft errors. However, this design requires an additional write-assist circuit, which consumes additional power and silicon area. In [8], a single-ended 9T SRAM cell (Figure 1e) employing power-gated transistors was proposed. This cell performs write '0' ('1') operation by weakening the pull-up (pull-down) transistor of the inverter that is fighting with the write access transistor. Like TPDF9T cells, this cell also supports bit interleaving to enhance soft error immunity. Since this cell utilizes two series NMOS transistors in the write path, the write '1' operation is difficult as an NMOS transistor does not pass a strong '1'. This cell also employs a write assist circuit to write data '1', which requires additional silicon area.

In this paper, we present a single-ended read disturb-free 10T SRAM cell (hereafter called the SEDF10T cell), which has following features:

(i) Power supply interruption write scheme [9] to improve write ability,

(ii) Separate read buffer to enhance read stability,

(iii) Single bit line to save area and bit line leakage power, and

(iv) Cross-point write structure for bit interleaving.

The remaining part of the paper is organized as follows: Section 2 describes the circuit diagram and various

operating modes of the proposed design. Section 3 presents simulation results and discussion. Section 4 provides a conclusion.

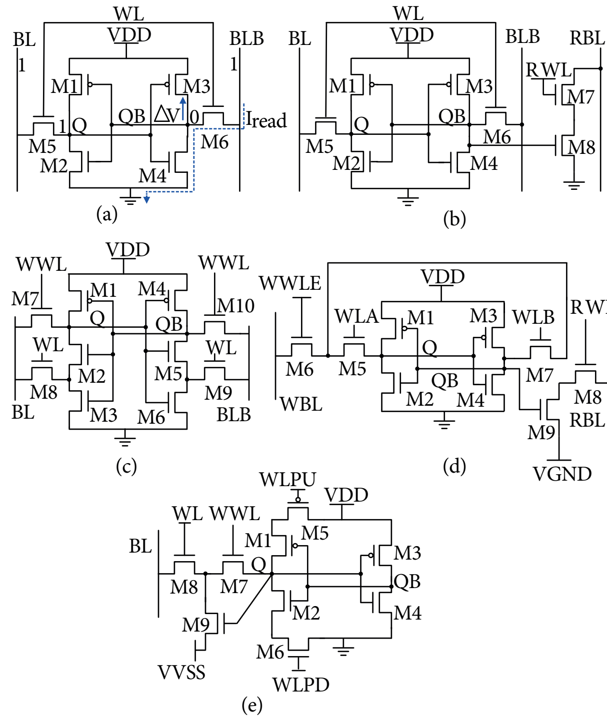

Figure 1. (a) Conventional 6T cell, (b) read-decoupled 8T cell [5], (c) ST-2 cell [6], (d) TPDF9T cell [7], and (e) power-gated 9T cell [8].

2. Proposed 10T SRAM cell

The schematic of the proposed SEDF10T SRAM cell is depicted in Figure 2. The proposed cell consists of a cross-coupled pair of inverters (M2–M3 and M5–M6) to hold the data at nodes Q and QB. Word line (WL) and word line 'A' (WLA) are row- and column-based, respectively, to form a cross-point structure during write '0'. Similarly, row-based WL and column-based word line 'B' (WLB) form a cross-point structure during write '1'. M1 is a power-gating transistor that cuts off the power supply of the left inverter when WLA is enabled for writing a '0' (Q = '0') in the cell. Similarly, M4 cuts off the power supply of the right inverter when WLB is activated to write a '1' (Q = '1' and QB = '0') in the cell. M7 and M8 are write access transistors while M9 and M10 form the read buffer through which bit line BL is discharged when virtual ground VVSS (row-based) is low. Table 1 shows the status of control signals during read, write, and hold modes.

Table 1. Control signals of proposed SRAM cell.

Operation	WL	WLA	WLB	VVSS	BL
Write '0'	'1'	'1'	'0'	'0'	'0'
Write '1'	'1'	'0'	'1'	'1'	'0'
Read	'1'	'0'	'0'	'0'	'1'
Hold	'0'	'0'	'0'	'1'	'1'

During read operations, BL is precharged to VDD while WLA, WLB, and VVSS are forced to ground. Now WL is activated to enable M9, which results in discharge of BL conditionally. For example, during read '0' operation (Q = '0', QB = '1'), BL is discharged by ground through M9 and M10, but during read '1' (Q = '1', QB = '0'), BL remains at precharged level VDD. Figure 3 illustrates the read '0' mode of the proposed SEDF10T cell.

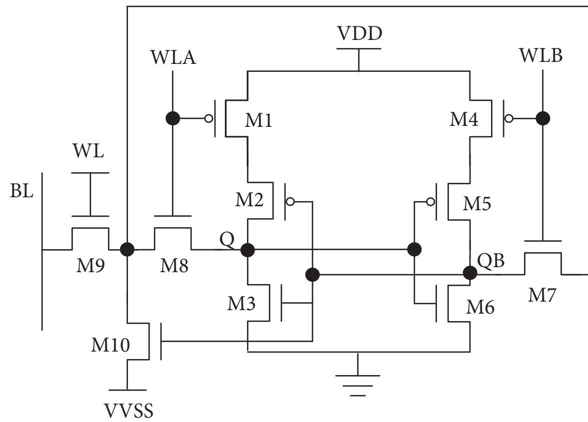

Figure 2. Schematic of the proposed SEDF10T SRAM cell.

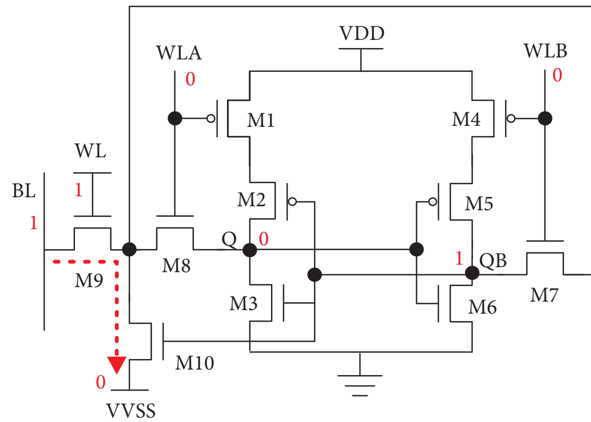

Figure 3. Proposed SEDF10T cell during read '0' mode.

During write operations, BL is forced to ground while WL is raised to VDD. Let us assume that initially node Q = '1'. To write a '0' in the cell, WLA is raised to VDD while WLB and VVSS are pulled to ground. OFF transistor M1 weakens M2, which results in faster discharge of node Q by BL through ON transistors M8 and M9. When node Q is pulled below the trip point of the right inverter, voltage at node QB begins to rise, the feedback loop starts to work, and the cell is flipped. After the write operation, the cell returns to hold mode. Figure 4a shows the write '0' mode of the proposed cell. For writing a '1' in the cell, WL and WLB are raised to VDD and WLA is made low. Now M4 is switched OFF to weaken transistor M5 and thus QB is discharged easily by BL through M7 and M9. Thus, logic '0' is stored at node QB and due to feedback action node Q stores data '1'. Write '1' operation of the proposed cell is illustrated in Figure 4b.

During hold mode, WL, WLA, and WLB remain at ground while VVSS is kept at VDD. Two cross-coupled inverters hold the stored data as long as power is ON.

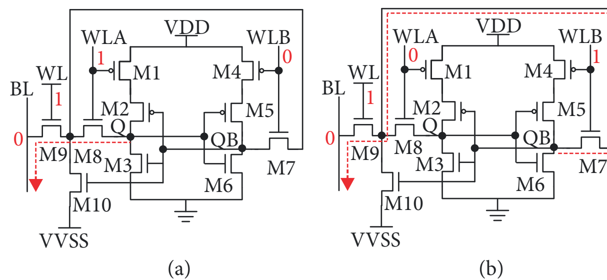

Figure 4. Proposed SEDF10 cell during (a) write '0' mode and (b) write '1' mode.

3. Simulation results and discussion

To show the effectiveness of the SEDF10T SRAM cell, important design metrics are extracted using 65-nm CMOS technology on Cadence. For comparison of the design metrics, the authors also designed and simulated the conv 6T (Figure 1a), ST-2 cell (Figure 1c) [6], TPDF9T cell (Figure 1d) [7], and power-gated 9T cell (hereafter referred to as the PG9T cell) (Figure 1e) [8] with 65-nm CMOS technology. For the conv 6T cell, width of pull-down, access, and pull-up transistors is equal to 300 nm, 200 nm, and 150 nm, respectively. Width of pull-down, access, and pull-up transistors in the proposed SEDF10T, ST-2, TPDF9T, and PG9T cells is equal to 300 nm, 200 nm, and 150 nm, respectively. The transistor width in the read buffer of all four cells is 200 nm. Power-gated transistors in the PG9T cell (M5 and M6) have a width of 150 nm. Length of all transistors of all these cells is 65 nm.

3.1. Read stability

The metric RSNM is used to quantify the read stability of a SRAM cell. It is estimated as the side length of the largest square embedded inside the read butterfly curve formed by plotting the voltage transfer characteristic (VTC) and inverse VTC of two inverters of a SRAM cell. Larger RSNM values indicate better read stability [10, 11]. Figure 5 shows the read butterfly curves for different cells under consideration. During read operations, the conv 6T and ST-2 cells show degraded RSNM due to rise in voltage at the ‘0’ storing node. On the other hand, the SEDF10T cell shows full swing in read VTCs as read current does not flow through internal storage nodes. Since TPDF9T and PG9T cells also employ separate read buffers, the read VTCs of these cells are similar to that of the SEDF10T cell as shown in Figure 5.

Figure 6 gives a comparison of RSNMs of different SRAM cells under consideration. The proposed SEDF10T cell shows 2.77 times and 1.47 times higher RSNM as compared to the conv 6T and ST-2 cells, respectively, at 400 mV. Because of their similar behavior during read operations, TPDF9T, PG9T, and the proposed cell show equal RSNM; therefore, the plots of RSNM for these cells overlap. Figure 7 shows the RSNM for different cells at TT, FNSP, and SNFP corners. At the FNSP corner, SEDF10T shows the lowest RSNM as inverters in the latch of the SEDF10T cell are less skewed at this corner than TT and SNFP corners. At the SNFP corner, the SEDF10T cell shows the highest RSNM, because at this corner, a PMOS transistor is stronger than an NMOS transistor, which results in increased switching threshold of the inverters. However, at all these corners, the proposed cell achieves larger RSNM as compared to the conv 6T and ST-2 cells and RSNM equal to those of the TPDF9T and PG9T cells.

3.2. Write ability

The write ability of a bit cell is quantified in terms of WSNM. It is the ability of a cell to pull down the voltage at ‘1’ storing node to a level below the write trip point voltage of the inverter storing logic ‘0’. For successful writes, a cell is required to be in a monostable state. This means that two VTCs should intersect at only one point. Figure 8 shows the VTCs of the SEDF10T cell during a write operation. It can be seen in the graph that the two VTCs intersect at only one point, indicating a successful write [12, 13].

In order to explore the effect of power-gating transistor M1 (or M4) on write ability, we consider the circuit of Figure 9, which shows the relevant part of the SEDF10T cell during write ‘0’.

Let us assume that initially logic ‘1’ is stored in the cell. To write a ‘0’, BL is pulled down to ground while WL and WLA are forced to VDD. Applying KCL at node Q, the discharge current I_{CQ} is

$$I_{CQ} = I_{AX} - I_{PU} \tag{1}$$

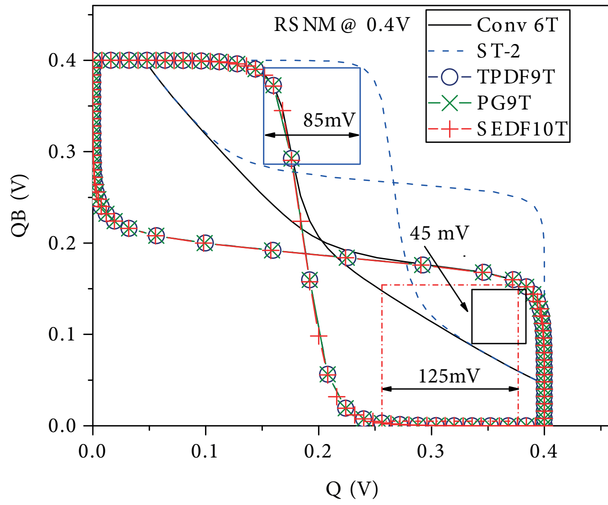

Figure 5. Read butterfly curves.

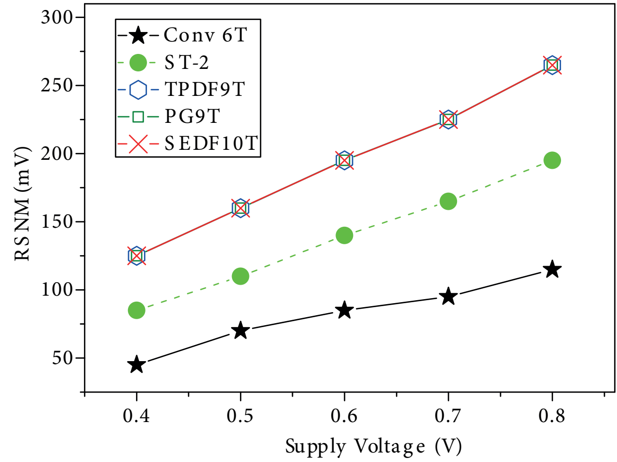

Figure 6. RSNM versus supply voltage.

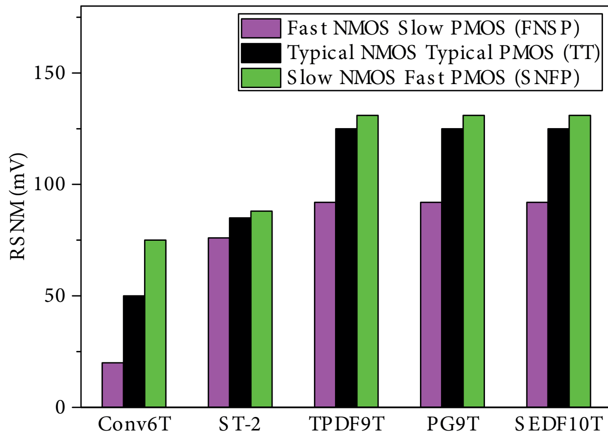

Figure 7. RSNM at different process corners.

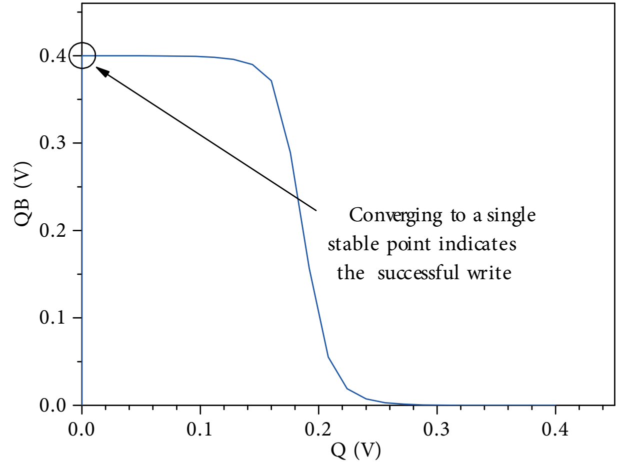

Figure 8. VTC during write operation.

as $I_{CQ} = -C_Q \frac{dV_Q}{dt}$; therefore,

$$-C_Q \frac{dV_Q}{dt} = I_{AX} - I_{PU}, \tag{2}$$

where I_{PU} is the current through M1 and M2 that charges node Q, I_{AX} is the current through M8 and M9 to discharge node Q, C_Q is the parasitic capacitance, and V_Q is the voltage at node Q. In the proposed cell, M1 is OFF due to high WLA during write '0', which makes I_{PU} almost equal to zero. Therefore,

$$-C_Q \frac{dV_Q}{dt} = I_{AX} - 0. \tag{3}$$

Thus, total available current for discharging node Q is I_{AX}, which is larger than the current $(I_{AX} - I_{PU})$. Therefore, node Q will discharge faster compared to that of the TPDF9T cell, for which the discharge current is $(I_{AX} - I_{PU})$. Similarly, M4 is OFF during write '1', resulting in faster discharge of node QB to write a '1' at node Q. This means that the SEDF10T cell offers improved WSNM as compared to the TPDF9T

cell. Figure 10 shows the WSNM for write ‘1’ for the proposed SEDF10T and other cells at 0.4 V. It can be observed that the SEDF10T cell achieves 5.14 times and 1.56 times larger WSNM for write ‘1’ as compared to single-ended TPDF9T and PG9T cells, respectively, at 400 mV without an additional write assist circuit. Note that the TPDF9T and PG9T cells need additional write assist circuits to improve the WSNM. To evaluate the performance of the proposed cell under process variation, 1000 Monte Carlo (MC) simulations are done for write ‘0’ and write ‘1’ operations at a supply voltage of 400 mV as shown in Figure 11. It can be observed that the proposed cell successfully performs write operations under process variation. The mean time for write ‘0’ (for QB to reach 0.9 VDD) is 19.63 ns with standard deviation equal to 4.627 ns, whereas, the mean time for write ‘1’ (for Q to reach 0.9 VDD) is 20.52 ns with standard deviation equal to 4.613 ns.

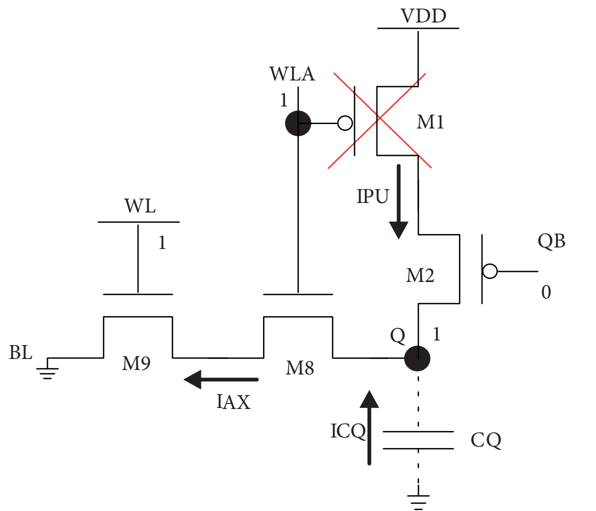

Figure 9. Relevant part of SEDF10T cell during write ‘0’ operation.

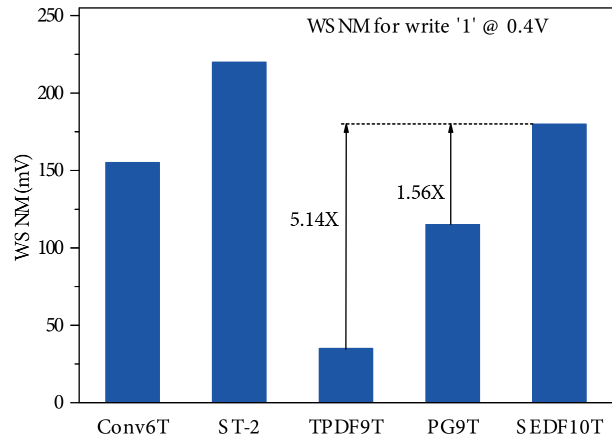

Figure 10. WSNM for write ‘1’.

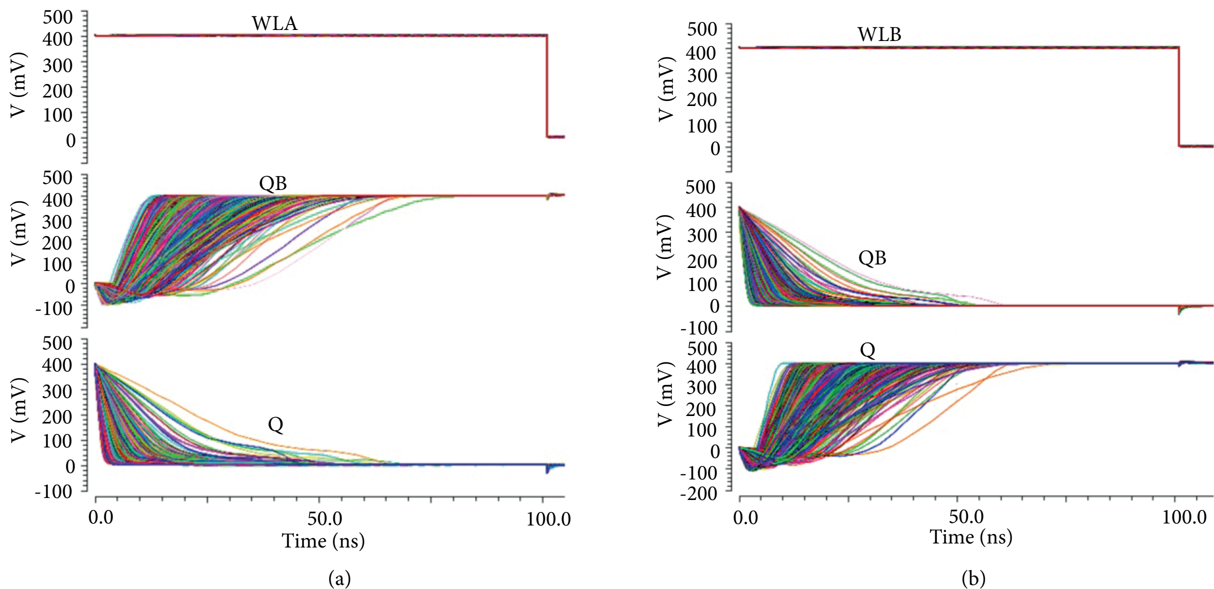

Figure 11. 1000 MC simulations for (a) write ‘0’ and (b) write ‘1’ operations.

3.3. Read/write delay

For differential read SRAM cells, read delay is the time elapsed in discharging one of the bit lines by 50 mV after activation of the read word line [14]. For a single-ended cell, read delay is the time taken by BL after activation of the read word line to discharge by 50 mV from its initial precharged level VDD [15]. Figure 12 illustrates the read delay for the different cells under consideration. It is observed that read delay of the proposed cell is 0.72 times that of the ST-2 cell at 0.4 V. Longer delay of the ST-2 cell is due to its larger bit line capacitance. Since the numbers of transistors in the read buffers of TPDF9T, PG9T, and SEDF10T cells are equal and of the same strength, the read delay of the proposed cell is approximately equal to those of TPDF9T and PG9T cells, as shown in Figure 12.

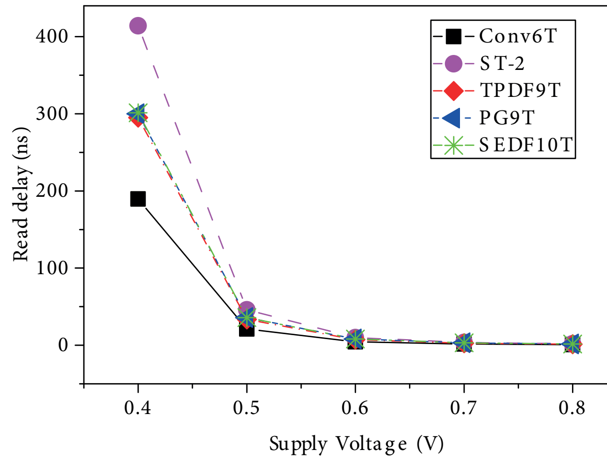

Figure 12. Read delay versus supply voltage.

For single-ended write operation, write ‘0’ access time or write ‘0’ delay is estimated as the time interval from activation of word line WLA to the instant when the ‘1’ storage node falls to 10% of its initial high value. Similarly, write ‘1’ access time or write ‘1’ delay is defined as the time from when word line WLB is activated to the time when the ‘0’ storage node rises to 90% of its initial low value [15]. During write operations, the source terminal of M2 (or M4) of the SEDF10T cell does not remain at VDD. Therefore, node Q (or QB) is weakly connected to VDD. Consequently, node Q (or QB) discharges faster through the write access transistor. Table 2 gives the write delay comparison of the proposed and other cells under consideration. From Table 2, it is observed that the write delay of the proposed cell is 77.56% less than that of the TPDF9T cell without write assist circuit. It is also observed that the PG9T cell shows the longest write ‘1’ delay among all the cells under consideration. This is because of two series NMOS transistors in the write path of the PG9T cell.

If a write assist technique such as word line-boosting is applied to the SEDF10T cell, it would perform even faster write operations compared to the TPDF9T cell (with boosted word line). Table 3 shows the results for write ‘1’ delay (for VDD = 0.4 V) with word line WLB boosted to 0.45 V. It is observed that our cell

Table 2. Write delay comparison at VDD = 0.4 V.

Delay	Conv 6T	ST-2	TPDF9T*	PG9T*	SEDF10T
Write ‘0’ (ns)	7.5	2.83	94.14	14.0	20.98
Write ‘1’ (ns)	7.5	2.83	93.04	574.6	20.08

*Without write assist circuit.

achieves 1.43 times shorter write ‘1’ delay as compared to the TPDF9T cell. Thus, the write performance of the SEDF10T cell can be improved by employing write assist methods, if required. Shorter write delay of the SEDF10T cell is due to the use of power-gated transistor M1 (or M4), which isolates storage nodes Q (or QB) from VDD during write operations. Besides, at VDD = 0.4 V, the TPDF9T cell without write assist fails to write at the SNFP corner, the worst case for writes [4], whereas the SEDF10T cell performs successful write operations with write ‘1’ delay of 22.25 ns.

Table 3. Write performance comparison with word line-boosting technique.

Cell	VDD (V)	WWLE/WL (V)	WLA (V)	WLB (V)	Write ‘1’ delay (ns)
TPDF9T	0.4	0.45	0	0.45	23.22
SEDF10T	0.4	0.45	0	0.45	16.19

3.4. Read/write power

Due to single-ended reads in the SEDF10T cell, switching activity on BL is less than that of the differential read ST-2 cell. BL of the SEDF10T cell is discharged if a 10’ is stored, or else it remains at its precharged level VDD. Thus, no switching activities occur during read ‘1’ operations. On the other hand, for differential read ST-2 cell, one of the bit lines is always discharged regardless of the stored data. Therefore, for equal probabilities of ‘0’ and ‘1’, the switching power consumption in the proposed cell is less compared to that of the ST-2 cell [15]. During write operations, BL of the SEDF10T cell remains at ground level regardless of writing data ‘0’ or data ‘1’. Therefore, no switching activity on BL occurs if two consecutive write operations are performed. On the other hand, for ST-2 and PG9T cells, BL is lowered to ground for writing data ‘0’ and raised to VDD for writing data ‘1’. Thus, BL power dissipation of the SEDF10T cell is less than that of ST-2 and PG9T cells. Also, due to single-ended writes, the number of write-drivers in the SEDF10T cell is half that of the differential ST-2 cell [15]. Hence, write power consumption of the SEDF10T cell is less than that of the differential write ST-2 cell.

3.5. Leakage Power

A major part of a SRAM remains in the idle state for a long time. Leakage current flows through the idle cells, which results in static power dissipation. The static power dissipation is mainly due to subthreshold current, junction leakage current, and gate leakage current. However, the subthreshold current dominates the junction and the gate leakage current. Therefore, leakage power dissipation can be minimized by reducing the subthreshold current. In the proposed cell, leakage current of M1 and M4 is negligible as their drain to source voltage is approximately zero. Therefore, the leakage current in the latch of SEDF10T and that of the conv 6T cell is almost equal. Due to high VVSS during hold, the bit line leakage of TPDF9T, PG9T, and the proposed cell is less than that of the conv 6T cell. In the proposed cell, stacking of M9, M8, and M3 (or M9, M7, and M6) also reduces leakage current [16]. Figure 13 shows leakage power versus supply voltage for the proposed and other cells. It can be observed that leakage power of the proposed cell is 0.89 times that of the ST-2 cell at 0.8 V. The ST-2 cell consumes the highest leakage power as it does not employ any mechanism to reduce bit line leakage. The bit line leakage path in the ST-2 cell holding a ‘0’ is BL-M8-M3-GND. Leakage currents also flow through the latch.

3.6. Bit interleaving for soft error immunity

In the bit-interleaved architecture, bits of different words are physically interleaved to mitigate soft errors. In the conv 6T cell, when word line WL is activated to write data in the selected cell, the access transistors of other cells of the same row also become ON, which connect the storage nodes to the bit lines. Such 'row-selected' but 'column-not-selected' cells, referred to as half-selected cells, undergo a pseudo read operation, which can cause a bit flip to take place. This problem is referred to as half-select disturbance [17]. Since the proposed cell is based on a cross-point write structure, in which row-based WL and column-based WLA (or WLB) must be enabled to select a cell, half-selected cells of a bit-interleaved architecture do not undergo pseudo read operation during a write operation. Figure 14 shows the 2 × 2 bit-interleaved architecture of the proposed SRAM cell. As shown in Figure 14, row_0 and column_0 both must be enabled (WL_0 = '1', WLA_0 = '1', WLB_0= '0', and BL_0 = '0') to write a '0' in the selected cell. During write '0' operation, a row-half-selected cell does not undergo any read disturbance because WLA_1 (or WLB_1) is disabled. Similarly, a column-half-selected cell also does not undergo read disturbance as WL_1 is not enabled.

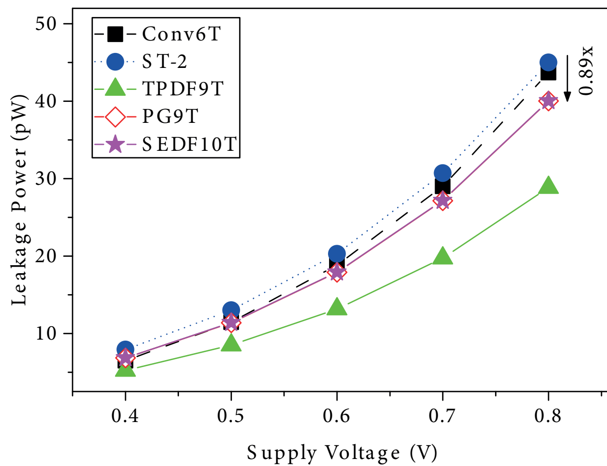

Figure 13. Leakage power versus supply voltage.

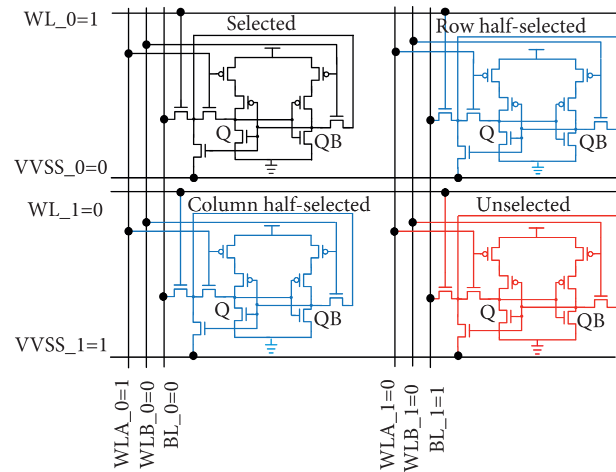

Figure 14. The 2 × 2 bit-interleaving architecture of SEDF10T cell during write '0'.

3.7. Bit cell area

Figures 15a–15c respectively show the layout of the conv 6T, TPDF9T, and SEDF10T cells using lambda-based design rules on a 65-nm technology node. As shown in the figure, the vertical dimension of the SEDF10T cell is maintained at two poly pitches and is equal to that of the conv 6T cell. The shorter vertical dimension of the SEDF10T cell maintains bit line capacitance at a minimum value. The proposed cell has five columns of the active region as compared to the conv 6T cell, which has four columns of the active region. Therefore, the horizontal dimension of our cell is 1.34 times longer than that of the conv 6T cell. Thus, the area of the SEDF10T cell is 1.34 times larger than that of the conv 6T cell. However, the TPDF9T cell occupies 1.30 times more area than the conv 6T cell. Therefore, the SEDF10T cell area is 1.030 times larger than that of the TPDF9T cell.

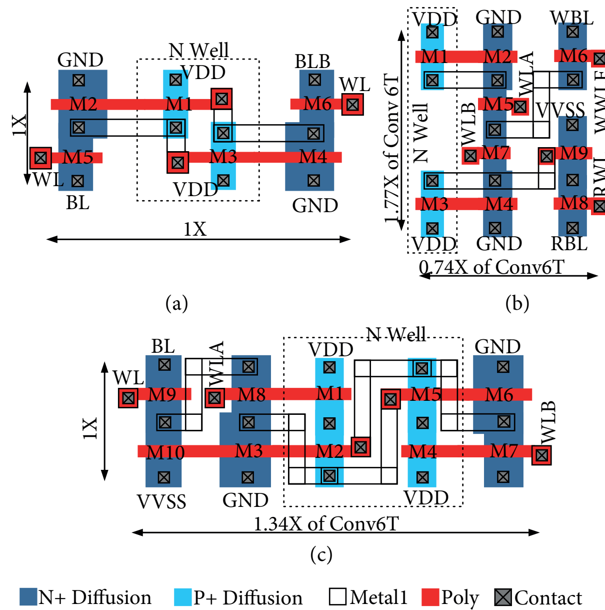

Figure 15. Layout of (a) conv 6T, (b) TPDF9T cell [7], and (c) SEDF10T cells.

3.8. Array-level area comparison

In this section the area of the SEDF10T 4kb array is compared with the area of the TPDF9T array. TPDF9T employs negative bit line (NBL) and write-word line boost techniques simultaneously. Therefore, areas of both the circuits are estimated at a 4kb array. Area of the NBL write assist-circuit was estimated in [4]. According to [4], the NBL write-assist circuit occupies an area of about 4% of the 72kb SRAM macro area. From this information, we estimated the area of the NBL write assist-circuit, which is about 4% of 4kb TPDF9T array. Area of the word line write-assist circuit is estimated to about 0.2% of the 4kb array [7]. Therefore, the total area of the write-assist circuit (NBL and word line boost) is about 4.2% of the 4kb TPDF9T array. Therefore, the area (normalized to 6T) of the TPDF9T 4kb array (with write-assist) is about 1.35 (= 1.30 + 4.2% of 1.30). Table 4 shows a normalized area comparison of the TPDF9T and SEDF10T arrays. From the table, it can be observed that at a 4kb array, SEDF10T occupies an area of about 1.34 whereas the TPDF9T area is about 1.35. Thus, the SEDF10T 4kb array consumes less area of 0.99 times that consumed by the TPDF9T 4kb array. Although the write-assist circuit enables successful write operation, it leads to an increase in switching power due to increased switching activities of additional control signals. Moreover, use of a boosting capacitor in the write-assist circuit increases the leakage current.

Table 4. Normalized area comparison at 4kb array.

Array	Conv 6T array	TPDF9T array w/o write-assist	TPDF9T array with write-assist	SEDF10T array w/o write-assist
4kb	1×	1.30×	1.35×	1.34×

Table 5. Bit cell comparison with the proposed design.

Parameter	Conv 6T cell	ST-2 cell [6]	TPDF9T cell [7]	PG9T cell [8]	Proposed cell
Reading/writing	Diff/Diff	Diff/Diff	SE/SE	SE/SE	SE/SE
Bit lines	2-BL	2-BL	1-WBL, 1-RBL	1-BL	1-BL
Control signals	1(WL)	2(WL, WWL)	5(WWLE, WLA, WLB, RWL, VGND)	5(WL, WWL, WLPU, WLPD, VVSS)	4(WL, WLA, WLB, VVSS)
Bit interleaving	No	Yes	Yes	Yes	Yes
RSNM (mV) @ 0.4 V	45	85	125	125	125
Write power (nW) @ 0.4 V	30.14	68	26.28	7.59	10.28
Read power (nW) @ 0.4 V	23.0	31.0	14.3	15.1	15.1
Hold power (pW) @ 0.4 V	7.4	8.0	6.6	6.63	6.7
Area	1×	2.1×	1.30×	1.32×	1.34×

4. Conclusion

In this paper, a single-ended read disturb-free 10T SRAM cell has been explored. The read decoupled buffer of the SEDF10T cell enables read disturb-free operation. The WSNM for write ‘1’ of the proposed cell is larger by 5.14 timesand 1.56 times compared to those of TPDF9T and PG9T cells, respectively. Due to differential write, the ST-2 cell shows improved WSNM, but this cell has lower RSNM than the SEDF10T cell. Table 5 gives the comparison of the proposed and other cells. The RSNM of the SEDF10T cell is 2.78 times and 1.47 times higher than those of conv 6T and ST-2 cells, respectively, at 0.4 V. Write power consumption of the proposed cell is 0.15 times that of the ST-2 cell at 0.4 V. The discussed cell is immune to soft errors as it has the capability of bit interleaving. The proposed design occupies an approximately 1.34 times larger area as compared to the conv 6T cell with 65-nm standard CMOS technology. Even though the SEDF10T cell consumes a larger area than the conv 6T cell, enhanced stability enables the SEDF10T cell to operate at reduced VDD.

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