Turkish Journal of Electrical Engineering & Computer Sciences

http://journals.tubitak.gov.tr/elektrik/

Research Article

Turk J Elec Eng & Comp Sci
(2018) 26: 2385 – 2394

doi:10.3906/elk-1707-352

Improved transient response capacitor less low dropout regulator employing adaptive bias and bulk modulation

Suresh ALAPATI*, Sreehari Rao PATRI
Department of Electronics and Communication Engineering, National Institute of Technology Warangal, Telangana State, India

Received: 27.07.2017 • **Accepted/Published Online:** 18.06.2018 • **Final Version:** 28.09.2018

Abstract: This paper presents a low quiescent current, fast settling time, and adaptively biased capacitor less low-dropout (LDO) regulator. The topology involves a segmented pass transistor with bulk modulation and adaptively biased current control stages to improve the transient performance. The bulk modulation of the pass transistor assists in fast settling of the output voltage. The frequency compensation makes the LDO voltage regulator stable adaptively over load current transitions. In addition, the biasing stage is designed such that it adapts to the load transitions while consuming the quiescent current abstemiously. This arrangement further improves settling time to be within 1 µs while restricting undershoot/overshoot to 171 mV/82 mV for a load current transition between 0 and 100 mA with load capacitor of 40 pF. The LDO regulator is designed using 0.18 μm UMC CMOS process by consuming 1.5 μA quiescent current at no loads.

Key words: Dropout voltage, adaptive biasing, bulk modulation, telescopic amplifier, voltage regulator

1. Introduction

The system on-chip (SoC) for portable appliances requires a power management unit that supplies power to its corresponding subsystems. For instance, basic operations of digital systems require different supply voltages as compared to that of clocking [1]. In addition, their analogue counterparts demand different supply voltages. These required voltages can be supplied by switching or low-dropout (LDO) regulators. LDO regulators with small footprint and less noise prevail over their switching counterpart. The typical response time of a LDO regulator for digital loads is expected to be in the range of 1 μs with tight boundary requirements on dynamic and static load/line tolerances and optimum power consumption [2, 3].

There exists a trade-off among multiple critical design parameters of LDO. The realization of LDO striking a reasonably good balance amongst these parameters simultaneously is a daunting task. They include optimum frequency compensation meeting stability requirements over the entire range of load currents, less footprint area, high-current efficiency, low output voltage undershoot/overshoot, and an accurate output voltage. To support multiple digital loads operated simultaneously and obtain a good throughput, a fast-transient response is mandatory [4]. A stage with a capacitor multiplier is used to improve the dynamic performance of LDO [5] but at the cost of increased power consumption. A flipped voltage follower based LDO [6] is used to reduce power consumption but suffers from low load and line regulation due to inferior dc gain. A fast-transient response is achieved in [7], but the LDO consumed a large quiescent current of 6 mA for the design, making it unsuitable

*Correspondence: suresh.sieger@gmail.com

for battery operated applications. The LDO in [8] achieved a better transient response and used an adaptive frequency compensation technique for compensation but achievement of accurate pole-zero cancellation is not possible. A class AB push pull error amplifier employed for LDO in [9] enhances slew rate at the gate of pass transistor and achieves a relatively good transient response. However, the stability at lower load currents below 50 μA is not ensured. Regulators proposed in [10, 11] use an adaptive two and three stages based upon load current demands to regulate the output but it consumes higher quiescent currents and drains the battery, affecting current efficiency.

The various trade-off parameters such as the relationship between the fixed bias current of error amplifier and lowest load current, the influence of adaptive bias ratio on transient response, and limitation of improvement in transient response with use of excess bias current at higher load conditions are discussed in [12]. The role of bulk modulation in improving the transient response is properly stated in [13]. However, an amplifier is used to drive the bulk terminal of the pass transistor and carries a large quiescent current and affects current efficiency.

The sluggishness and large variations of output voltage transient response due to the large single pass transistor used in conventional capacitorless LDO regulators is discussed in [14, 15] and a pass transistor segmentation based capacitorless LDO proposed offered a better transient response and stability at lower load currents. However, the settling time and transient response are poor. A slew rate enhanced capacitorless LDO based on output transient detection is proposed in [16]. However, the large bias current used for the topology affects the current efficiency. Another capacitorless LDO that employs a capacitive coupling from output to a biasing circuit is proposed in [17]. However, an extra amplifier inserted in the feedback path occupies excess area and degrades stability. An auxiliary undershoot reduction circuit operated in the subthreshold is used for the capacitorless LDO reported in [18]. However, the circuit is complex and the settling time of the undershoot voltage is large.

In the present paper, the segmentation of pass transistors and their selection for regulation according to the load improves stability and transient response. The adaptive biasing of error amplifier improves the load regulation and current efficiency. The pass transistor's bulk modulation in addition to its gate drive settles the overshoots sooner. The proposed LDO circuit implementation is introduced in Section 2, followed by a detailed discussion of each stage in their subsections. The results are reported in section 3. Conclusions regarding the proposed regulator are stated in section 4.

2. Proposed circuit implementation of LDO

The proposed LDO topology shown in Figure 1 consists of a high gain error amplifier constituting transistors M_{d1}-M_{d6}, buffer transistors M_{b1}-M_{b2}, and two segmented pass transistors M_{P1} and M_{P2}, one supporting lower currents while the other higher load currents. The output voltage is sampled by resistors R_{F1} and R_{F2} to provide a level shifted voltage to the noninverting input of the error amplifier whose other input is constant voltage V_{ref}. A fixed bias current I_B of 1 μA is used at the tail of error amplifier that ensures the stability of LDO for a lower load current. A compensation capacitor C_g is connected between output and node V_b through a common gate transistor M_{d4}. The bulk modulation of the pass transistor is done through a R_1C_1 network. The design intricacies of the LDO are discussed in the following sections.

2.1. Error amplifier configuration

Power efficiency and high accuracy are the required attributes of an error amplifier of the proposed LDO. A pseudotelescopic amplifier with load transistors (M_{d5},M_{d6}) is used that isolates driving transistors (M_{d1},M_{d2})

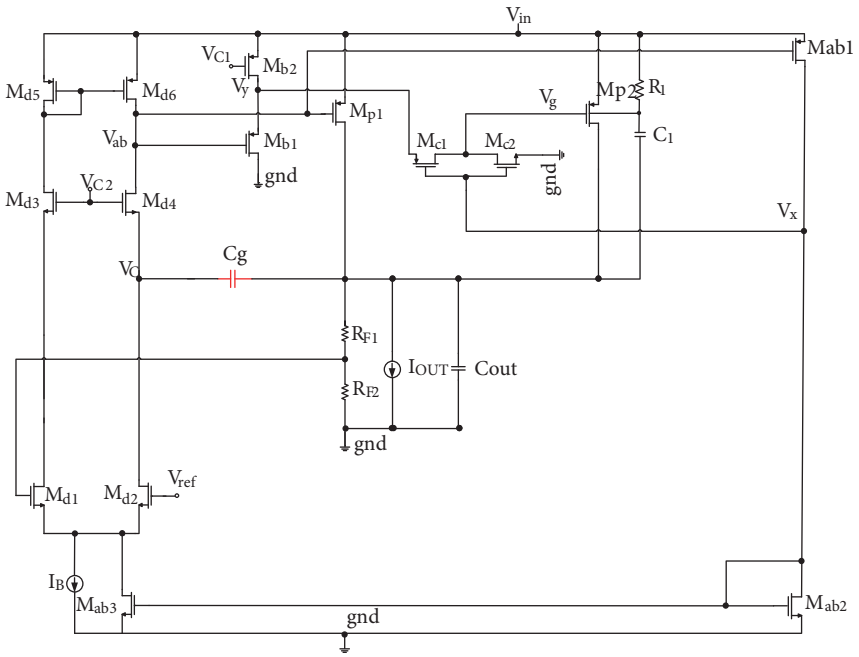

Figure 1. Circuit diagram implementation of the capacitor less LDO regulator.

from its output node V_{ab} through current buffer transistors (M_{d3},M_{d4}). The error amplifier receives inputs from a feedback network (consisting of resistors R_{F1} and R_{F2}) and a reference voltage. The transconductance of (M_{d1}, M_{d2}) is adjusted dynamically by tail current source as explained in section 2.4. The output resistance at node V_b is $R_{out} = (g_{md4} \times r_{d4} \times r_{d2}) \parallel (r_{d6})$ and the small signal voltage gain is $g_{md1} \times R_{out}$. The g_{md4} and g_{md1} are the transconductance of M_{d4}, M_{d1} transistors and r_{d4}, r_{d2},r_{d6} are the intrinsic resistances of M_{d4}, M_{d2}, and M_{d6} transistors, respectively.

2.2. Pass transistor segmentation and control section

In the conventional capacitor less LDO regulator a single large size pass transistor supports both heavy and lower load currents. The large size of the pass transistor leads to corresponding large gate capacitance affecting the slew rate and thereby resulting in sluggish transient response. Moreover, the proximity of the output pole and pass transistor pole degrades the stability especially at lower and light load conditions. The mobile appliances remain in standby operations for a longer period of time before they wake up for the operation, and so a single large size pass transistor used for handling both operations slows the response of the error amplifier and also consumes more power for regulation. Thus, a single error amplifier driving segmented pass transistors one catering to lower load currents while the other for higher load currents is used. The control section comprising transistors (M_{c1},M_{c2}) is used to switch between the pass transistors adapting to load demands. The segmentation improves the transient response and balances stability over the entire load current range while occupying a relatively small footprint area and consuming less power.

2.3. Adaptive bias structure

The bias requirements of the LDO are different for different loads. Higher gain and faster operation are required at higher load currents as compared to lower loads to improve current efficiency. Accordingly, the bias of the

error amplifier is made adaptive. A fixed current source is employed to meet the bias requirements at lighter loads. As the load varies, the corresponding variations are sensed by the current sensing feedback loop formed by M_{ab1}-M_{ab2}-M_{ab3} and scaled down suitably. This arrangement ensures minimum phase margin at lower load currents [12] while optimizing bias currents at higher loads.

2.4. Frequency compensation

The proposed LDO architecture strikes better trade-offs among gain, bandwidth, and magnitude of the transient load ripple. In the conventional on-chip LDO, the pass transistor gate capacitance constitutes the dominant pole, while the pole corresponding to the output node is nondominant. This composition makes the regulator unstable at lower loads, while it is unconditionally stable at higher loads. However, due to the pass transistor segmentation, only the smaller pass transistor is active at lighter loads. This arrangement makes the pole due to the pass transistor gate nondominant, forcing the pole at the output node to become dominant. As the load current increases, the poles start moving closer, affecting the stability. This requires one to compensate the LDO against load variations.

The capacitance C_g along with the current buffer transistor M_{d4} as shown in Figure 2 generates a zero that compensates the movement of the load pole, making the system stable. This compensation is attributed to the adaptive biasing applied to the error amplifier that varies the transconductance of transistor M_{d4} as per load variations. Further, this arrangement avoids the feed forward signal path and thus gets rid of the right-hand plane zero. However, the slow response of the adaptive biasing loop may not support the stability over entire load currents, in particular, during transients from low to high load transitions, which may lead to oscillations. These oscillations can be reduced by using the bulk modulation mechanism explained in the following section.

2.5. Bulk modulation structure

The architecture proposed attempts to augment stability by exploiting bulk modulation of pass transistor M_{p2} varying the corresponding threshold voltage as per the load variations. The transconductance variation bulk

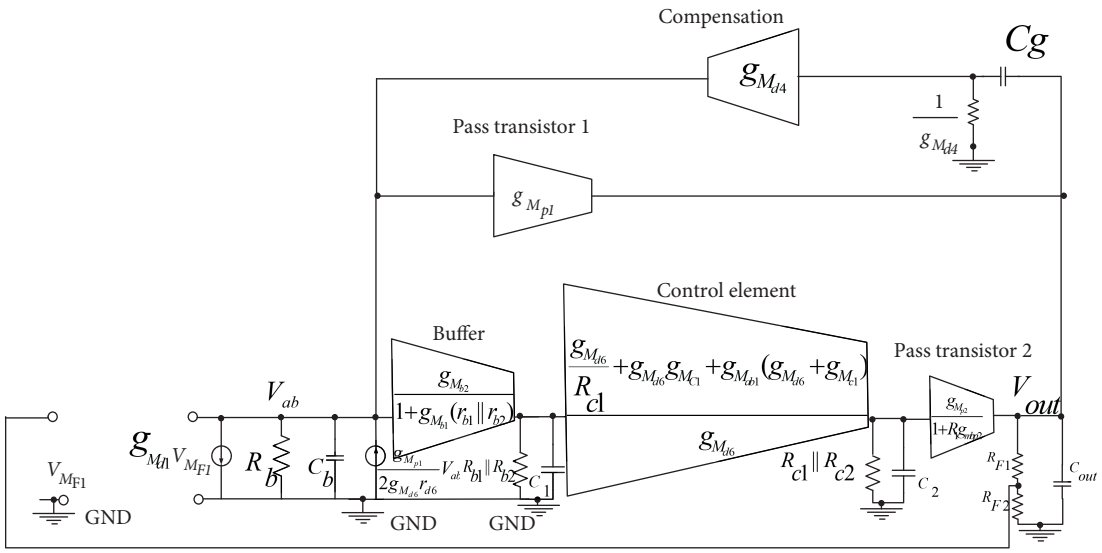

Figure 2. Small signal equivalent diagram of the proposed regulator.

transconductance is a function of source to bulk voltage V_{sb} [13]. An undershoot that results due to the load variation from low to high is coupled by C_1 to the bulk terminal of M_{p2} as shown in Figure 2. The corresponding threshold voltage variation leads to the required increment in drain current, thereby reducing undershoots and also settling faster. The bulk potential is restored to its nominal value (1.8 V) at the end of load transition. Therefore, the bulk modulation precipitates the movement of the dominant pole towards compensating zero, thereby improving stability. A similar improvement can be found in the transient response during the converse load transition. This topology employs bulk modulation of the pass transistor with only two passive elements R_1 and C_1 without consuming extra quiescent current, thereby conserving the power and reaping more benefits as compared to [13]. The corresponding transfer function for the proposed architecture is as follows:

$$\frac{V_{out}}{V_{M_{F1}}} = \frac{X_1 \times X_3}{1 + X_1 \times X_3 \times \beta + X_5 \times X_3}, \tag{1}$$

where

$$X_1 = \frac{V_{ab}}{V_{M_{F1}}} = \frac{g_{M_{d1}}}{\frac{R_b}{1+sC_bR_b} - \frac{g_{M_{p1}}}{2g_{M_{d6}}r_{d6}}}. \tag{2}$$

$$X_3 = \frac{V_{ab}}{V_{out}} = \frac{g_{M_{d4}}sC_B}{g_{M_{d4}} + sC_B}. \tag{3}$$

$$\begin{aligned} X_5 = \frac{V_{out}}{V_{ab}} = g_{M_{p1}} + \frac{g_{M_{c2}}(r_{c1} \parallel r_{c2})}{1 + g_{M_{c2}}(r_{c1} \parallel r_{c2})} \times \frac{1}{1 + sC(r_{c1} \parallel r_{c2})} \times \frac{1}{r_{c1}} + g_{M_{c1}} \\ + \frac{g_{M_{ab1}}}{g_{M_{ab2}}} + (g_{M_{c1}} + g_{M_{ab2}}) \times \frac{r_{c1} \parallel r_{c2}}{1 + sC(r_{c1} \parallel r_{c2})} \times \frac{g_{M_{p2}}}{1 + R_1}. \end{aligned} \tag{4}$$

$$\beta = \frac{R_{F2}}{R_{F1} + R_{F2}}. \tag{5}$$

3. Results

The proposed LDO provides a nominal regulated output voltage of 1.6 V for a dropout of 200 mV at 100 mA load current and is implemented in UMC 0.18 μm CMOS technology using the cadence design systems spectre tool. The proposed architecture consumes a quiescent current that varies from 1.5 μA at no load to 20 μA at full load. The frequency response is depicted in Figure 3. It demonstrates the loop system stability of the LDO for C_1=1 pF and C_{out}=40 pF. The phase margin is 54.56^o at no load current and 84.96^o at full load current.

The transient response of the proposed LDO is shown in Figure 4, which also includes the corresponding plot for the conventional on-chip LDO. The impact of pass transistor segmentation and bulk modulation are shown explicitly.

An undershoot of 722.29 mV with settling time of 1.59 μs and an overshoot of 200 mV with settling time of more than 10 μs is observed for the conventional LDO. Adaptive biasing with pass transistor segmentation reduces undershoot to 340.84 mV and settling time to 1 μs. The reduction in overshoot of 88.58 mV can be observed with corresponding settling time of 4.15 μs. The inclusion of bulk modulation to the LDO reduces undershoot to 171.24 mV with settling time of 443.59 ns while restricting the overshoot to 82.92 mV.

The load regulation of the proposed regulator is shown in Figure 5. It is observed that the proposed regulator exhibits a load regulation of 0.104 mV/mA.

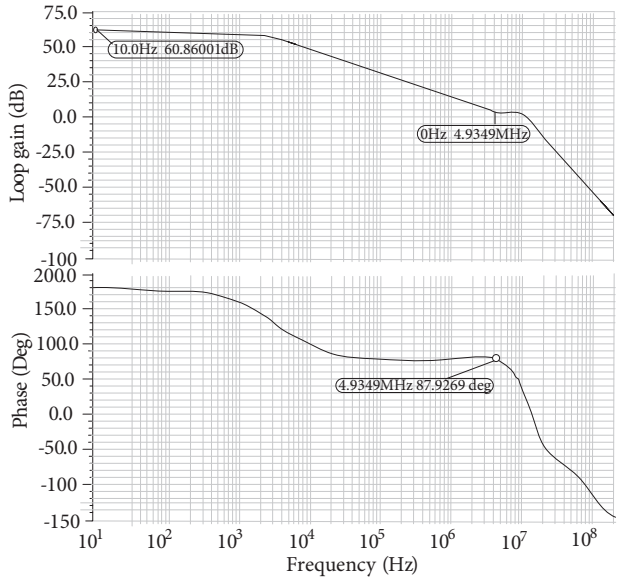

Figure 3. Frequency response of LDO at a load current of 100 mA.

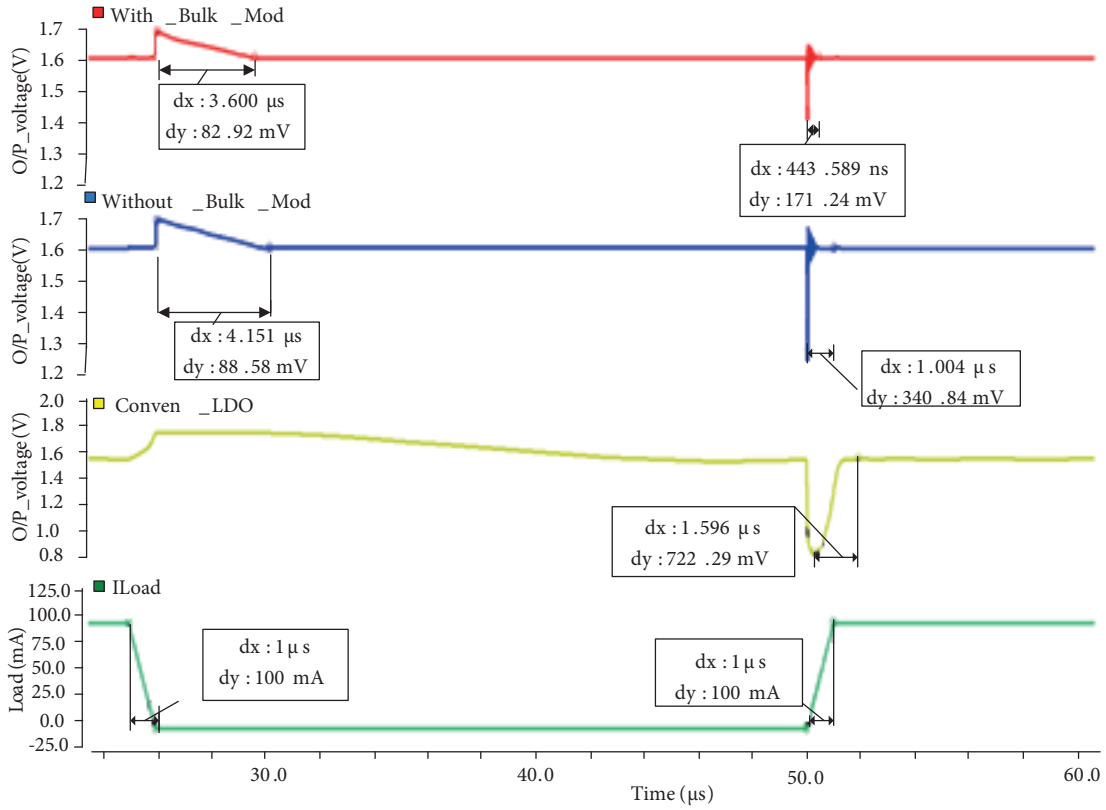

Figure 4. Transient responses of LDOs.

The ability of the LDO to reject the power supply ripple rejection (PSRR) is demonstrated in Figure 7 by superimposing a 200 mV ripple at 1 MHz on the supply. It can be seen that the LDO offers a power supply rejection of −43.37 dB at 10 Hz and −32 dB at 1 MHz at a load current of 100 mA.

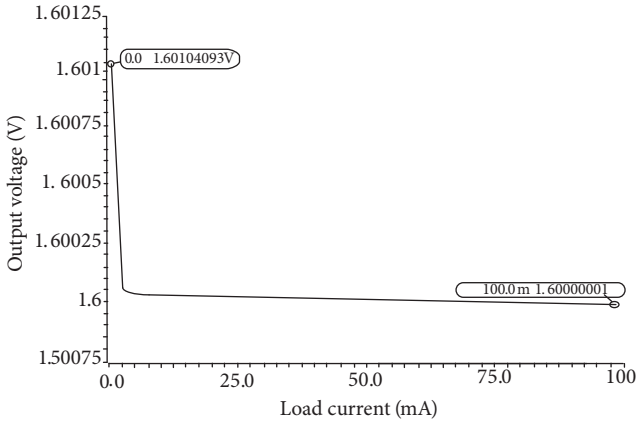

Figure 5. Load regulation of the proposed regulator for a input 1.8 V supply voltage.

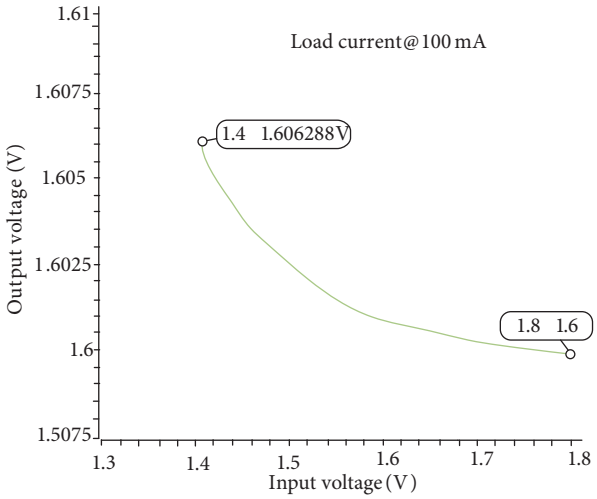

Figure 6. Line regulation of the proposed regulator at the load current of 100 mA.

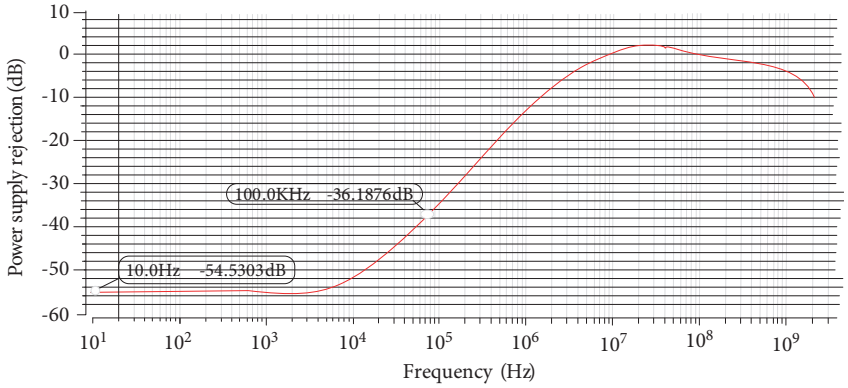

Figure 7. Power supply rejection ratio of the proposed regulator at 100 mA load current.

The proposed architecture exhibits a current efficiency η of 99.89%, which is evaluated from the following equation (6):

$$\eta = \frac{V_{out} \times I_{out}}{V_{in} \times (I_{out} + I_q)} \times 100 \tag{6}$$

The quiescent current (IQ) variation of the proposed regulator against load current is shown in Figure 8. The pass transistor M_{p1} supports lower load currents up to 2.5 mA while the higher range currents are supported by both M_{p1} and M_{p2}.

The layout of the proposed regulator is given in Figure 9. The worst case transient response at different process corners is reported in Table 1. It is observed from the tabulated values that the variation in undershoot/overshoot along with settling times is meager for the case of corner (tt and ff). However, there is a slight degradation in performance due to the worst case of slow (lightly doped PMOS and NMOS) corner due to the drop in the gain of the pass transistor occurring due to lower conductivity of the lightly doped PMOS pass transistor.

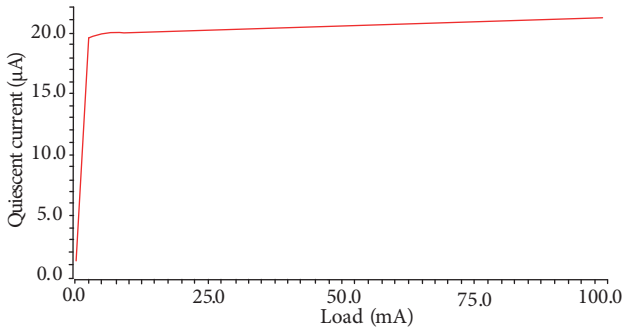

Figure 8. Quiescent current consumption as a function of load current.

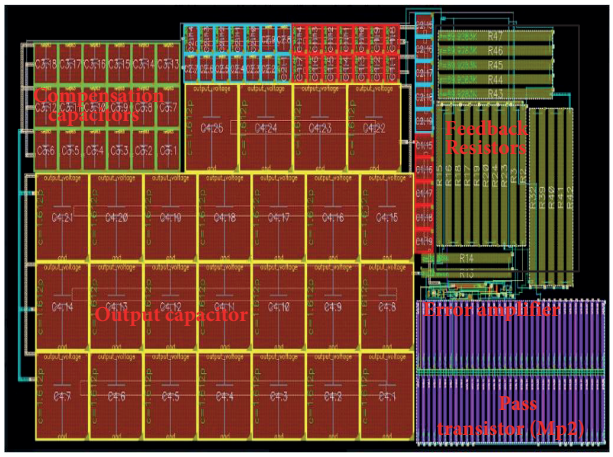

Figure 9. Layout of the proposed LDO.

Table 1. Transient response at various process corners.

Process corners	Undershoot/settling time	Overshoot/settling time
Typical-Typical	171.24 mV/427.375 ns	84.196 mV/4.85 µs
Slow-Slow	247.734 mV/997.625 ns	119.917 mV/5.743 µs
Fast-Fast	119.215 mV/542.681 ns	69.65 mV/3.42 µs

The load regulation performance is provided in Table 2. It is envisaged from the results reported that variation in load regulation is almost negligible with temperature.

Table 2. Load regulation at different temperatures.

Temperature (0 ^{o}C)	V_{out}(V)@100 mA	V_{out}(V)@0 mA	Load Regulation (mV/mA)
-40	1.60003	1.60077	0.074
27	1.59993	1.60113	0.012
85	1.59987	1.60255	0.026

A comparison with the latest state of the art LDOs is shown in Table 3.

The architecture proposed in this paper uses a 40 pF output capacitor similar to that of [13, 14] but consumes a lower quiescent current of 1.5 μA at no load. It can be observed the proposed architecture improves the transient response by decreasing undershoot and overshoot voltages. Further, this design shows an improvement in load transient settling time comparable to the state of the art LDOs illustrated in Table 3. The lower load regulation of 0.104 mV/mA achieved from the proposed LDO is better than that of its counterparts. The response time is given by (T_R) in Eq. (7) and the overall performance of the architecture is given by the figure of merit (FOM) shown in Eq. (8).

$$T_R = \frac{C_{out}}{I_{max}}, \tag{7}$$

$$FOM = \frac{T_R I_Q}{I_{max}}, \tag{8}$$

Table 3. State of the art LDOs comparison.

Reference	[16]	[17]	[18]	[14]	This work
Year	2010	2010	2012	2016	2017
Technology	0.35 μm	0.09 μm	0.35 μm	0.18 μm	0.18 μm
Nominal voltage	1.2 V	1 V	1 V	1.6 V	1.6 V
Supply voltage	1.4 V	1.2 V	1.2 V	1.8 V	1.8 V
Dropout voltage	200 mV	200 mV	200 mV	200 mV	200 mV
Outputcap. (C_{out})	100 pF	50 pF	100 pF	40 pF	40 pF
Line reg.	-	3.78 mV/V	0.39 mV/V	-	0.0157 mV/V
Load reg.	0.4 mV/mA	0.1 mV/mA	0.078 mV/mA	4 mV/mA	0.104 mV/mA
Quiescent current(I_Q)	43 μA	8 μA	28-380 μA	4.8 μA	1.5 μA
Load current($I_{(max.)}$)	100 mA	100 mA	100 mA	100 mA	100 mA
ΔIO,max	99 mA	99 mA	100 mA	100 mA	100 mA
Undershoot (ΔV_{out}) / Settlingtime	70 mV/3 μs 1 μA $\rightarrow$100 mA	62 mV/2 μs 1 μA $\rightarrow$100 mA	105 mV/5 μs 0 $\rightarrow$100 mA	180 mV/4 μs 0 $\rightarrow$100 mA	171.2 mV/0.4 μs 0 $\rightarrow$100 mA
Overshoot/Settlingtime	70 mV/3 μs 100 mA $\rightarrow$ 0 mA	72 mV/2 μs 100 mA $\rightarrow$0 mA	50 mV/5 μs 100 mA $\rightarrow$0 mA	200 mV/1.5 μs 1 mA $\rightarrow$100 uA	82.92 mV/3.6 μs 100 mA $\rightarrow$0 mA
PSRR	- -	$\leq$ –44 dB @1 kHz	$\leq$ –13.15 dB @1 MHz	- -	$\leq$ –36.18 dB @100 kHz
Current eff@100mA	99.96%	99.98%	99.98%	99.99%	99.89%
FOM	30.40 ns	2.48 ns	29.40 ns	3.45 ns	0.98 ns

where C_{out} is output capacitor, ΔV_{out} is undershoot voltage, I_{max} is the maximum load current, and I_Q represents the quiescent current at lower load currents. The improvement in the performance of the LDO is evident from the lowest figure of merit of 0.98 ns. This paper has presented an ultralow power and fast LDO regulator with its reduced quiescent current and good transient response. The incorporation of schemes like adaptive biasing, bulk modulation, and high slew rate control element assists them. The adaptive biasing extends closed loop bandwidth, bulk modulation instantaneously meets the demands of transient response by its controls over the pass transistor drive while gate voltage reaches supply voltage, and a control stage improves the slew rate at the gate of the pass transistor. The frequency compensation sustains stability for a wide range of load currents. Although the reported LDO has higher quiescent compared to the LDO reported in [14] by a meager amount, the improved transient response, high current efficiency, and better settling time are benefits for digital applications that demand quick response in nanoseconds.

4. Conclusions

This paper presents a low power and fast LDO regulator with its reduced quiescent current and improved transient response. The adaptive biasing with pass transistor segmentation optimizes the quiescent current requirements in tune with the load variations. This adaptive frequency compensation sustains stability for a wide range of load currents. This topology restricts the undershoot/overshoot to 171 mV/82 mV for a load current transition between 0 and 100 mA with load capacitor of 40 pF and by virtue of bulk modulation further assists in reducing transient voltage ripple and settles the overall response within 443.58 ns. The topology LDO regulator is designed using 0.18 μm UMC CMOS process by consuming 1.5 μA quiescent current at no loads. The LDO with improved transient response, high current efficiency, and better settling time is comparable to state of the art LDOs and is suitable for fast changing digital loads.

References

[1] Kang YH, Kim JK, Hwang SW, High-voltage analog system for a mobile NAND flash. IEEE J Solid-St Circ 2008; 43: 507-517.

[2] López T, Alarcón E. Power MOSFET technology roadmap toward high power density voltage regulators for next-generation computer processors. IEEE T Power Electr 2012; 27: 2193-2203.

[3] Peng SY, Liu LH, Chang PK, Wang TY, Li HY. A power-efficient reconfigurable output-capacitor-less low dropout regulator for low-power analog sensing front-end. IEEE T Circuits-I 2017; 64: 1318-1327.

[4] Huang M, Lu Y, Martins RP. An output-capacitor-free analog-assisted digital low-dropout regulator with tri-loop control. ISSCC Dig Tech Pap I 2017; 342-343.

[5] Lim J, Lee J, Jung S. SI/PI Co-simulation including voltage regulating circuitry for high-performance multi-chip package. Int Symp Elec Compat 2014; 366-369.

[6] Milliken RJ, Silva-Martinez J, Sanchez-Sinencio E. Full on-chip CMOS low-dropout voltage regulator. IEEE T Circuits-I 2007; 54: 1879-1890.

[7] Man TY, Leung KN, Leung CY, Mok PKT, Chan M. Development of single-transistor-control LDO based on flipped voltage follower for SoC. IEEE T Circuits-I 2008; 55: 1392-1401.

[8] Hazucha P, Karnik T, Bloechel BA, Parsons C, Finan D,Borkar S. Area-efficient linear regulator with ultra-fast load regulation. IEEE J Solid-St Circ 2005; 40: 933-940.

[9] Chun Ka, Mok PKT. Pole-zero tracking frequency compensation for low dropout regulator. ISCAS 2002: IEEE International Symposium On Circuits And Systems - Proceedings 2002; 4: 735-738.

[10] Man TY, Mok PKT , Chan M. A high slew-rate push–pull output amplifier for low-quiescent current low-dropout regulators with transient-response improvement. IEEE T Circuits-II 2007; 54: 755-759.

[11] Chong S, Chan PK. A 0.9µA quiescent current output-capacitorless LDO regulator with adaptive power transistors in 65-nm CMOS. IEEE T Circuits-I 2013; 60: 1072-1081.

[12] Maity A, Patra A. Trade offs aware design procedure for an adaptively biased capacitorless low dropout regulator using nested miller compensation. IEEE T Power Electr 2016; 31: 369-380.

[13] Keikhosravy K , Mirabbasi S. A 0.13µm CMOS low-power capacitor-less LDO regulator using bulk-modulation technique. IEEE T Circuits-I 2014; 61: 3105-3114.

[14] Saberkari A, Qaraqanabadi F, Shirmohammadli V, Martínez H, Alarcon E. Output-capacitorless segmented low-dropout voltage regulator with controlled pass transistors. Int J Circ Theor App 2016; 44: 460-475.

[15] Shirmohammadli V, Saberkari A, Martínez-García H, Alarcón-Cot E. Enhancing the performance of output-capacitorless LDO regulators by pass-transistor segmentation. ISCAS 2016: IEEE International Symposium On Circuits And Systems – Proceeding 2016; 490-493.

[16] Or PY, Leung KN. An output-capacitorless low-dropout regulator with direct voltage-spike detection. IEEE J Solid-St Circ 2010; 45: 458-466.

[17] Guo J , Leung KN. A 6µw chip-area-efficient output-capacitorless LDO in 90-nm CMOS technology. IEEE J Solid-St Circ 2010; 45: 1896-1905.

[18] Zhan C, Ki WH. An output-capacitor-free adaptively biased low-dropout regulator with subthreshold undershoot-reduction for SoC. IEEE T Circuits-I 2012; 59: 1119-1131.