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An enhanced grey wolf optimization algorithm with improved exploration ability for analog circuit design automation

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Abstract: A novel circuit sizing technique with improved accuracy and efficiency is proposed to resolve the sizing issues in the analog circuit design. The grey wolf optimization (GWO) algorithm has the total number of iterations divided equally for exploration and exploitation, overlooking the impact of balance between these two phases, aimed for the convergence at a globally optimal solution. An enhanced version of a typical GWO algorithm termed as enhanced grey wolf optimization (EGWO) algorithm is presented with improved exploration ability and is successfully applied in analog circuit design. A set of 23 classical benchmark functions is evaluated and the outcomes are compared with recent state of the art. A conventional two-stage CMOS operational amplifier circuit realized in UMC 180nm CMOS technology is used as a benchmark to validate the efficiency and accuracy of the proposed optimization technique. A statistical study is also conducted over the final solution to investigate the exploration ability of the algorithm proving it to be one of the robust and reliable techniques.

Key words: Analog integrated circuit sizing, automated circuit sizing tool, enhanced grey wolf optimization, operational amplifier, robust

1. Introduction

With the scaling of the CMOS process, the demand for the integration of both analog and digital circuits on the same die has increased. Though the analog circuitry in an integrated circuit (IC) is less when compared to its digital counterpart, its complexity and nonlinearity makes the design process more challenging. The technology scaling has put more constraints on the analog circuit design, therefore making the design process more complicated, time-consuming, requiring skill, and costly, resulting in increased overall time-to-market [1]. Automation of digital circuits has been successful over the past few decades due to its structured nature and high level of abstraction. On the other hand, evolution of reliable tools for analog circuit automation is not mature enough, making it an emerging field of research [2],[3].

A typical circuit design process starts with topology selection followed by circuit level implementation, and then its transformation into layout [4]. The nonsuperficial process of obtaining the optimal design parameters to improve the accuracy of the circuit and reduce the design time is done using an iterative soft computing technique. This paper focuses on the second phase of circuit design, i.e, circuit sizing, considering its significance with the presumption that the designer has decided the appropriate topology of the circuit.

The classic analog circuit design automation includes synthesis and optimization. Different synthesis-based approaches available in analog circuit sizing tools are demonstrated in Figure 1 [5].The synthesis phase

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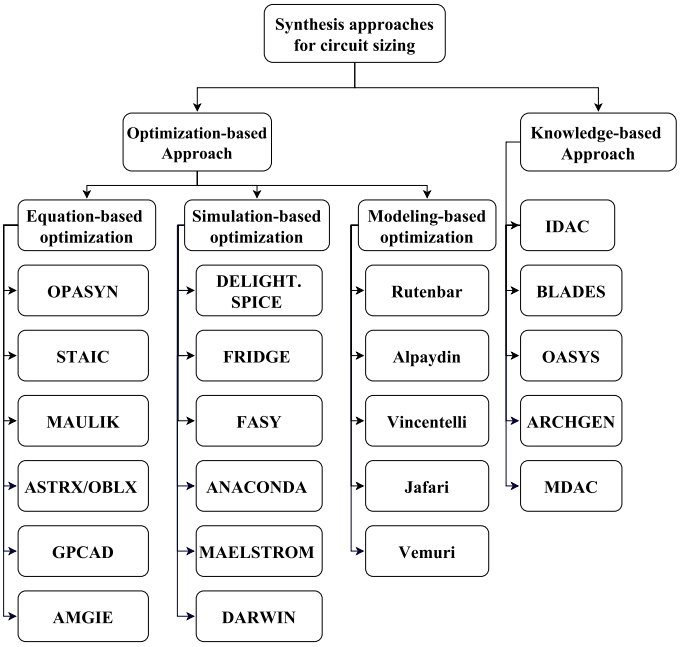

Figure 1. Classification of synthesis in circuit sizing tools [5].

is characterized into knowledge-based and optimization-based approaches. In the knowledge-based approach, as shown in Figure 2a, a design plan is created by the designer considering design equations. Figure 2b demonstrates the optimization-based approach that mostly concentrates on the optimization process rather than following a design plan. The knowledge-based approach has short computation time but long setup time with compromised accuracy besides restriction to a specific set of circuit topologies, making it inefficient. An optimization-based approach includes an optimization engine with equation-based, simulation-based, or modeling-based evaluation procedure as an iterative process. The optimization-based approach is preferred over the knowledge-based approach due to its advantages such as short setup time and better accuracy at the expense of high computation time due to iterations. Nevertheless, with the evolution of high-speed processors, the computation time for analog circuit sizing remains within tolerable limits.

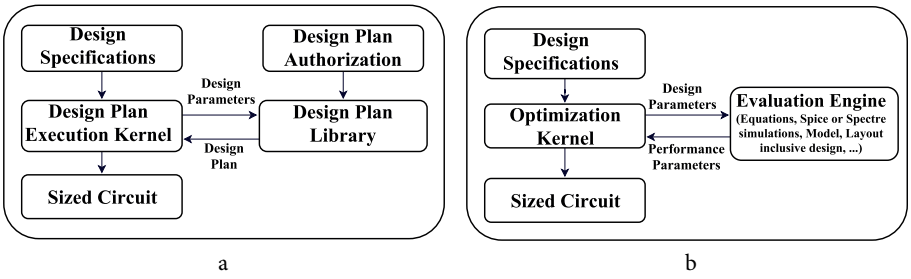

Figure 2. (a) Knowledge-based automatic circuit sizing, (b) optimization-based automatic circuit sizing.

The second phase of analog circuit design automation, i.e., optimization phase deals with iteration of the primary solution obtained during the synthesis phase to optimal values. Optimization techniques are classified as deterministic and metaheuristic [5]. A class of metaheuristic algorithms, viz. swarm intelligence algorithms have gained a significant interest in the development of analog circuit sizing tools due to their robust nature,

ease of implementation, and high flexibility. GWO is one of the recently developed heuristics which is applied in solving various optimization problems such as optimal design of double-layer grids [6] and optimal power flow problem [7]. Besides conventional GWO, different variants were proposed by researchers such as binary GWO [8], parallelized GWO [9], hybrid GWO-PSO [10], integrated GWO-DE [11], and modified GWO [12]. In this paper, enhanced grey wolf optimization (EGWO) algorithm is presented for the automatic sizing of analog circuits by stabilizing the ratio of exploration and exploitation which is the bottleneck of many optimization algorithms in circuit design. The efficiency of the proposed method is then compared with the related techniques that use different algorithms such as particle swarm optimization (PSO) algorithm [13], whale optimization algorithm (WOA) [14], a hybrid of aging leader and challengers (ALC) and PSO algorithm [15], gravitational search algorithm (GSA) [16], advanced GSA (AGSA) [16], and GWO.

The rest of this paper is organized as follows: Section 2 provides a brief overview of the EGWO algorithm. The performance evaluation of the EGWO and its comparison with respect to 23 classical benchmark functions is discussed in Section 3. In Section 4, we discuss the implementation of the presented technique for the design of conventional two-stage operational amplifier in UMC 180 nm CMOS process. Simulation results of the proposed method and their comparison with other circuit sizing tools along with a statistical study is provided in Section 5. Finally, conclusions are drawn in Section 6.

2. Enhanced grey wolf optimization algorithm

The key purpose of an optimization algorithm is to obtain a global optimum. In this process, it has to accomplish two phases, i.e., exploration and exploitation. Exploration deals with scattering the search agents throughout the search space, followed by converging towards a global optimum in the exploitation phase. Proper balance needs to be maintained between exploration and exploitation in order to obtain convergence at global optimum by avoiding local minima. According to the no free lunch (NFL) theorem [17], there exists no single algorithm that can solve all the optimization problems due to the trade-offs between exploration and exploitation. Hence, there is always a need for more sophisticated algorithms to tackle different optimization problems. An effort to refine one of the existing algorithms is presented in the form of EGWO.

The GWO algorithm [18] discusses the mathematical model outlining the social hierarchy and hunting behavior of grey wolfs. In GWO, the exploration and exploitation depend on two parameters: $\overrightarrow{a}$ and $\overrightarrow{A}$. Half of the iterations are devoted to the exploration phase, i.e., when $\left|\overrightarrow{A}\right| \geq 1$ and the other half are assigned to the exploitation phase, i.e., when $\left|\overrightarrow{A}\right| < 1$. Higher exploration results in lower probability of stagnation at local optimum. The modifications are done keeping in mind the ratio of exploration and exploitation that is to be maintained. The EGWO improves the exploration ability by increasing the nonlinearity of the parameter $\overrightarrow{a}$ as shown below:

$$a = \begin{cases} 2\left(1 - \frac{t}{T}\right) & ; \text{ for conventional } GWO \\ 2\left(1 - \frac{t^i}{T^i}\right) & ; \text{ for enhanced } GWO \end{cases}, \tag{1}$$

where t is the present iteration and T is the maximum number of iterations.

The variation of $\overrightarrow{a}$ over the course of 500 iterations for different values of i is shown in Figure **??** that helps in determining the value of i $(= 3)$ for slightly increasing the number of iterations assigned for exploration. Figure **??** shows the variation of $\overrightarrow{A}$ as an effect of variation in $\overrightarrow{a}$ using box plot. Besides changing the value

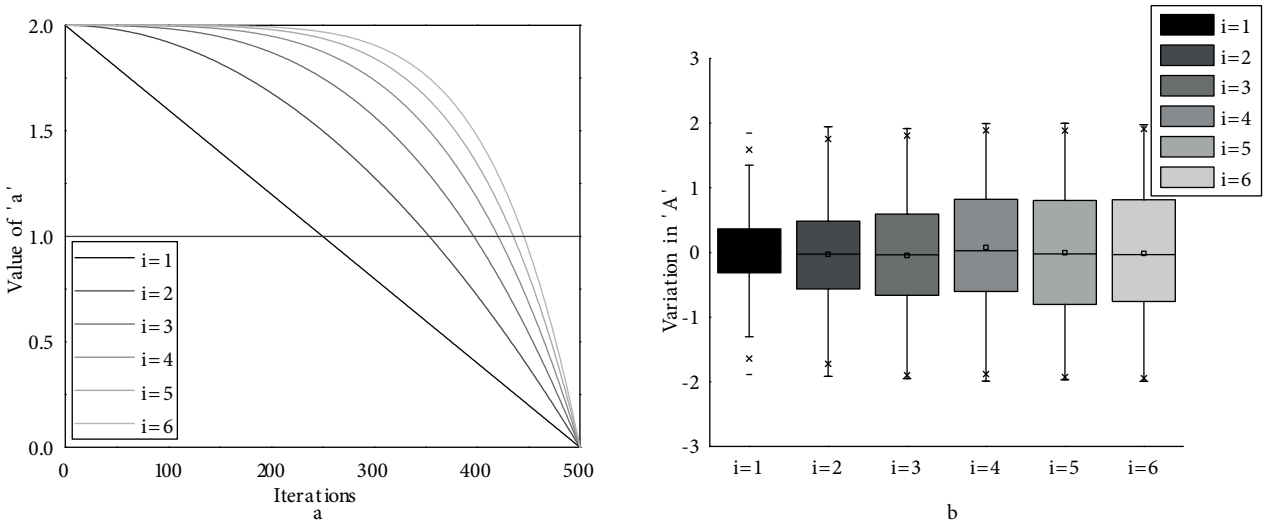

Figure 3. (a)Variation of a over iterations, (b) box plot for values of A.

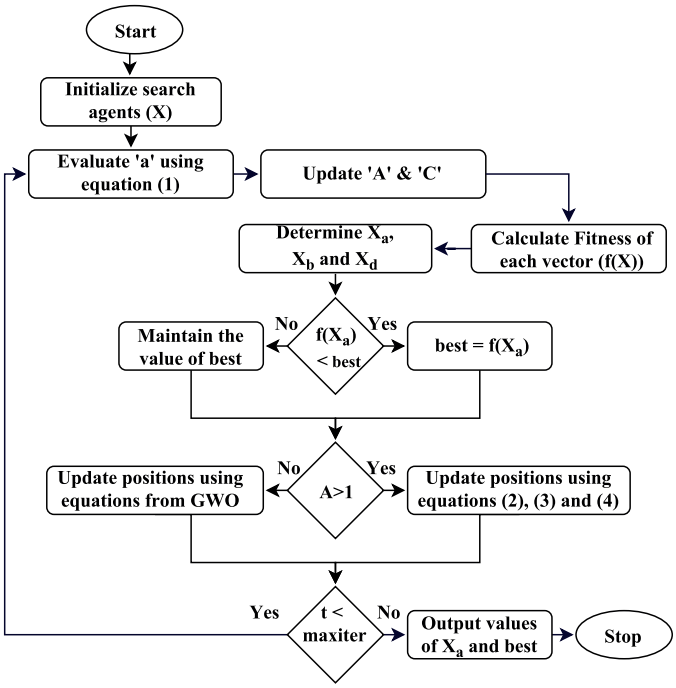

Figure 4. Optimization flow for the EGWO.

of $\overrightarrow{a}$, in order to further improve the exploration ability, the procedure to update the position is modified by including slight randomness in the position update of search agents. Here, a strategy of calculating the vectors $\overrightarrow{D_a}$, $\overrightarrow{D_b}$, and $\overrightarrow{D_d}$ is applied to avoid trapping at local optima. The formulation of the updated positions is as follows:

$$\overrightarrow{D_a} = \left|\overrightarrow{C}_1 \overrightarrow{X_{ra}} - \overrightarrow{X_{rb}}\right|, \overrightarrow{D_b} = \left|\overrightarrow{C}_2 \overrightarrow{X_{rb}} - \overrightarrow{X_{rd}}\right|, \overrightarrow{D_d} = \left|\overrightarrow{C}_3 \overrightarrow{X_{rd}} - \overrightarrow{X_{ra}}\right|, \tag{2}$$

$$\overrightarrow{X_1'} = \left|\overrightarrow{X}_a - \overrightarrow{A_1} \cdot \left(\overrightarrow{D_a'}\right)\right|, \overrightarrow{X_2'} = \left|\overrightarrow{X}_b - \overrightarrow{A_2} \cdot \left(\overrightarrow{D_b'}\right)\right|, \overrightarrow{X_3'} = \left|\overrightarrow{X}_d - \overrightarrow{A_3} \cdot \left(\overrightarrow{D_d'}\right)\right|, \tag{3}$$

$$\overrightarrow{X'}(t+1) = \frac{\left(\overrightarrow{X_1'} + \overrightarrow{X_2'} + \overrightarrow{X_3'}\right)}{3}, \tag{4}$$

where ra, rb, and rd are random search agents from within the population such that $ra \neq rb \neq rd$. The vectors $\overrightarrow{D_a'}$, $\overrightarrow{D_b'}$, and $\overrightarrow{D_d'}$ are used only when the value of A is greater than 1. The optimization framework, shown in Figure 4, demonstrates the iterative process of optimization using the EGWO.

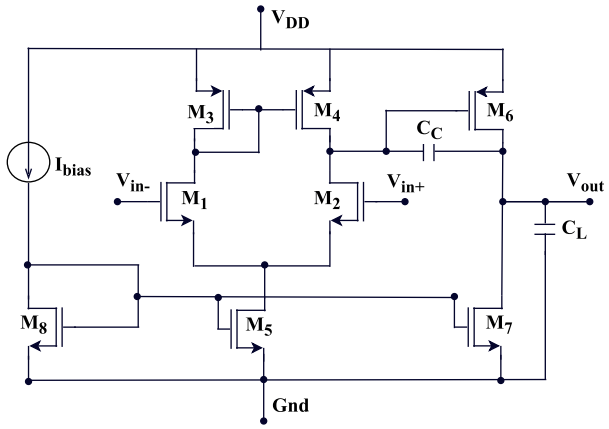

Figure 5. Schematic of miller compensated two-stage CMOS operational amplifier.

3. Performance evaluation of the EGWO

The performance of the enhanced GWO is compared with other algorithms with respect to 23 classical and popular benchmark functions, employed by many researchers, to check the efficiency of the proposed algorithm. These benchmark functions [19] are classified as unimodal, fixed (low) dimensional, and multimodal high dimensional benchmark functions. The simulation results after evaluation of the said benchmark functions, with 20 independent runs, using the proposed EGWO algorithm is compared with other algorithms, namely sine-cosine algorithm (SCA) [20], particle swarm optimization (PSO) [21], grey wolf optimization (GWO), and modified GWO [12]. Table 1 reports the mean, worst, and best-so-far solutions after the final iteration.

Functions $F_1 - F_7$ are unimodal functions that have only global optimum solution and are used to examine optimization algorithms for the rate of convergence. The results for these unimodal functions show that the EGWO outperforms the other algorithms on five out of seven for D=10. For multimodal functions $F_8 - F_{13}$ with many local minima, the final results are more important as they reflect the algorithm's ability to avoid local optima and obtain the near-global optimum. Testing on functions $F_8 - F_{13}$ show that the proposed algorithm performs better than the other algorithms on three out of six multimodal high-dimensional benchmark functions. Functions $F_{14} - F_{23}$ are simpler due to a smaller number of local minima and low dimensionalities. Validation for this set of functions shows that the EGWO performs better than the other algorithms on seven out of ten of the multimodal low-dimensional benchmark functions.

Table 1. Minimization results of 23 benchmark functions over 20 independent runs for $F1 - F23$.

Function		EGWO	MGWO	GWO	SCA	PSO
F1	M	**6.39E-255**	1.77E-203	7.27E-185	6.87E-14	3.65E-22
	B	**0**	3.40E-210	1.50E-188	4.58E-21	6.04E-30
	W	**1.24E-253**	3.32E-202	1.06E-183	7.63E-13	5.29E-21
F2	M	**5.54E-146**	7.04E-119	1.23E-106	4.23E-18	3.92E-10
	B	**4.48E-149**	5.12E-121	3.25E-108	1.64E-22	1.13E-14
	W	**1.02E-144**	3.82E-118	5.16E-106	2.46E-17	5.56E-09
F3	M	**7.03E-69**	1.33E-52	1.00E-52	477.45	0.10697
	B	**2.21E-79**	3.20E-66	7.93E-63	6.56457	0.03107
	W	**1.34E-67**	1.59E-51	1.42E-51	2016.502	0.22511
F4	M	**1.78E-68**	3.84E-53	1.21E-45	2.53889	0.12472
	B	**7.30E-71**	2.97E-56	5.60E-48	0.00605	0.0372
	W	**1.08E-67**	2.77E-52	7.92E-45	9.33451	0.35465
F5	Mean	**26.2359**	26.7851	26.50665	27.94805	49.58214
	Best	25.11832	26.17388	25.23714	27.31307	**3.96877**
	Worst	27.15566	28.54891	**27.14311**	28.87265	124.1508
F6	Mean	0.51215	0.61415	0.63433	3.94743	**9.69E-21**
	Best	1.99E-05	0.25023	1.76E-06	3.26782	**2.64E-29**
	Worst	1.00192	1.49914	1.2534	4.40688	**1.66E-19**
F7	Mean	**0.00016**	0.00032	0.00021	0.00689	0.02041
	Best	**2.57E-05**	0.00011	6.92E-05	0.00049	0.00786
	Worst	**0.00031**	0.00076	0.00049	0.02634	0.03687
F8	Mean	-5806.37	-5705.05	-6485.47	-4195.37	**-6535.5**
	Best	-7523.56	-6501.72	-7602.48	-4901.78	**-7634.22**
	Worst	-3962.7	-4901.58	**-5273.48**	-3651.37	-4103.55
F9	Mean	**0**	**0**	**0**	1.46292	37.31178
	Best	**0**	**0**	**0**	**0**	20.89413
	Worst	**0**	**0**	**0**	23.17803	56.71271
F10	Mean	**7.82E-15**	**7.82E-15**	8.53E-15	12.56573	1.46E-11
	Best	**4.44E-15**	**4.44E-15**	7.99E-15	1.44E-10	1.51E-14
	Worst	**7.99E-15**	**7.99E-15**	1.51E-14	20.23885	1.73E-10
F11	Mean	**0**	0.00129	0.00201	0.02531	0.00824
	Best	**0**	**0**	**0**	**0**	**0**
	Worst	**0**	0.0131	0.03233	0.31675	0.04924
F12	Mean	**0.01091**	0.05028	0.03011	0.50929	0.01136
	Best	1.93E-06	0.01968	0.00655	0.35015	**1.83E-31**
	Worst	**0.04596**	0.14342	0.07216	0.91857	0.10367
F13	Mean	0.39694	0.52992	0.48782	2.17183	**0.00275**
	Best	0.09811	0.19838	0.21072	1.86228	**2.95E-29**
	Worst	1.11513	0.82957	0.83777	2.47633	**0.01099**
F14	Mean	5.11802	4.22526	4.91577	**1.29562**	3.02281
	Best	**0.998**	**0.998**	**0.998**	**0.998**	**0.998**
	Worst	10.76318	12.67051	12.67051	**2.9821**	6.90333
F15	Mean	0.00537	0.00443	0.00532	0.00077	**0.00064**
	Best	0.00031	0.00031	0.00031	0.00032	**0.00031**
	Worst	0.02036	0.02036	0.02036	0.00145	**0.00107**
F16	Mean	**-1.03163**	**-1.03163**	**-1.03163**	-1.03162	**-1.03163**
	Best	**-1.03163**	**-1.03163**	**-1.03163**	-1.03162	**-1.03163**
	Worst	**-1.03163**	**-1.03163**	**-1.03163**	-1.0316	**-1.03163**

Table 1. Continued.

Function		EGWO	MGWO	GWO	SCA	PSO
F17	Mean	0.397888	0.397888	0.397893	0.398391	**0.397887**
	Best	**0.397887**	**0.397887**	**0.397887**	0.397907	**0.397887**
	Worst	0.397894	0.397899	0.398018	0.401533	**0.397887**
F18	Mean	**3**	3.000001	3.000001	3.000001	**3**
	Best	**3**	**3**	**3**	**3**	**3**
	Worst	**3**	3.000006	3.000008	3.000006	**3**
F19	Mean	**-3.86266**	-3.86196	-3.86117	-3.85538	-3.86265
	Best	**-3.86278**	-3.86278	-3.86278	-3.86218	-3.86278
	Worst	**-3.8649**	-3.85592	-3.8549	-3.85418	-3.86278
F20	Mean	**-3.27508**	-3.26041	-3.25905	-2.9348	-3.27444
	Best	**-3.32199**	**-3.32199**	**-3.32199**	-3.16861	**-3.32199**
	Worst	**-3.28476**	-3.08668	-3.08668	-1.91857	-3.2031
F21	Mean	**-9.89793**	-9.39278	-9.6479	-3.45751	-7.62471
	Best	**-10.153199**	**-10.153199**	**-10.153199**	-7.250155	**-10.153199**
	Worst	-5.055198	-5.055197	-5.100635	-0.497293	-5.055198
F22	Mean	**-10.402559**	-10.1389	-10.137125	-4.756824	-9.581963
	Best	**-10.402957**	-10.40295	-10.40292	-7.667205	-10.40294
	Worst	**-10.402101**	-5.12861	-5.087671	-0.907976	-5.087672
F23	Mean	-10.535763	**-10.5361**	-10.265962	-5.282028	-9.727579
	Best	**-10.536409**	-10.5364	-10.5364	-8.559539	-10.536408
	Worst	-10.535106	**-10.5356**	-5.12848	-0.945664	-5.128481

The convergence rates of the EGWO, SCA, PSO, GWO, and MGWO algorithms has been investigated for functions $F_1 - F_{23}$. The descending trend proves the ability of the EGWO in obtaining better approximation of global optimum over the course of iterations. Overall, these results show the potential of the EGWO in solving problems (of the types tested) that cannot be solved efficiently by other algorithms.

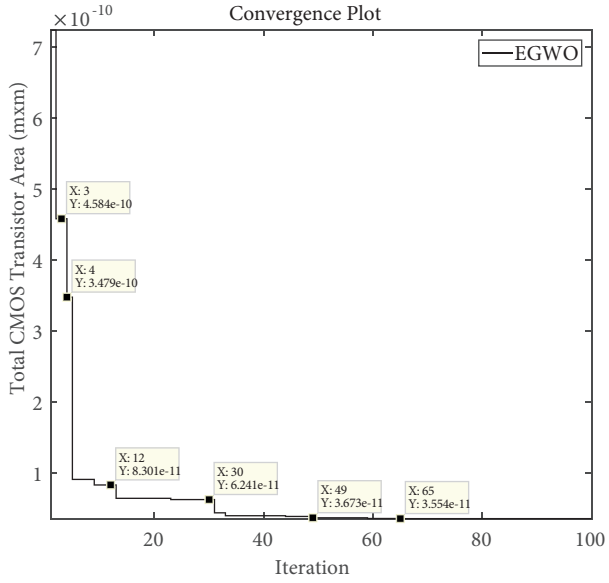

Figure 6. Convergence trend for optimal CMOS transistor area using the EGWO.

4. Formulation of cost function and implementation

The circuit-level implementation and the optimization of the geometrical ratios of MOS transistors for analog circuits employing the EGWO is discussed in this section. Here, the constraints and technology parameters are initialized to obtain the design parameters, i.e., the aspect ratio of the transistors, bias current (I_{bias}), and capacitor values. The process starts with initialization of parameters randomly within the range specified by the designer followed by focusing on the optimization of the cost function. The algorithm results in new values of the design parameters for optimal value of cost function when the termination condition is satisfied.

The circuit selected as a case study for optimization is a two-stage conventional CMOS operational amplifier with miller-compensated topology as shown in Figure 4. The motive of the EGWO is to reduce the overall MOS transistor area while meeting the target specifications of the operational amplifier that includes DC gain (A_v), unity gain bandwidth (UGB), slew rate (SR), common mode voltages (V_{ICmin} and V_{ICmax}), power dissipation (P_d), and load capacitance (C_L). To mitigate the effects of the channel length modulation, the channel length of MOS transistors is taken more than the minimum transistor length, i.e., $L_i = 0.72\ \mu m$ for $i = 1\ to\ 8$. The design parameters of operational amplifier include widths of transistors (W_i for $i = 1\ to\ 8$), capacitances (C_C and C_L), and I_{bias}. After imposing the appropriate matching properties, transistors M1, M3, and M5 are chosen to be identical to M2, M4, and M8, respectively. The empirical equations used for the design of the operational amplifier are explained in [22].

The initial population size for the EGWO algorithm is considered to be a matrix of size (number of particles (P) $\times$ particle vector (Q)), where P = 60 and Q = 7. The particle vector for the optimal design of two-stage CMOS operational amplifier is as follows:

$$X_{opamp} = [A_v, C_L, SR, V_{ICmin}, V_{ICmax}, UGB, P_d]\,. \tag{5}$$

Here, the cost function is defined as the total MOS area occupied (sum of widths $\times$ lengths) by all the transistors which is given as:

$$CF = \sum_{i=1}^{N} (W_i \times L_i)\,, \tag{6}$$

where N is the total number of transistors in a circuit with the desired value of the cost function to be less than 300 μm^2 for the given circuit. Hence, the EGWO algorithm is utilized for obtaining the optimal value of the cost function.

5. Results and discussion

The optimized design of the two-stage operational amplifier, shown in Figure 5, aims to reduce the overall MOS transistor area with constraints on A_v, C_L, SR, V_{ICmin}, V_{ICmax}, UGB, and P_d as given in column 2 of Table 2. The aspect ratios of the MOS transistors obtained from the EGWO using MATLAB are employed for the circuit-level implementation of operational amplifier in Cadence IC616 using the INTEL core i7 4790 CPU@3.60 GHz with 16 GB RAM.

Table 3 shows the optimum design parameters of a two-stage operational amplifier obtained using the EGWO and other related algorithms. The illustration of the optimization trend for optimal design of the two-stage operational amplifier is shown in the form of convergence plot in Figure 6. The convergence plot shows different feasible solutions at different iteration with convergence at an optimal solution (minimum area), which is finally considered for the design of operational amplifier. In Table 2, it can be observed that the EGWO has

Table 2. Results obtained using the EGWO and its comparison using different algorithms.

Design specifications	Target	PSO [13]	WOA [14]	ALC-PSO [15]	GSA [16]	AGSA [16]	GWO	EGWO
A_v (dB)	>60	59.19	74.08	90.85	60.14	81.13	75.38	**77.43**
GBW (MHz)	>3	3	3	112.5	3.136	3.29	3.26	**16.95**
PM $(degrees)$	>45	63.53	–	66.5	47.53	57.91	60.06	**64.86**
SR $(V/\mu s)$	>10	**18.35**	10	161.4	10.29	12.34	11.42	10.05
Pd (mW)	<2.5	0.184	1.137	0.018	1.053	0.332	0.151	**0.094**
CL (pF)	>7	–	**7**	0.05	10.02	10	**7**	**7**
V_{ICmin} (V)	>0.3	–	-0.01	-0.85	-0.86	-1.22	0.3	**0.4**
V_{ICmax} (V)	<1.6	–	**1.1**	0.95	1.8	1.79	1.4	1.2
$CMRR$ (dB)	>60	67.08	–	88.94	81.99	84.6	82.15	**86.31**
$PSRR+$ (dB)	>70	63.84	–	88.94	77.36	97.45	85.62	**87.5**
$PSRR$- (dB)	>70	**99.16**	–	100.3	86.82	84.86	80.15	78.65
$Area(\mu m^2)$	Objective	**28.52**	93.86	10.91	114.6	70.32	43.15	35.56
FOM_{opamp}	Maximum	–	0.43	5.625	0.69	1.09	1.05	6.818
Technology (μm)		0.18	0.18	0.13	0.35	0.35	0.18	0.18
Run-time (s)	Minimum	–	–	–	198.4	308	**0.418**	0.432

Table 3. Design parameters for two-stage operational amplifier using the EGWO.

Design Parameters	Simulation-based		Equation-based				
	GSA [16]	AGSA [16]	PSO [13]	WOA [14]	ALC-PSO [15]	GWO	EGWO
$W1/L1$ $(\mu m/\mu m)$	4/2	4/2	7.74/0.18	4/2	4/2	10/0.7	9.4/0.7
$W3/L3$ $(\mu m/\mu m)$	4/2	4/2	14.4/0.18	5/2	4/2	1/0.7	2.2/0.7
$W5/L5$ $(\mu m/\mu m)$	4/2	4/2	1.96/0.18	2/2	2.8/2	5.7/0.7	2.3/0.7
$W6/L6$ $(\mu m/\mu m)$	21.94/2	7.16/2	98.23/0.18	21.54/2	24/2	20.75/0.7	8/0.7
$W7/L7$ $(\mu m/\mu m)$	11.36/2	4/2	11.97/0.18	5.38/2	9.2/2	7.5/0.7	15/0.7
$W8/L8$ $(\mu m/\mu m)$	4/2	4/2	1.96/0.18	2/2	2.8/2	5.7/0.7	2.3/0.7
I_{bias} (μA)	45.28	30	34.46	49.0	1	21.7	17.4
CC (pF)	4.4	2.2	–	2.45	0.025	1.9	1.65
CL (pF)	10.02	10	–	7	0.05	7	7

the ability to obtain a set of feasible solutions considering designer-specific performance requirements. Figures 7a – 7c show the response of the two-stage operational amplifier to obtain A_v, phase margin (PM), UGB, SR, common mode rejection ratio $(CMRR)$, and power supply rejection ratio $(PSRR)$.5

The proposed technique results in low power, making it relatively preferable for low-power circuit sizing problem. For a fair comparison between recent techniques using algorithms such as CO, PSO, GSAPSO, GSA, and GWO, with application to circuit sizing that utilizes different technologies, figure of merit is considered which is given as follows:

$$FOM_{opamp} = \frac{C_L\,(pF) \cdot UGB\,(MHz)}{I_{bias}\,(\mu A)}. \tag{7}$$

As can be observed from Table 2, the presented EGWO results in better performance as compared to the aforementioned algorithms.

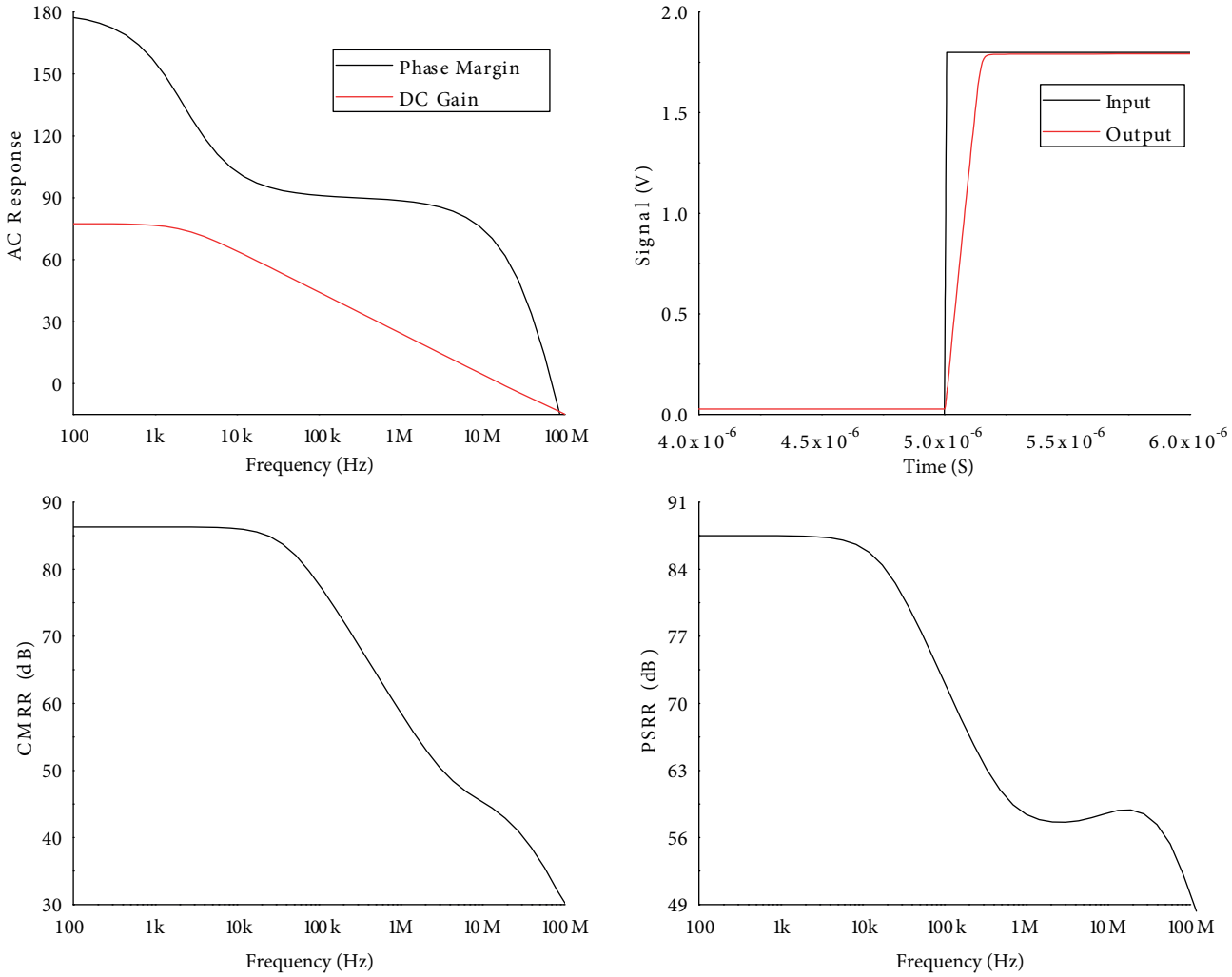

Figure 7. Response of two-stage CMOS operational amplifier, using the EGWO, to obtain (a) gain and phase margin, (b) slew rate, (c) CMRR, and (d) PSRR.

5.1. Statistical study

Metaheuristic algorithms' capability makes their application in IC sizing more comfortable. However, the random nature of these algorithms stops them from producing constant output for every execution. Therefore, executing these algorithms only once may not be enough to comment on their performance. Hence, a statistical study is required to verify the actual performance and robustness of the presented method. The results shown in Table 3 are considered as the best solutions obtained by using the respective algorithms.

The EGWO-based optimization process is repeated for 20 times with 20 different initializations of search agents. Table 4 shows the actual performance of the proposed algorithm for its application to analog circuit sizing, with each column representing the results obtained by using the best, average, and worst solutions from EGWO. Moreover, it is observed that all individual runs lead to feasible solutions which demonstrates the strong exploration ability of the EGWO-based optimization process. The layout for the two-stage operational amplifier for the best, median, and worst solutions obtained using the EGWO is depicted in Figures 8a – 8c respectively, highlighting the MOS area occupied by the circuit.

Table 4. Results obtained using the EGWO and its comparison using different algorithms.

Design Specifications	EGWO (best)	EGWO (median)	EGWO (worst)
A_v (dB)	77.43	65	78
$GBW(MHz)$	16.95	7.56	7.65
PM(degrees)	64.86	65	60.05
$SR(V/\mu s)$	10.05	10.25	10.02
$Pd(\mu W)$	94.5	167	225
$CL(pF)$	7	7	7
$V_{ICmin}(V)$	0.4	0.4	0.5
$V_{ICmax}(V)$	1.2	1.1	1.2
$CMRR(dB)$	86.31	90	90.51
$PSRR+(dB)$	87.5	104.1	107.08
$PSRR–(dB)$	78.65	80.08	80.5
$Area(\mu m^2)$	34.16	77	171.5
FOM_{opamp}	6.818	2.252	2.142

5.2. Corner analysis

Table 5. Results obtained after performing corner analysis on the best solution.

Corner	T (C)	Vdd - 5% (V)			Vdd (V)			Vdd + 5% (V)		
		Av (dB)	GBW (MHz)	PM (Deg)	Av (dB)	GBW (MHz)	PM (Deg)	Av (dB)	GBW (MHz)	PM (Deg)
FF	**-40**	78.15	11.95	69.2	78.12	13.32	67.54	78.21	13.89	66.95
	25	77.65	13.06	67.56	77.62	15.33	64.46	77.61	14.37	66.3
	90	76.77	14.18	65.92	76.61	15.93	63.65	76.57	15.54	64.57
FS	**-40**	77.32	10	71.98	78.32	12.66	68.79	78.32	13.04	68.57
	25	77.12	11.87	69.11	77.83	14.2	66.36	7.79	14.37	66.48
	90	76.44	12.86	67.67	96.98	15.33	64.66	76.85	15.54	64.72
SS	**-40**	76.8	9.6	73.5	78.37	13.67	68.77	77.62	14.94	67.37
	25	77.01	11.44	70.68	77.94	15.33	66.01	76.86	15.54	66.15
	90	76.43	12.86	68.52	77.22	16.13	64.74	75.78	16.16	65.14
SF	**-40**	78.37	12.49	69.61	77.75	14.38	67.52	77.37	15.54	66.13
	25	78	13.63	67.79	77	16.13	64.66	76.33	15.5	65.87
	90	77.24	14.88	65.91	75.89	16.97	63.32	74.88	16.92	63.7
TT	**-40**	78.12	11.16	70.99	78.04	14.82	68.04	78.1	13.65	68.28
	25	77.77	12.86	68.25	77.43	16.95	64.85	77.42	15	66.11
	90	77.04	14.84	65.23	76.56	17.05	64.17	76.37	16.32	64.1

6. Conclusion

Automation of analog circuit design and sizing would have been more successful if the optimization algorithms could have incorporated the major trade-offs like accuracy, robustness, and run-time simultaneously. This paper addresses the challenge by introducing an improved algorithm, i.e., the EGWO, considering it to be a step towards the improved performance of automated sizing tools. Here, the balance between exploration and exploitation is revisited to improve the exploration ability prior to convergence at globally optimal solution. The results obtained after evaluating a set of 23 benchmark functions is compared with algorithms from recent

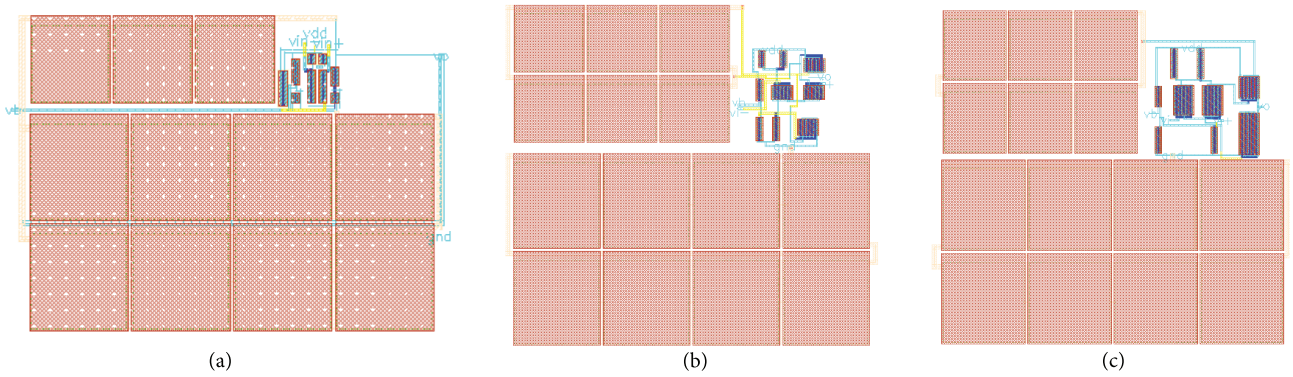

Figure 8. Layout of the two-stage operational amplifier for (a) best, (b) median, and (c) worst solutions obtained using the EGWO.

literature revealing its robustness and better performance owing to higher ability of exploration. Despite the advantages, the EGWO suffers from additional run-time due to inclusion of additional steps in the process of enhancement. The same is validated considering a two-stage CMOS operational amplifier in UMC 180nm technology as a benchmark circuit, resulting in a reduced area and power consumption, in comparison to the foregoing algorithms. To ensure the robustness of the EGWO, a statistical study is performed with over 20 independent runs to return a feasible solution in every case. The challenges faced in this work were fine-tuning the design parameters and design specifications that have been overcome by manual tuning. Further sophistication can be attained by incorporating multiobjective algorithms with progressive constraint handling methodologies in the proposed method.

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