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A novel adaptive hysteresis DC-DC buck converter for portable devices

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Abstract: This paper presents a new technique that adjusts the hysteresis window depending on the variations in load current caused by a voltage-mode circuit to reduce the voltage and current ripples. Moreover, a compact current-sensing circuit is used to provide an accurate sensing signal for achieving fast hysteresis window adjustment. In addition, a zero-current detection circuit is also proposed to eliminate the reverse current at light loads. As a result, this technique reduces the voltage ripple below 8.08 mV_{pp} and the current ripple below 93.98 mA_{pp} for a load current of 500 mA. Circuit simulation is performed using 0.18 μm CMOS process parameters.

Key words: DC-DC buck converter, zero-current detection, hysteresis comparator

1. Introduction

DC-DC buck converters are widely used in portable devices like cellular phones, laptop computers, and digital cameras etc. To obtain the effective power conversion, these converters must satisfy several key specifications, such as wide load current range, low voltage and current ripples, fast transient response, high power efficiency, stable operation, and simplicity. For such conversion, hysteresis DC-DC buck converters have been studied as a core technology [1–8]. However, the conventional hysteresis DC-DC buck converter has low power efficiency at light loads due to its high voltage and current ripples. To improve the power efficiency, a hysteresis DC-DC buck converter was proposed [9]. This converter is based on an adaptive window control circuit to reduce the voltage and current ripples. The input signals for the adaptive window control are generated by additional current-mode circuits. These circuits are composed of a current-sensing circuit, a continuous conduction mode (CCM) and discontinuous conduction mode (DCM) selection circuit, a CCM load-dependent hysteresis circuit, a DCM switching frequency control circuit, and an analog switch circuit. Thus, it can be seen that this approach to control the inductor current is somewhat complex.

In this paper, we present a simple adaptive window control circuit which dynamically generates the high and low hysteresis threshold voltages V_H and V_L by a voltage-mode circuit instead of the current-mode circuit. A current-sensing circuit is compactly designed so that the number of transistors for realizing it is reduced to about half as compared to other current-sensing circuits. Besides, a zero-current detection (ZCD) circuit is proposed not only to completely eliminate a reverse current at light loads, but also to automatically operate in the DCM or the CCM without their selection circuit.

The organization of this paper is as follows. The proposed control strategy and a circuit implementation using hysteresis control are described in Section 2. Simulation results validating the this strategy are presented and discussed in Section 3, and Section 4 gives the conclusion.

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2. Hysteresis DC-DC buck converter

2.1. Conventional hysteresis DC-DC buck converter circuit

Figure 1 shows the block diagram of the conventional hysteresis DC-DC buck converter, consisting of a fixed-window hysteresis comparator, a dead time control circuit, and a power PMOS (M_P) and a NMOS (M_N) switch. The fixed-window hysteresis comparator uses high (V_H) and low (V_L) threshold voltages to compare the output feedback voltage (V_f). When V_f exceeds V_H, the power M_P switch is turned off and the power M_N switch is turned on. When V_f becomes lower than V_L, the power M_P switch is turned on and the power M_N switch is turned off. This repetitive process produces a constant average output voltage. However, owing to the fixed hysteresis window, the voltage and current ripples increase under certain load conditions, thus reducing the power efficiency and potentially rendering the system unstable.

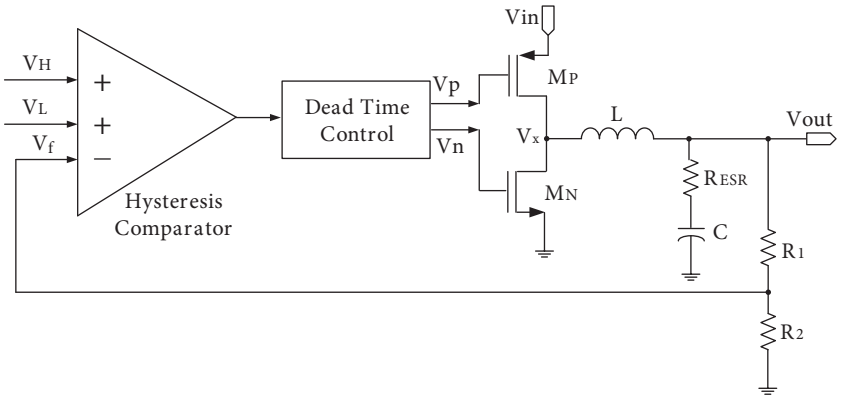


Figure 1. Block diagram of a conventional hysteresis DC-DC buck converter.

2.2. Proposed adaptive hysteresis DC-DC buck converter circuit

Figure 2 shows the control strategy of the proposed adaptive hysteresis DC-DC buck converter. Its salient feature is that the voltage and current ripples are reduced by voltage-mode circuit according to the load, i.e. high load, light load, and very light load.

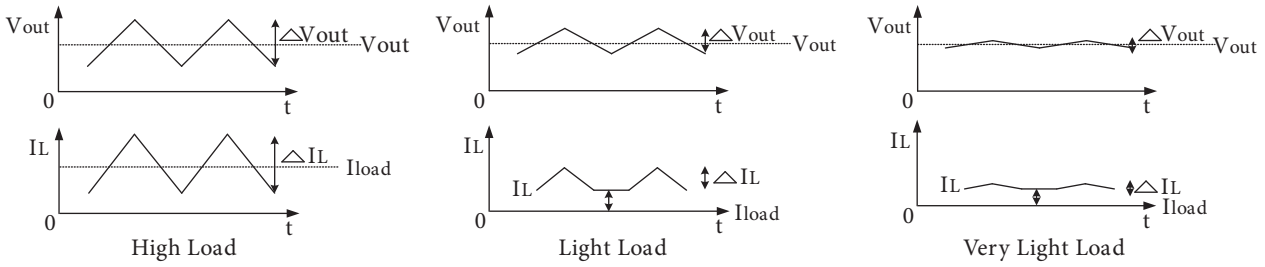


Figure 2. Control strategy of the proposed adaptive hysteresis DC-DC buck converter.

To improve the hysteresis DC-DC buck converter operating parameters, an enhanced control method is proposed, as shown in Figure 3. The distinctive feature of this circuit configuration is that the hysteresis comparator window is automatically controlled by the voltage-mode circuit. It also automatically operates in the DCM or CCM according to the variation in the load current through the proposed ZCD circuit without

their selection circuit. Thus, the proposed architecture is fast-settling and significantly reduces the voltage and current ripples compared to a conventional hysteresis DC-DC buck converter.

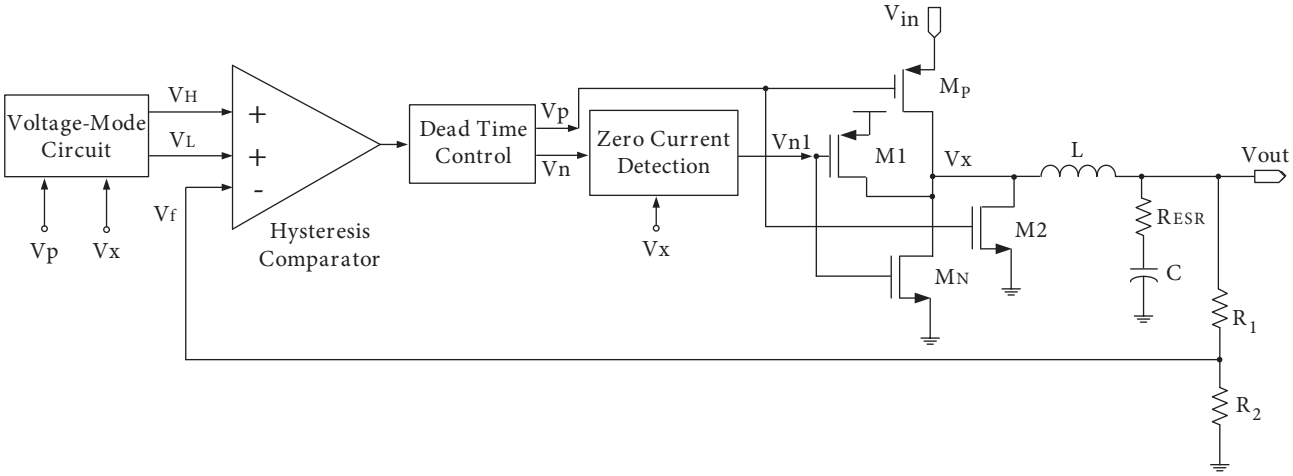


Figure 3. Block diagram of the proposed adaptive hysteresis DC-DC buck converter.

The AC component of the output voltage is given by

$$\Delta V_{\text{out}} = \Delta V_{\text{ESR}}(t) + \Delta V_{\text{c}}(t) = \Delta i_{\text{L}}(t) R_{\text{ESR}} + \frac{1}{C}\int \Delta i_{\text{L}}(t)dt, \tag{1}$$

where the change $\Delta V_{\text{ESR}}(t)$ is the voltage across the parasitic resistance, R_{ESR}, and the change $\Delta V_{\text{c}}(t)$ is the voltage across the capacitor, C. The change $\Delta V_{\text{f}}(t)$ in feedback voltage, V_{f}, can be written as

$$\Delta V_{\text{f}}(t) = \frac{R_2}{R_1 + R_2}\Delta V_{\text{out}} = \frac{R_2}{R_1 + R_2}\left(\Delta i_{\text{L}}(t) R_{\text{ESR}} + \frac{1}{C}\int \Delta i_{\text{L}}(t)dt\right). \tag{2}$$

The hysteresis control is determined by the proportional term, which is the first term in (2). Thus, by omitting the integral term, $\Delta V_{\text{f}}(t)$ and $\Delta i_{\text{L}}(t)$ can be substituted into hysteresis window ΔH_{ys} and inductor current ripple ΔI_{L}, respectively. ΔI_{L} can be written as

$$\Delta I_{\text{L}} = \frac{(R_1 + R_2)\Delta H_{\text{ys}}}{R_2 R_{\text{ESR}}}. \tag{3}$$

The switching frequency, f_{s}, of the buck converter can be written as

$$f_{\text{s}} \simeq \frac{V_{\text{out}}(V_{\text{in}} - V_{\text{out}})}{V_{\text{in}} L}\frac{1}{\Delta I_{\text{L}}}. \tag{4}$$

Then, by substituting Eq. (3) into Eq. (4), the switching frequency f_{s} can be expressed as

$$f_{\text{s}} \simeq \frac{V_{\text{out}}(V_{\text{in}} - V_{\text{out}})}{V_{\text{in}} L}\frac{R_2 R_{\text{ESR}}}{(R_1 + R_2)\Delta H_{\text{ys}}}, \tag{5}$$

where the R_2 is incorporated into the calculation of f_s. Therefore, the switching frequency of the proposed adaptive hysteresis DC-DC buck converter can be increased even for a small value of R_{ESR} by selecting the resistor R_2 appropriately.

Tables 1 and 2 show the state of power MOSFETs according to the hysteresis comparator operation in the CCM and DCM, respectively.

Table 1. The state of power MOSFETs according to the hysteresis comparator operation in the CCM.

Operation condition	Output	Power MOSFET state
$V_f > V_H$	High signal	PMOS M_P : off NMOS M_N : on
$V_f < V_L$	Low signal	PMOS M_P : on NMOS M_N : off

Table 2. The state of power MOSFETs according to the hysteresis comparator operation in the DCM.

Operation condition	Output	Power MOSFET state
$V_f > V_H$	High signal	PMOS M_P : off NMOS M_N : off (Controlled by ZCD)
$V_f < V_L$	Low signal	PMOS M_P : on NMOS M_N : off (Controlled by ZCD)

2.3. Voltage-mode circuit

2.3.1. Current sensing circuit

One of the essential building blocks of the proposed adaptive hysteresis DC-DC buck converter is the current-sensing circuit. The inductor current which provides the information of supply and output voltage should be accurately sensed when the power PMOS (M_P) is on. Several different current-sensing techniques have been published and implemented [9–11]. These techniques suffer from some drawbacks such as complicated circuit design, so such techniques can be limited to current-sensing applications.

Figure 4 shows the compact current-sensing circuit proposed to achieve fast hysteresis window adjustment depending on the variation in the load current. The current flowing through the power PMOS (M_P) is sensed instead of the inductor current. In the on-state, the node voltages V_A, V_B, and V_C can be expressed as

$$V_A = V_{in} - \frac{R_{on3}R_{onP}I_P}{R_{on6}+R_{on3}} = V_{in} - \frac{R_{onP}I_P}{1+\frac{R_{on6}}{R_{on3}}}, \tag{6}$$

$$V_B = V_{in} - (I_{sen}R_{on1}), \tag{7}$$

and

$$V_C = V_A - (I_{on}R_{on4}), \tag{8}$$

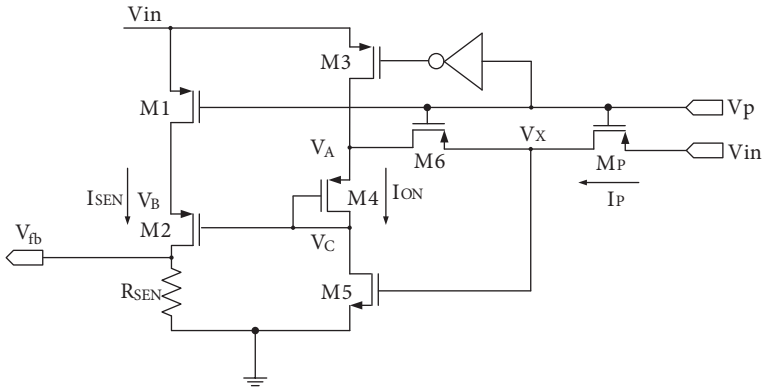


Figure 4. Diagram of the proposed current-sensing circuit.

where I_{P}, I_{on}, and I_{sen} denote the drain current of the power PMOS ($\mathrm{M_P}$), the drain current of M4, and the sense current that flows through M2, respectively. The equivalent resistance between the source and drain can be expressed as

$$R_{\mathrm{on}} = \frac{L}{\mu_{\mathrm{p}} C_{\mathrm{OX}} W (V_{\mathrm{SG}} - |V_{\mathrm{TP}}|)}, \tag{9}$$

where μ_{p}, C_{ox}, L, W, V_{SG}, and V_{TP} represent the effective channel mobility, gate oxide capacitance per unit area, channel length and width of a MOSFET transistor, source-gate voltage, and threshold voltage, respectively. The sense current can be expressed as

$$I_{\mathrm{sen}} = \frac{R_{\mathrm{onP}} I_{\mathrm{P}}}{\left(\frac{R_{\mathrm{on6}}}{R_{\mathrm{on3}}} + 1\right) R_{\mathrm{on1}}}. \tag{10}$$

The sense ratio is determined by the parameter $R_{\mathrm{on6}} / R_{\mathrm{on3}}$ and the aspect ratio of the power PMOS ($\mathrm{M_p}$) and M1. With $R_{\mathrm{on6}} / R_{\mathrm{on3}}$ selected properly, I_{sen} could be sufficiently small for a low-power DC-DC converter with high load current. For adaptive hysteresis DC-DC buck converter application, only the sensing voltage, V_{fb}, is required in a voltage-mode adaptive hysteresis window control circuit during the on-state. In the off-state, there is only a small amount of current flowing through the sensing resistor $\mathrm{R_{SEN}}$.

2.3.2. Voltage-mode adaptive hysteresis window control circuit

Figure 5 shows a voltage-mode adaptive hysteresis window control circuit. The voltage divider formed by resistors R_{on1}, R_{H1}, and R_{H2} generates V_{H} and V_{L} at the two output nodes. The voltage divider input V_{fb} is supplied by a current-sensing circuit depending on the variation in the load current. V_{H} and V_{L} are defined by Eqs. (11) and (12), respectively. ΔH_{ys} is expressed in (13), emphasizing its dependency on V_{fb}.

$$V_{\mathrm{H}} = \frac{R_{\mathrm{H1}} + R_{\mathrm{H2}}}{R_{\mathrm{on1}} + R_{\mathrm{H1}} + R_{\mathrm{H2}}} V_{\mathrm{fb}}, \tag{11}$$

$$V_{\mathrm{L}} = \frac{R_{\mathrm{H2}}}{R_{\mathrm{on1}} + R_{\mathrm{H1}} + R_{\mathrm{H2}}} V_{\mathrm{fb}}, \tag{12}$$

$$\Delta H_{\mathrm{ys}} = V_{\mathrm{H}} - V_{\mathrm{L}} = \frac{R_{\mathrm{H1}}}{R_{\mathrm{on1}} + R_{\mathrm{H1}} + R_{\mathrm{H2}}} V_{\mathrm{fb}}. \tag{13}$$

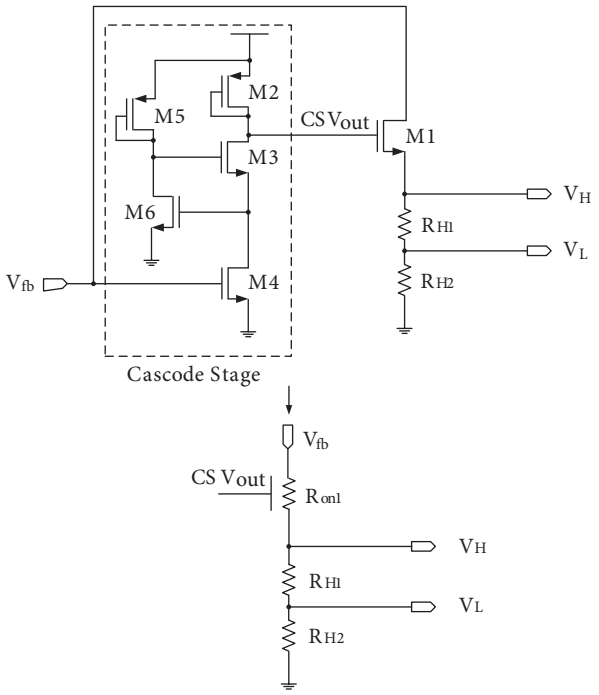


Figure 5. Diagram of the proposed voltage-mode adaptive hysteresis window control circuit.

2.4. Zero-current detection circuit

2.4.1. Conventional zero-current detection circuit

A ZCD circuit is required to improve the power conversion efficiency in the DCM by preventing a reverse current from flowing backwards to the source. Figure 6a shows a schematic of a conventional ZCD. As shown by the waveforms in Figure 6b, this circuit does not completely eliminate a reverse current. The inductor current ramps up when the power PMOS switch is turned on, and ramps down when the power NMOS switch is turned on. The power NMOS switch is turned off by the ZCD circuit when the current decreases and crosses zero in the DCM. At this moment, resonance occurs at the floating V_x node in the inductor and the parasitic capacitors at both ends of the power switches owing to the residual energy present in the reactive elements. The damping produced by the resistance of the inductor itself does not significantly reduce the resonance, owing to its low ohmic value. A large resonance amplitude could greatly affect other circuits, impact power conversion efficiency at light and very light loads, and cause electromagnetic interference (EMI).

2.4.2. Proposed zero-current detection circuit

To resolve these problems, a ZCD circuit with no resonance ringing that also includes a detection and a control logic circuit is proposed, as shown in Figure 7a. When a reverse current is detected at the Vx node, a logic high signal is generated by the comparator and further applied to the clock input of D1. Depending on the load value, Vn and Vp change their frequency. The inverted Vn is connected to the reset at D1 and to the clock at D2. In addition, the D input of D2 is connected to the Q output of D1; thus, the output of D2 is directly influenced by the frequency of Vn. D2 plays one of the most important roles in the proposed ZCD, as shown in Figures 7b and 7c, with its operation depending on the load value. If the load is less than 53 mA (DCM), the Q output of D2 becomes logic low. This signal and Vn pass through the AND gate to turn off the power NMOS

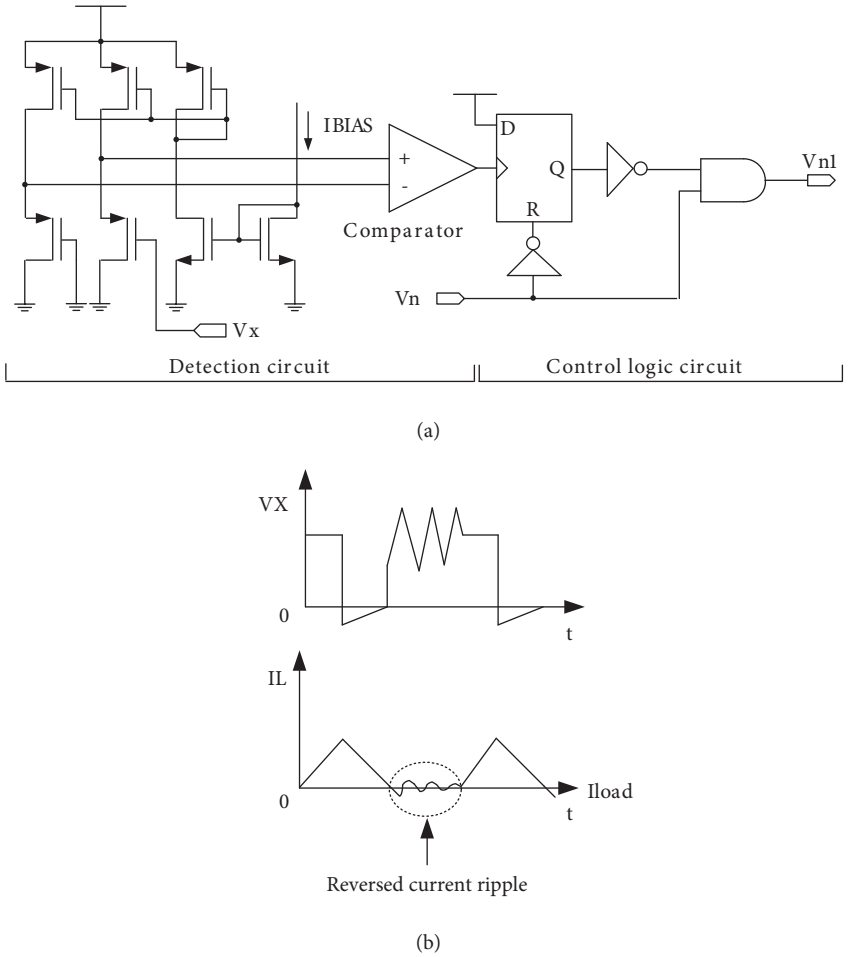


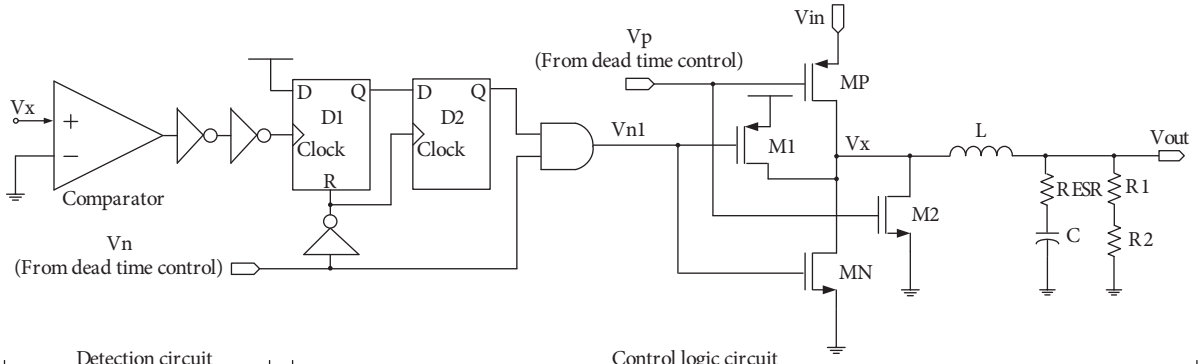
Figure 6. (a) Diagram of a conventional ZCD and (b) output timing diagram when a ZCD event occurs.

M_N switch. Furthermore, if the load is higher than 54 mA (CCM), the Q output of D2 becomes logic high, and this signal and Vn pass through the AND gate to turn on the power NMOS M_N switch. The proposed ZCD circuit automatically operates in the DCM or CCM on the basis of variation in the load current without their selection circuit. The M1 switch is designed so that the leakage current compensation and the output current (inductor current) are allowed to rise from 0 mA to several milliamperes, as shown in Figure 8a. The M2 switch is designed to prevent ringing of the output current, as shown in Figure 8b.

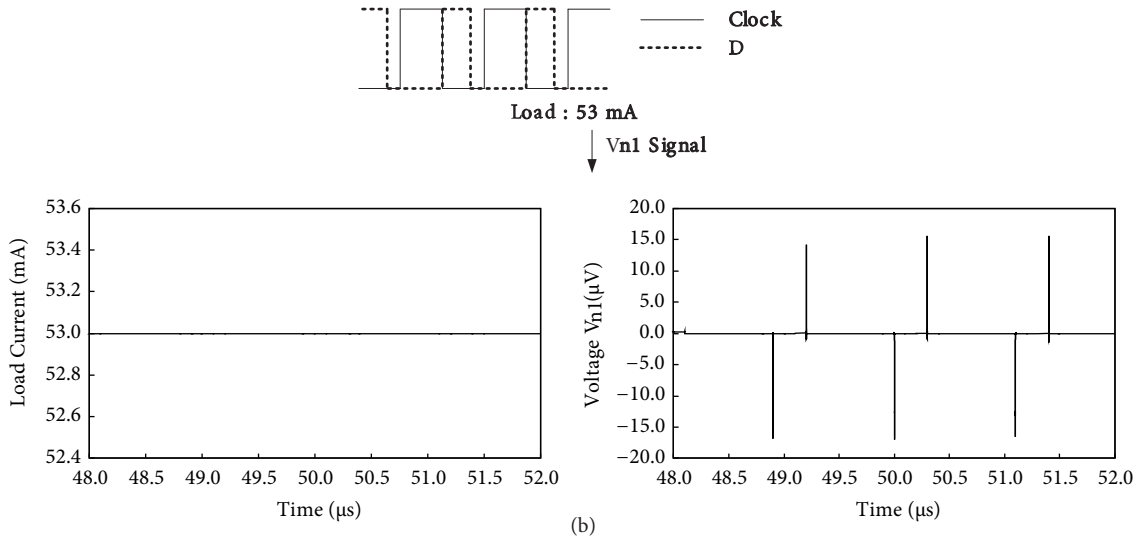
3. Simulation results

Figure 9 shows the voltage and current ripples for a load current of 500 mA at an input voltage of 1.8 V and an output voltage of 1.2 V. The voltage and current ripples of the proposed adaptive hysteresis DC-DC buck converter are estimated respectively at 8.08 mV_{pp} and 93.98 mA_{pp} for the 500 mA load condition, as shown in Figure 9.

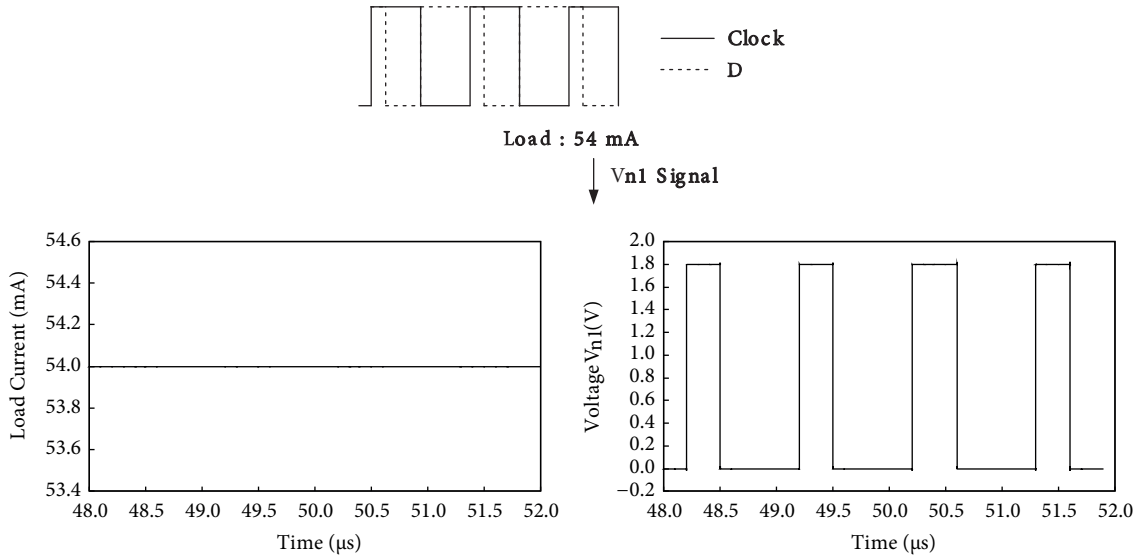
Figure 10 shows the voltage and current ripples in DCM operation under a no-load condition. The voltage ripple is 163.13 μV_{pp}, the current ripple is 2.11 mA_{pp}. Figure 11 shows the current ripple for a load current of 25 mA. The minimum current ripple ΔI_{Lmin} is to increase from 0 mA to 1 mA to prevent ringing and the reverse current.



(a)



(b)



(c)

Figure 7. (a) Diagram of the proposed ZCD and the timing diagrams of V_{n1} for loads of (b) 53 mA and (c) 54 mA.

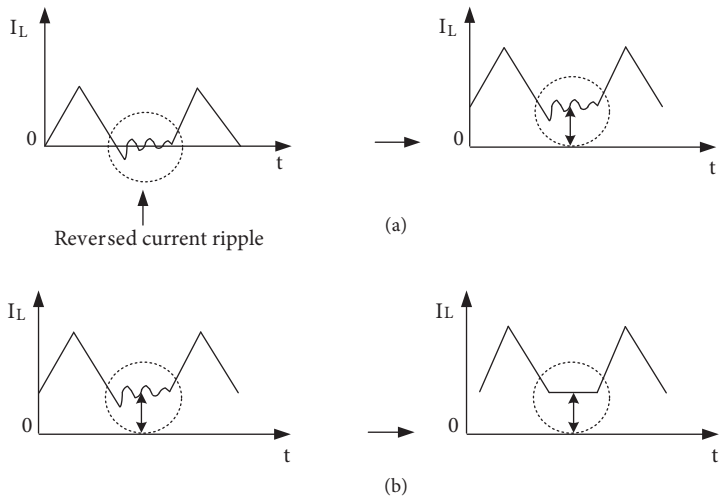


Figure 8. Timing diagrams when the (a) M1 and (b) M2 switches operate.

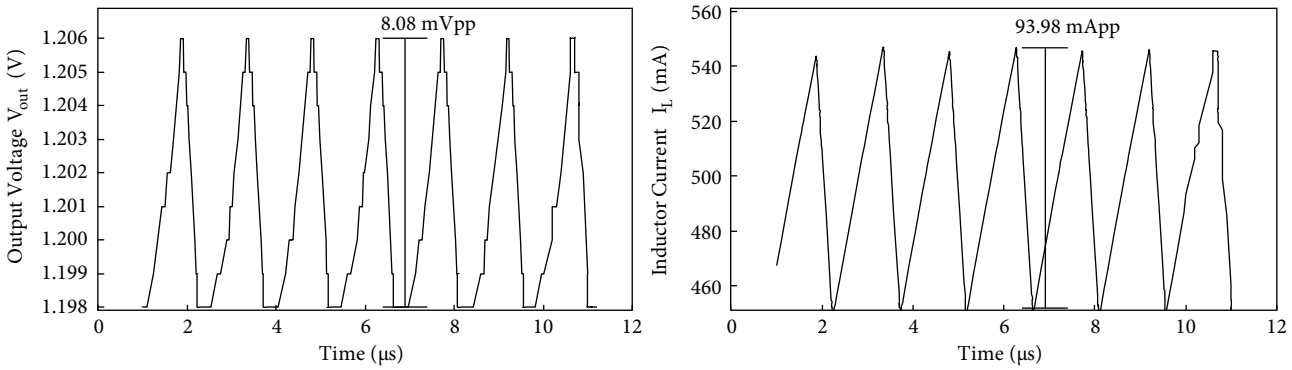


Figure 9. Voltage and current ripples for a 500 mA load current: voltage ripple and current ripple.

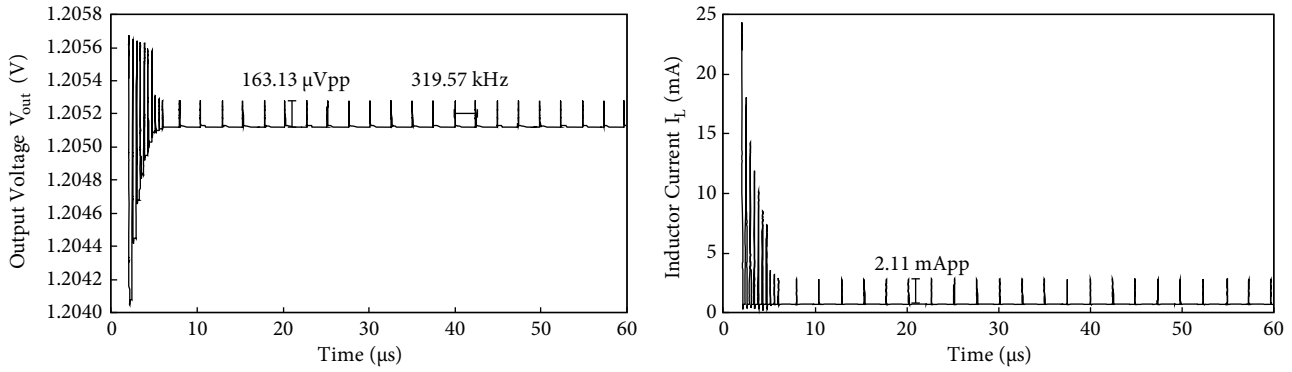


Figure 10. Voltage and current ripples during DCM operation under no-load conditions.

Figure 12 shows the voltage and current ripples under transient load transient conditions, when the load current changes from 0 mA to 500 mA and from 500 mA to 0 mA. For these cases, the output of the proposed adaptive hysteresis DC-DC buck converter can recover within 6.14 μs for a rising load current transient, and within 4.53 μs for a falling load current transient.

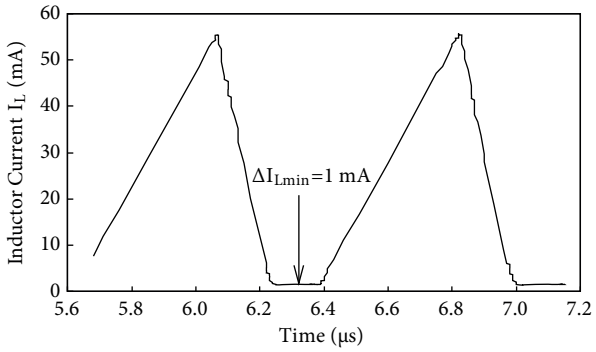


Figure 11. Current ripple of the proposed ZCD during DCM operation for a load current of 25 mA.

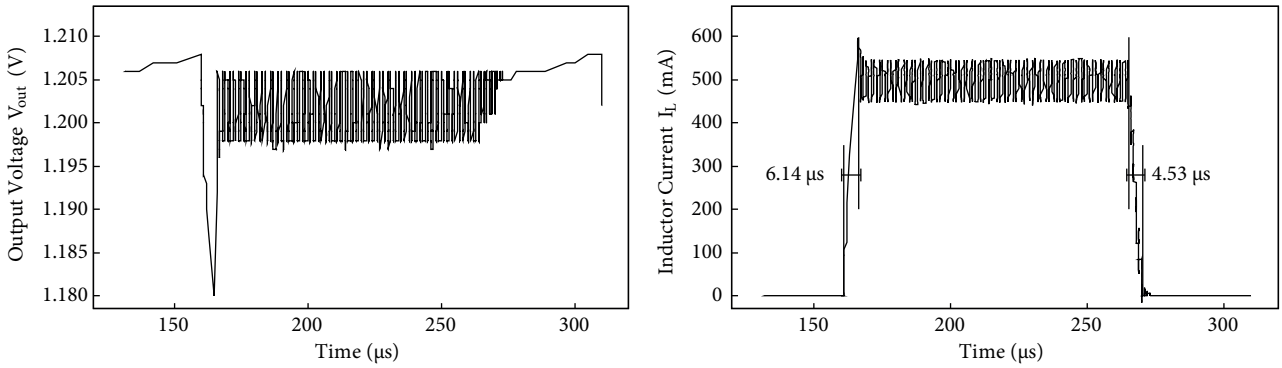


Figure 12. Load transient response voltage and current ripples: load currents from 0 mA to 500 mA and from 500 mA to 0 mA.

Figures 13a and 13b shows comparison of the voltage and current ripples for the conventional and proposed buck converters. The current ripple is reduced from 65% (conventional) to 9% (proposed) and the voltage ripple is reduced from 85% (conventional) to 5% (proposed). Figure 13c compares the power efficiency of the conventional and proposed buck converters, showing that the efficiency of the proposed converter improved by up to 9.5% in the DCM operation. Chiefly, the proposed adaptive hysteresis DC-DC buck converter operates at lower current and voltage ripple, exhibiting higher power efficiency than the conventional hysteretic DC-DC buck converter.

Comparison of the performances of the designed novel adaptive hysteresis DC-DC buck converter with the work [9] is made in Table 3. The circuit simulation of the proposed converter was implemented with 0.18 μm CMOS process parameters. The switching frequency of the proposed converter is from 319.57 kHz to 732.06 kHz for 0 mA to 500 mA load conditions, respectively. The proposed converter reduces the voltage ripple below 8.08 mVpp and the current ripple below 93.98 mApp for a load current of 500 mA. The maximum efficiency of the proposed converter is around 95.2% and the small inductor is able to make the circuit smaller. For demonstrating the fast-transient response, the load current changes from 0 to 500 mA and back to 0 mA with rising time of 6.14 μs and falling time of 4.53 μs.

4. Conclusion

This paper presented a new technique aiming to improve the performance of the conventional hysteretic DC-DC buck converter. The proposed converter adjusts the hysteresis window depending on the variation in

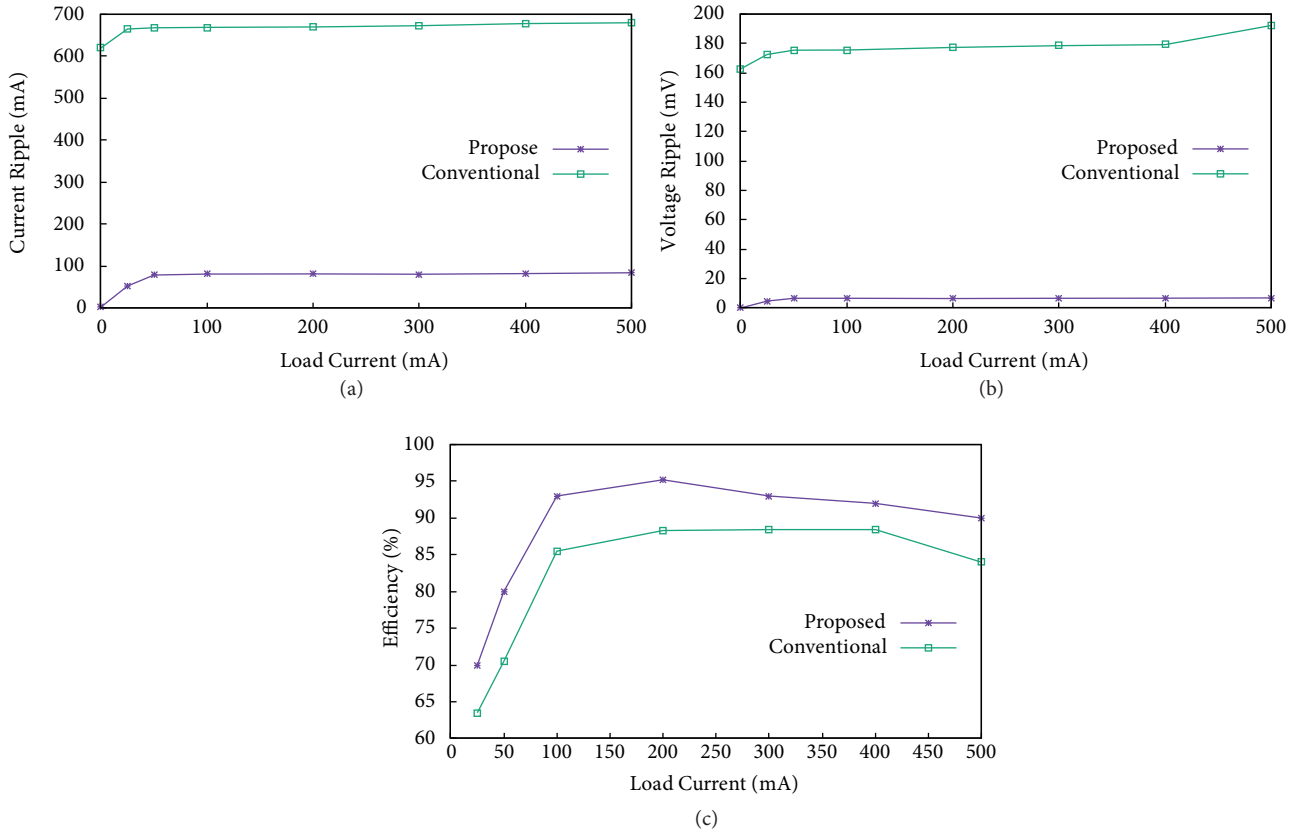


Figure 13. Simulation results at different loads: (a) current ripple, (b) voltage ripple, and (c) power efficiency.

Table 3. Performance comparison.

Parameter	[9]	This work
Technology	0.35 μm	0.18 μm
Switching frequency	35 kHz to 400 kHz	319.57 kHz to 732.06 kHz
Input voltage	5 V	1.8 V
Output voltage	2.9 V	1.2 V
Output inductor, L	20 μH	4.7 μH
Output capacitor, C	20 μF	4.7 μF
Output load current	0 mA to 800 mA	0 mA to 500 mA
Output voltage ripple	15 mV_{pp}@ 500 mA	8.08 mV_{pp}@ 500 mA
Output current ripple	Not included	93.98 mA_{pp}@ 500 mA
Power peak efficiency	96% @ Vout = 2.9 V	95.2% @ Vout = 1.2 V
Transient recovery time	32 μs (0 $\rightarrow$ 800 mA) 10 μs (800 $\rightarrow$ 0 mA)	6.14 μs (0 $\rightarrow$ 500 mA) 4.53 μs (500 $\rightarrow$ 0 mA)

load current. Moreover, a compact current-sensing circuit was proposed to provide an accurate sensing signal for achieving fast hysteresis window adjustment. In addition, this paper presented the novel ZCD circuit to eliminate the reverse current at light loads. This ZCD performance showed that the efficiency of the proposed

converter improved by up to 9.5% in the DCM operation. This ZCD circuit also automatically operates in the DCM or CCM according to the variation in the load current without their selection circuit. Simulation results show that the output voltage ripple can be effectively reduced to 8.08 mV_{pp} to achieve a high power conversion efficiency and excellent regulation performance for a load current of 500 mA. Therefore, the proposed technique can be helpfully used in DC-DC buck converters for portable devices.

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