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A quasi-Z-source active neutral point clamped inverter topology employing symmetrical/unsymmetrical boost modulation control scheme for renewable energy resources

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Abstract: This paper proposes a bipolar quasi-Z-source active neutral point clamped inverter (QZS-ANPCI) topology. It acts as a buck/boost inverter (3-phase, 3-level) to integrate renewable energy resources under their fluctuating DC voltages. We propose a symmetrical/unsymmetrical boost modulation control technique to mitigate the DC-link unbalance voltage problem in an ANPC inverter. This worthwhile control technique exploits voltage-current closed-loops on AC and DC sides to regulate the desired parameters. Moreover, the constant boost control (CBC) modulation has provided a switching sequence that generates a symmetrical/unsymmetrical full shoot-through (FST) state for boosting input DC voltage in the proposed inverter. Detailed loss and efficiency analysis is carried out to show its superior performance under the proposed scheme. Furthermore, the total harmonic distortion (THD) of the proposed QZS-ANPCI meets IEEE Standard-519. Simulink/MATLAB (MathWorks, USA) and PSIM (Powersim, USA) software programs are used to simulate the proposed topology. To verify the theoretical proposals and simulation results, we have developed an experimental prototype setup (1 kW). Both simulation results and experimental data show satisfactory agreement and support the theoretical postulates.

Key words: Z-source inverter, quasi-z-source inverter, buck/boost inverter, neutral point clamped inverter, active neutral point clamped inverter

1. Introduction

Renewable energy resources (RERs) are penetrating into electrical power systems. This trend is due to the rising inevitable problems of global warming. The main reason is the excessive consumption of fossil fuel for energy generation. Over the years, several RERs such as solar, wind, hybrid solar-gas, and biomass resources have been explored and developed for alternative power generation [1]. Power conditioning converters are mandatory to interface RERs with utility grid systems. Therefore, the voltage-fed inverter (VFI) and the current-fed inverter (CFI) are two main conventional power inverters that synchronize these resources with interconnected utility grids. These converters do not have the boost ability during low DC input voltage. Instead, they require separate DC-DC boost converters at their input stage. The Z-source inverter (ZSI) [2], developed in 2003, has a built-in buck/boost characteristic to overcome the above problems. The ZSI exploits unipolar X-shaped impedance (Z)

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integrated with the conventional inverter. It contains capacitors (C) and inductors (L) as passive components. Due to its inherent characteristics, classical converters, such as DC-DC, AC-DC, DC-AC, and AC-AC, can have buck/boost ability working together with the same impedance [3].

An improved form of the ZSI is the QZSI to overcome its problems. There are four distinct QZSI topologies for RERs. These topologies have various advantages, such as a continuous input current, lower component ratings, reduced component count, reduced input source stress, and simplified control strategies compared to the conventional ZSI [4]. There are many pulse-width modulation (PWM) techniques for ZSIs. These techniques include simple boost control (SBC), maximum boost control (MBC), constant boost control (CBC), and developed space-vector pulse width modulation (SVPWM) control. The conventional ZSI topologies have employed modulations in different research works [5, 6].

The most popular multilevel inverter developed to overcome the limitations of VFIs is the neutral point clamped inverter (NPCI). This is because it has lower voltage stresses, switching losses, conduction losses, switching frequency, and THD than those of 2-level inverters [7, 8]. Therefore, it has many applications at medium voltage levels. Furthermore, the authors of [9] applied the z-source impedance concept in NPCI. Also, the works in [10, 11] derived a Z-source NPCI structure to decrease the number of passive components and also proposed a modulation scheme. Due to improved performance of the quasi-Z-source impedance, the works in [12, 13] presented a proposed single-phase quasi-Z-source NPCI and its modulation scheme. To overcome the drawbacks of the traditional Z-source NPCI, the work in [14] also presented two transformer-based z-source NPCI structures. Recently, Yu [15] demonstrated a simulation-based proposed quasi-Z-source NPCI topology with reduced capacitor voltage. Another research study in [16] proposed an LC-switched NPCI topology to reduce the number of passive components. This topology multilevel inverter uses a symmetrical boosting control method (FST).

Furthermore, the authors of [17] proposed a 3-level boost PFC converter and control scheme to improve voltage imbalance and zero current distortion. They can feed to linear loads as well as nonlinear loads nonsymmetrically. The authors of [18] developed a PFC rectifier-based multilevel boost converter using a nonsymmetrical active capacitive divider structure. This structure reduces the switching losses and uses a smaller inductor. Also, 4-level operation is achieved instead of 3-level converter operation with the same number of components . Another research study implemented a single voltage source-based DC-link capacitors voltage balancing technique for NPC inverters using an inductor boost topology [19]. This used a single source-based simple DC-DC boost stage at the NPCI input.

Recent studies have explored new multilevel boost topologies and control strategies to provide improved performance. The work in [20] developed a single-phase modified quasi-Z-source cascaded hybrid inverter (5-level). This uses a greater number of components and uses only a symmetrical boosting technique for a single input source. This is a cascaded topology with a greater number of components. Moreover, a dual-T-type seven-level boost ANPC topology, proposed in [21], provides a scheme for balancing the voltage of floating capacitors (FCs). This scheme feeds to a 3-phase load using a single input source. This converter topology is two-staged dual T-type and increases the complexity.

For recent control techniques, the work in [22] proposed a PWM strategy for a cascaded H-bridge inverter to cope with unbalanced DC input sources. This study does not have a voltage boosting stage in cascaded topology. In the same way, the SVPWM technique proposed in [23] can balance neutral point voltage in a low voltage T-type NPC inverter. It generates nonsymmetrical shoot-through states to deal with input voltage

variations. Similarly, the carrier-based PWM technique was developed for two separate PV MPPTs supplying power to a T-type inverter (3-level) [24].

However, this paper focuses on two independent input voltage sources (positive and negative sides) instead of a single input voltage source. These sources may be RERs with large variations of voltages independently. This study also proposes a symmetrical/unsymmetrical boost control technique for independent RERs using modified CBC-PWM to provide balanced DC-link voltages. This mitigates the problem of unbalancing DC and AC voltages and improves the performance of converter, whereas the conventional Z-source NPC or multilevel inverter offers the feature of symmetrical boosting control method (FST). They are usually designed to feed the 3-phase balanced loads if input voltages sources are equal and identical, but if positive and negative side input voltages are independent RERs and their magnitude fluctuates then they suffer from unbalancing output voltage, increased THDs, and neutral point shifting issues. They require an unsymmetrical boost control method to overcome these issues.

In this paper, we have contributed to the literature in the following ways. First, we have proposed a QZS-ANPCI topology. Since the multilevel ANPCI has superior performance as compared to multilevel NPCI [17, 18], a 3-level ANPCI topology has been combined with a dual quasi-Z-source impedance network. We have developed a modulation control scheme to provide its efficient performance. To evaluate the results, we have performed a simulation of the proposed system in Simulink/MATLAB and PSIM softwares. Finally, we have verified these results by developing a hardware prototype model.

The structure of this article is as follows: Section 1 has described the background history of ZSI topology. Section 2 presents the theoretical development of the control scheme. Section 3 provides a detailed theoretical and mathematical analysis of the proposed topology. Section 4 presents the simulation results. Section 5 illustrates experimental results and discussion. Section 6 evaluates the conclusion.

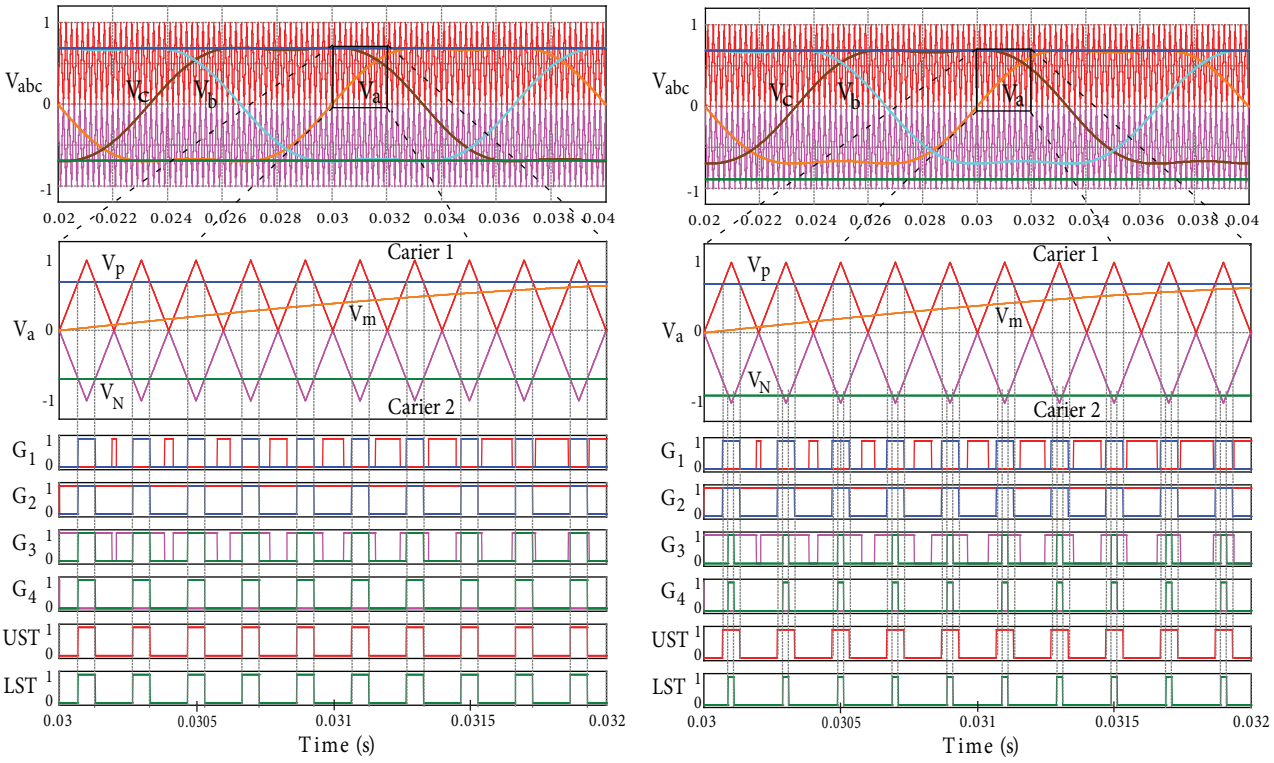
2. Proposed control strategy and modulation technique

Previously, the authors of [6] proposed a constant boost control (CBC) modulation as depicted in Figure 1a. It has better performance as compared to other PWM modulation techniques. Moreover, this technique has increased modulation index M, from 1 to $2/\sqrt{3}$. The reference voltages (Va, Vb, Vc) are mixed with a third harmonic component having 1/6 the magnitude of the fundamental component to form CBC modulation signals. When carrier signals exceed two straight lines (V_P, V_N), then uniform upper and lower ST pulses are generated. The upper and lower side ST pulses turn on the inverter leg switches (G_{1X}, G_{2X}, G_{3X}, $X = \{1,2,3,4\}$) simultaneously in the traditional FST state for a short period of time. However, in the proposed modulation technique, upper side inverter switches ($G_{1X}, G_{2X}, G_{3X}, G_{Y5}, X = \{1,2\}, Y = \{1,2,3\}$) undergo the on-state simultaneously to produce the upper side ST state. The lower side switches ($G_{1X}, G_{2X}, G_{3X}, G_{Y6}, X = \{3,4\}, Y = \{1,2,3\}$) conduct to generate the lower side ST state. These pulses have upper and lower side ST duty ratios (D_{0P}, D_{0N}) to boost input DC voltages. If the upper side ST duty ratio (D_{0P}) is equal to the lower side ST duty ratio (D_{0N}), then FST and full nonshoot-through (FNST) states are generated [11]. This type of traditional voltage boost is known as symmetrical boost conversion. The single carrier-based CBC generates ST states with a frequency two times the carrier frequency. However, bipolar carrier-based CBC produces the same ST states at the frequency as that of carriers.

If upper and lower ST duty ratios (D_{0P}, D_{0N}) have different values, then first FST occurs and next either the upper or lower ST state occurs in a switching cycle as illustrated in Figure 1b. The modulation

scheme calculates the modulation index M taking the highest ST duty ratio that is the greater value among D_{0P} and D_{0N}. Therefore, this type of proposed voltage boost is called unsymmetrical boost conversion. The proposed modulation technique can perform both symmetrical and unsymmetrical boost conversion. These ST states are inserted into zero states of traditional inverter. This type of modulation does not distort AC side power flow. The ST duty ratio (D) is expressed by Eq. (1).

$$D = \left(1 - \frac{\sqrt{3}M}{2}\right) \tag{1}$$



(a) Traditional constant boost control (CBC) using symmetrical boost modulation scheme

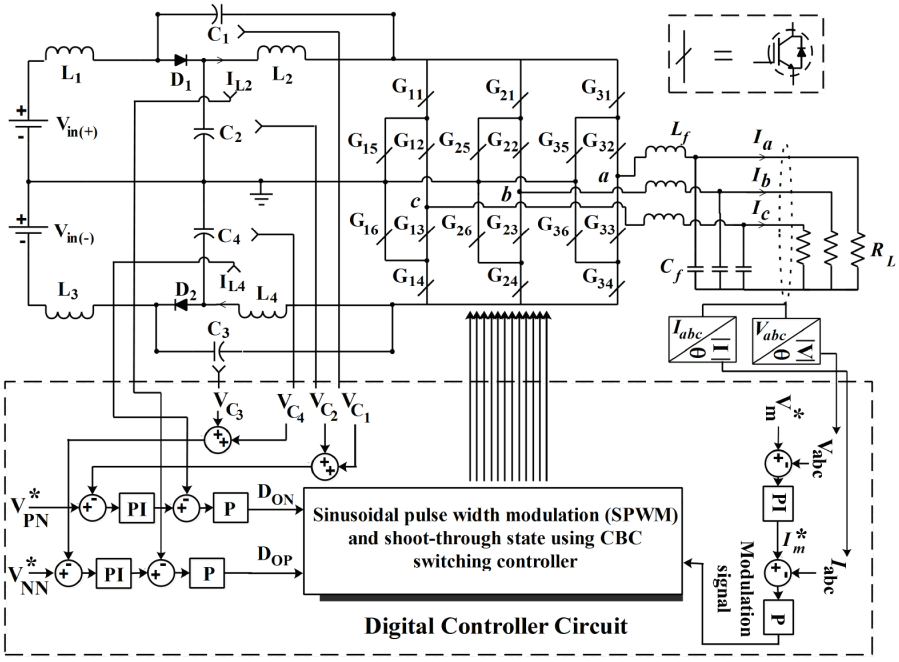
(b) Proposed constant boost control (CBC) using unsymmetrical boost modulation scheme

Figure 1. Traditional and proposed modulation schemes.

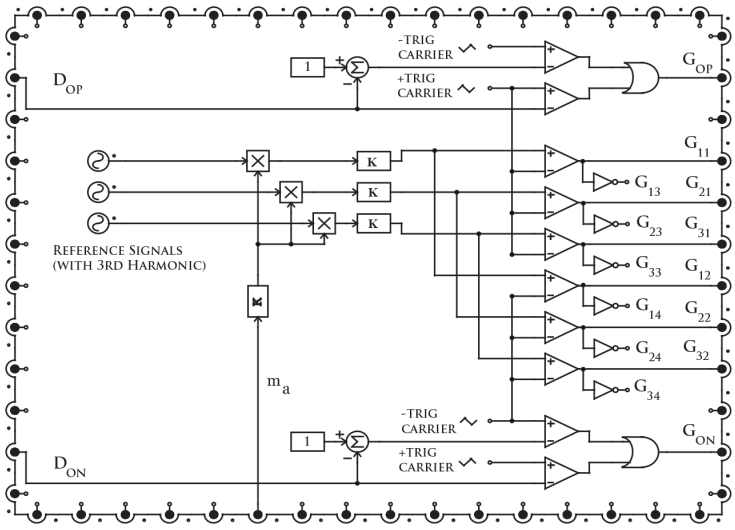
3. Proposed quasi-Z-source ANPC inverter (QZS-ANPCI) topology

Here we present the proposed QZS-ANPCI topology and its detailed control scheme for RERs, as illustrated in Figures 2a and 2b. The operating principle is equivalent to that of a conventional buck/boost Z-source NPC inverter [11]. In this proposed topology, there are four switching modes of operation over one switching time period (T). These modes repeat the ST and NST states two times in a switching sequence.

Moreover, we propose the proportional integrator (PI) regulator, proportional (P) regulator, and control scheme according to [19, 20]. There are two DC-side voltage-current closed-loop controllers. Here, the DC-link voltages (V_{PN}*, V_{NN}*) used in each outer loop with the PI regulator are reference constant voltages. The feedback DC-link voltages (V_{PN}, V_{NN}) are compared with the reference DC-link voltages. An output of the



(a)



(b)

Figure 2. Detailed schematic of proposed QZS-ANPCI and its control scheme: (a) proposed topology and its control scheme, (b) internal detailed controller block of proposed SPWM with CBC technique.

outer loop PI regulator ensures tracking of the desired DC-link voltage. However, the feedback inductor currents (I_{L1}, I_{L3}) used in the inner loop with the P regulator rapidly improve the dynamic response. These controllers generate the upper and lower side ST signals to boost the input DC voltages.

In the same way, there is one AC-side voltage-current closed-loop controller in the control scheme. The output RMS voltage (V_{abc}*), used as a reference voltage, is compared with the feedback AC voltage (V_{abc}). The purpose of the outer loop PI regulator is to track the desired AC voltage under load current variation. While

the load current (I_{abc}) quickly improves dynamic response by using it in the inner loop with a P regulator, the AC-side closed-loop controller produces a modulation signal. The digital microcontroller logically combines the preceding ST signals and modulation signal by using the CBC technique. The values of these AC- and DC-side parameters are provided in Section 5 for simulation and experimentation.

3.1. Modes 1 and 3: first ST state ($0 \leq t < 0.5\ D_{OP}T$) and second ST State ($0.5\ T \leq t < 0.5\ (1 + D_{ON})\ T$)

In the proposed modulation, there are two lower and upper side ST duty ratios (D_{0P}, D_{0N}) whose time intervals (T_{0P}, T_{0N}) can be described by Eqs. (2) and (3). If both ST duty ratios are equal, then upper and lower side switches in each inverter leg conduct simultaneously as a traditional FST state, which is shown in Figure 3a. However, if both sides' ST duty ratios are discrete, the upper side switches and lower side switches can go into separate ST and NST stages just after the FST stage as depicted in Figures 3b and **??**. In this case, diodes $D1$ and $D2$ become reverse-biased. Here, there is no power transfer to the AC load during the FST state. Table 1 provides the equations of the proposed QZS-ANPCI topology during the ST state.

$$T_{0P} = \left(\frac{D_{OP}}{2}\right) T \tag{2}$$

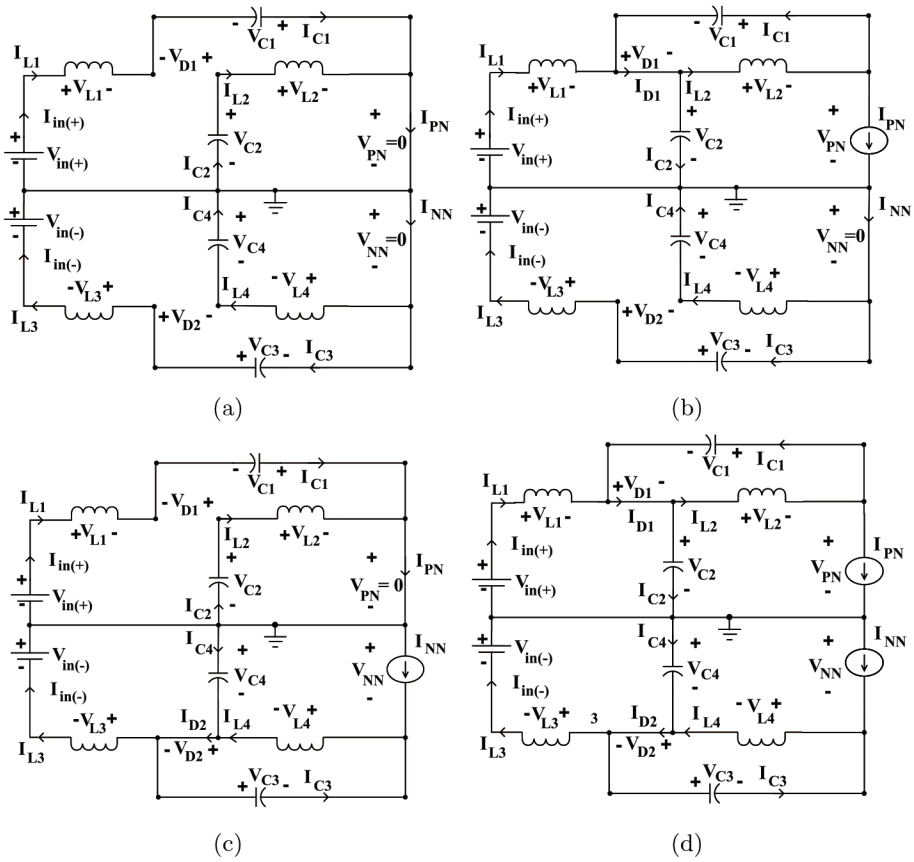


Figure 3. Symmetrical/unsymmetrical boost mode operation of proposed QZS-NPCI: (a) FST state in symmetrical boost mode, (b) UST and lower NST state in unsymmetrical boost mode, (c) LST and upper NST state in unsymmetrical boost mode, (d) FNST state in symmetrical boost mode.

$$T_{0N} = \left(\frac{D_{ON}}{2}\right) T \tag{3}$$

Table 1. Equations during ST and NST states.

Sr. no.	Equations during NST state	Equations during ST state
1	$V_{L1} = V_{in(+)} - V_{C2}$	$V_{L1} = V_{in(+)} + V_{C1}$
2	$V_{L2} = -V_{C1}$	$V_{L2} = V_{C2}$
3	$V_{PN} = V_{C2} - V_{L2} = V_{C2} + V_{C1}$	$V_{PN} = 0$
4	$V_{D1} = 0$	$V_{D1} = V_{C1} + V_{C2}$
5	$V_{L3} = V_{in(-)} - V_{C4}$	$V_{L3} = V_{in(-)} + V_{C3}$
6	$V_{L4} = -V_{C3}$	$V_{L4} = V_{C4}$
7	$V_{NN} = V_{C4} - V_{L4} = V_{C4} + V_{C3}$	$V_{NN} = 0$
8	$V_{D2} = 0$	$V_{D2} = V_{C3} + V_{C4}$

3.2. Modes 2 and 4: first NST state ($0.5D_{OP} \leq t < 0.5T$) and second NST state ($0.5\ (1 + D_{ON})\ T \leq t < T$)

Similarly, the NST states of both modes are similar to those of the classical VFI. In the proposed topology, input sources with quasi-Z-source impedances act as current sources during NST states. The power transfers from the DC input towards the AC load in these states. Moreover, diodes $D1$ and $D2$ conduct for equal upper and lower NST time intervals just like conventional modulation, as shown in Figure 3d. However, in the proposed modulation, upper and lower NST states can have discrete time intervals (T_{1P}, T_{1N}) as given by Eq. (4) and Eq. (5). In this case, upper and lower NST states occur separately as described in Section 3.1. Table 1 gives the equations of the proposed QZS-ANPCI topology during the NST time interval.

$$T_{1P} = \left(\frac{1 - D_{OP}}{2}\right) T \tag{4}$$

$$T_{1N} = \left(\frac{1 - D_{ON}}{2}\right) T \tag{5}$$

3.3. Case 1: Unsymmetrical boost operation

If an ANPC inverter has either different RERs as input sources or unbalanced loads, then unsymmetrical boost conversion becomes necessary. By applying the voltage-second principle on inductors over one switching time period (T), Table 2 formulates the capacitor voltages. In addition, this table mathematically denotes the positive side DC-link voltage as V_{PN} and negative side DC-link voltage as V_{NN}. Furthermore, the peak DC-link voltage $V_{0,NPC}$ across the proposed QZS-ANPCI bridge, in the case of the unsymmetrical boost conversion, is calculated as follows.

$$V_{0,NPC} = V_{PN} + V_{NN} = \left(\frac{1}{1 - 2D_{0P}}\right) V_{in(+)} + \left(\frac{1}{1 - 2D_{0N}}\right) V_{in(-)} \tag{6}$$

Table 2. Equations during ST and NST states.

Sr. no.	Voltage	Equations over one switching cycle
1	$\sum V_{L1(AVG)} = 0$	$\left(\frac{1-D_{OP}}{2}\right) T\left(V_{in(+)} - V_{C2}\right) + \left(\frac{D_{OP}}{2}\right) T\left(V_{in(+)} + V_{C1}\right) = 0$
2	$\sum V_{L2(AVG)} = 0$	$\left(\frac{1-D_{OP}}{2}\right) T\left(-V_{C2}\right) + \left(\frac{D_{OP}}{2}\right) T\left(V_{C1}\right) = 0$
3	$\sum V_{L3(AVG)} = 0$	$\left(\frac{1-D_{ON}}{2}\right) T\left(V_{in(-)} - V_{C4}\right) + \left(\frac{D_{ON}}{2}\right) T\left(V_{in(-)} + V_{C3}\right) = 0$
4	$\sum V_{L4(AVG)} = 0$	$\left(\frac{1-D_{ON}}{2}\right) T\left(-V_{C4}\right) + \left(\frac{D_{ON}}{2}\right) T\left(V_{C3}\right) = 0$
5	V_{C1}	$\left(\frac{D_{OP}}{1-2D_{OP}}\right) V_{in(+)}$
6	V_{C2}	$\left(\frac{1-D_{OP}}{1-2D_{OP}}\right) V_{in(+)}$
7	V_{C3}	$\left(\frac{D_{ON}}{1-2D_{ON}}\right) V_{in(-)}$
8	V_{C4}	$\left(\frac{1-D_{ON}}{1-2D_{ON}}\right) V_{in(-)}$
9	$V_{PN} = V_{C1} + V_{C2}$	$\left(\frac{1}{1-2D_{OP}}\right) V_{in(+)}$
10	$V_{NN} = V_{C3} + V_{C4}$	$\left(\frac{1}{1-2D_{ON}}\right) V_{in(-)}$

3.4. Case 2: Symmetrical boost operation

If the QZS-ANPCI has balanced load and equal input voltage sources, then FST and FNST states are utilized in modulation for symmetrical boost conversion. Since $V_{in(+)} = V_{in(-)} = V_{in}/2$ and $D_{0P} = D_{0N} = D$, therefore:

$$V_{0,NPC} = \left(\frac{1}{1-2D}\right) V_{in} = BV_{in} \tag{7}$$

Here, $B = 1/(1-2D)$ is a voltage boost factor and D is a shoot-through duty ratio in FST modulation. The peak output voltage can be written in buck mode of operation as follows.

$$V_{ac,peak} = M\left(\frac{V_{0,NPC}}{2}\right) = \left(\frac{M}{1-2D}\right)\frac{V_{in}}{2} \tag{8}$$

In boost mode of operation, Eq. (8) can be rewritten as follows.

$$V_{ac,peak} = \left(\frac{G}{1-2D}\right)\frac{V_{in}}{2} \tag{9}$$

The overall voltage gain can be given as:

$$G = MB = \frac{V_{0,NPC}}{V_{in}} = \left(\frac{M}{1-2D}\right) \tag{10}$$

The inductor currents are derived and the following relationship is found.

$$i_{L1} = i_{L2} = \left(\frac{1-D_{OP}}{1-2D_{OP}}\right) i_{PN} \tag{11}$$

$$i_{L3} = i_{L4} = \left(\frac{1 - D_{ON}}{1 - 2D_{ON}}\right) i_{NN} \tag{12}$$

Here, i_{L1}, i_{L2}, i_{L3}, and i_{L4} are instantaneous inductor currents. Also, i_{PN} and i_{NN} are instantaneous DC-link output currents during NST states.

4. Design parameters for the proposed topology

The important design parameters of inductors and capacitors for the proposed topology are the inductor current ripple $(k_L(\%))$ and capacitor voltage ripple $(k_C(\%))$, given as follows:

$$k_C(\%) = \frac{\Delta v_C}{V_C} * 100 \tag{13}$$

$$k_L(\%) = \frac{\Delta i_L}{I_L} * 100 \tag{14}$$

Moreover, the inductance and capacitance values have been derived and calculated for the proposed QZS-NPCI topology using the following equations.

$$L_{1,2,3,4} = \left[\frac{D\,(1-D)}{(1-2D)}\right] * \left[\frac{V_{in(+)}}{k_L f_s \overline{i_{in(+)}}}\right] \tag{15}$$

$$C_{1,3} = (1-2D) * \left[\frac{\overline{i_{in(+)}}}{k_C f_s V_{in(+)}}\right] \tag{16}$$

$$C_{2,4} = \left[\frac{D\,(1-2D)}{(1-D)}\right] * \left[\frac{\overline{i_{in(+)}}}{k_C f_s V_{in(+)}}\right] \tag{17}$$

5. Simulation

Simulink/MATLAB has been used to simulate the developed system. Furthermore, PSIM software was used to develope the proposed topology along with the control strategy to validate the MATLAB simulation results. The developed system comprises a control strategy and restructured QZS-ANPCI topology, as mentioned in Section 3. Table 3 shows the parameter values to implement in simulation as well as in the hardware prototype model. Each model physically has a 3-phase Y-connected load through the low-pass filter. The proposed system delivers the rated power to loads as a stand-alone system. Therefore, it is essential to regulate the AC output voltage and DC-link voltage across the inverter bridge.

The waveforms in the case of steady-state and dynamic response are the simulated results as shown in Figure 4. These waveforms have 3 categories: (1) symmetrical boost operation (steady state), (2) unsymmetrical boost operation (steady state), and (3) impact of input DC voltages and output load variations (dynamic response).

Figure 4a illustrates the upper side ST switching signal (V_G), input voltage $(V_{in(+)})$, and capacitor voltages (V_{C1}, V_{C2}). Similarly, Figure 4b shows lower side switching signal (V_G), input voltage $(V_{in(-)})$, and

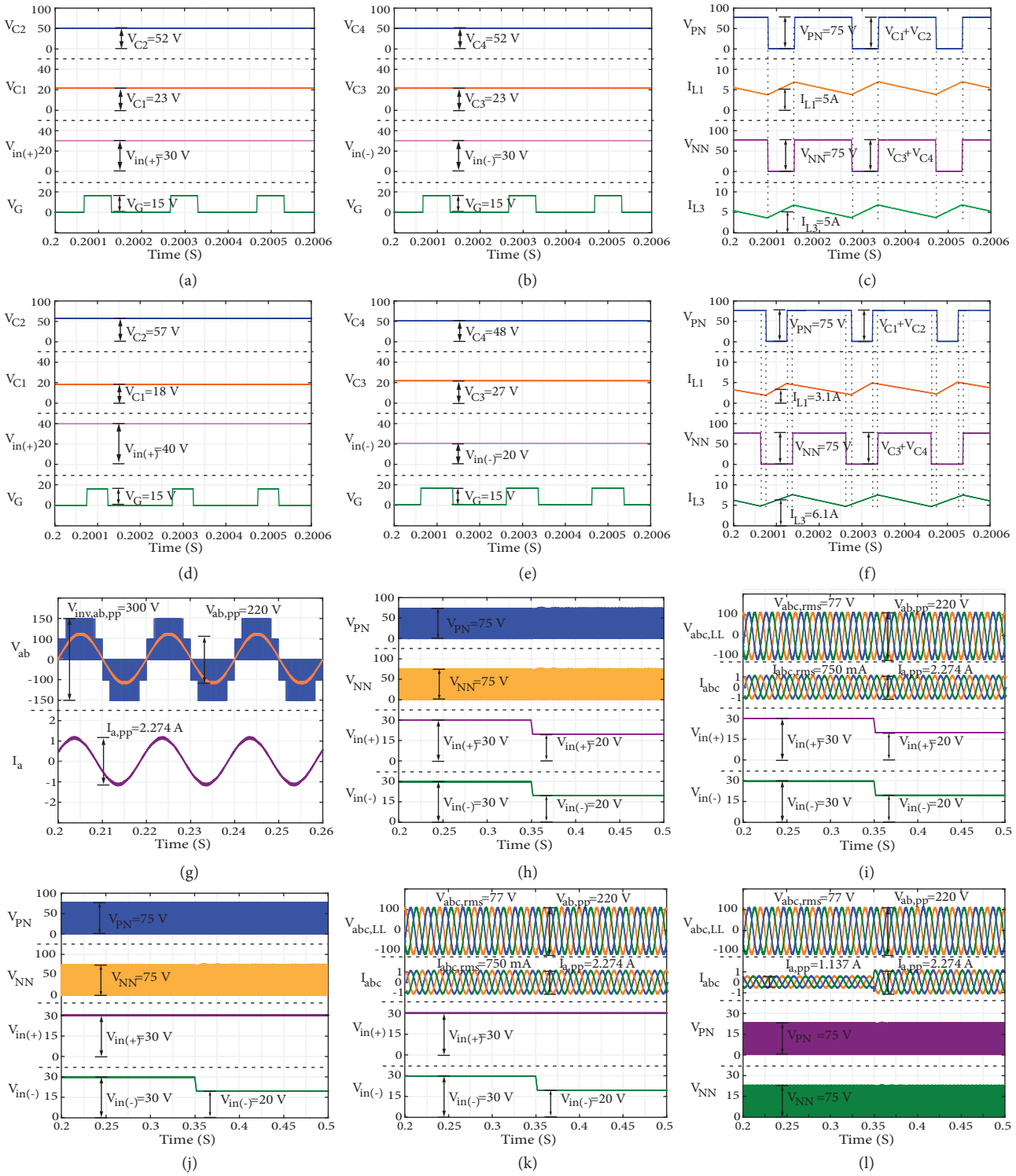


Figure 4. (a) $V_{GE_{UST}}, V_{in(+)}, V_{C1}, V_{C2}$; (b) $V_{GE_{LST}}, V_{in(-)}, V_{C3}, V_{C4}$; (c) $I_{L3}, V_{NN}, I_{L1}, V_{PN}$ in symmetrical boost mode; (d) $V_{GE_{UST}}, V_{in(+)}, V_{C1}, V_{C2}$; (e) $V_{GE_{LST}}, V_{in(-)}, V_{C3}, V_{C4}$; (f) $I_{L3}, V_{NN}, I_{L1}, V_{PN}$ in unsymmetrical boost mode; (g) $Ia, V_{ab}, V_{inv,ab}$ at $R_L = 60\Omega$ in both modes; (h) $V_{in(+)}, V_{in(-)}, V_{NN}, V_{PN}$; (i) $V_{abc}, I_{abc}, V_{in(+)}, V_{in(-)}$ for change of $V_{in(+)} = V_{in(-)} = 30V$ to $20V$; (j) $V_{in(+)}, V_{in(-)}, V_{NN}, V_{PN}$; (k) $V_{abc}, I_{abc}, V_{in(+)}, V_{in(-)}$ for change of $V_{in(+)} = 30V$ to $20V$; (l) $V_{abc}, I_{abc}, V_{PN}, V_{NN}$ for dynamic change of $R_L = 120\Omega$ to 60Ω.

Table 3. Parameter values used in simulation and experimentation setup.

Sr. no.	Parameters	Values
1	Input DC voltage range, $V_{in} = V_{in(+)} + V_{in(-)}$	20 to 150V
2	Desired DC-link voltages, $V_{PN} = V_{NN}$	75 V
3	Desired DC-link voltage across inverter bridge, $V_{0,NPC}$	150 V
4	Rated AC output voltages (V_{ab}, V_{bc}, V_{ca})	74 V (RMS)
5	Inductance, L_1, L_2, L_3, L_4	500 μ H
6	Capacitance, C_1, C_2, C_3, C_4	500 μ F
7	Output filter inductor, L_f	10 mH
8	Output filter inductor, C_f	2 μ F
9	Inverter switching frequency, F_{sw}	5 kHz
10	Y-connected 3-phase load	10 Ω, 60 Ω, 120 Ω
11	Proportional gain constant, K_p	10
12	Integral gain constant, K_i	1500

capacitor voltages (V_{C3}, V_{C4}). Furthermore, Figure 4c provides captured waveforms for inductor currents (I_{L1}, I_{L3}) and DC-link voltages (V_{PN}, V_{NN}). The ST states for duty ratio (D_{OP}, D_{ON}), input voltages, capacitor voltages, and inductor currents on both sides provide symmetrical boost operation at $V_{in(+)}$=$V_{in(-)}$=30 V.

Since input DC voltages, especially those of RERs, do not remain equal, we set 40 V and 20 V for $V_{in(+)}$ and $V_{in(-)}$ to observe the system behavior, respectively. Figures 4d–4f illustrate unsymmetrical boost operation. The ST states (D_{OP}, D_{ON}), input voltages, capacitor voltages, and inductor currents on both positive and negative sides have discrete values.

Thereafter, Figure 4g demonstrates fixed load voltage Vab and load current Ia under both boost mode operations at resistive load, $R = 60\ \Omega$.

Finally, dynamic change of either input voltages or load ensures the effectiveness of DC-side and AC-side loop controllers. At t = 0.3s, both input voltages symmetrically change their values from 30 V to 20 V, as shown in Figures 4h and 4i. Figures 4j and 4k provide the unsymmetrical change of one input voltage from 30 V to 20 V at t = 0.3s. In both cases, DC-side feedback control maintains constant DC-link voltages. Consequently, the proposed system provides rated RMS output voltages. Similarly, Figure 4l illustrates that load, changed from $R = 120\ \Omega$ to $R = 60\ \Omega$, does not affect output voltages or DC-link voltages due to AC-side feedback control.

In these cases, the control parameters (DC-link voltages, AC voltages) maintain their constant values under step change of either input voltages or load. This shows that the response of the control system is fast and has negligible impact on control parameters due to the control strategy.

6. Harmonic analysis

In order to evaluate the harmonic contents in the waveforms (current and voltage), we can present these electrical signals as Fourier series expressions as follows:

$$F(t) = \frac{a_0}{2} + \sum_{h=1}^{\infty} [a_h cos(h\omega t) + b_h sin(h\omega t)] \tag{18}$$

Here,

$$\begin{aligned} a_0 &= \frac{2}{T}\int_0^T f(t)dt \\ a_h &= \frac{2}{T}\int_0^T f(t)cos(h\omega t)dt \\ b_h &= \frac{2}{T}\int_0^T f(t)sin(h\omega t)dt \end{aligned}$$

This expression of Fourier series can be written as:

$$F(t) = \sum_{h=0}^{\infty} c_h cos(h\omega t + \theta_h) \tag{19}$$

Here,

$$\begin{aligned} c_0 &= 0 \; at \; \theta_0 = 0 \; (dc \; component) \\ c_h &= \sqrt{a_h + b_h} \\ \theta_h &= tan^{-1}\left(\frac{b_h}{a_h}\right) \end{aligned}$$

The term in Eq. (19) is known as the harmonics of $F(t)$. The fast Fourier transform (FFT) of any waveform is the composition of impulses having frequency ω=h ω_0 at h = 0, $\pm1, \pm2$,.... whereas the THDs of voltage and current are given by following equations:

$$V_{THD} = \frac{\sqrt{\sum_{h=2}^{\infty} V_h^2}}{V_1} \tag{20}$$

Here, V_1 is the fundamental voltage component and V_h is the voltage harmonic component.

$$I_{THD} = \frac{\sqrt{\sum_{h=2}^{\infty} I_h^2}}{I_1} \tag{21}$$

Here, I_1 is the fundamental current component and I_h is the current harmonic component.

To analyze the harmonic contents in the proposed topology, Table 4 and Figure 5 show THDs of output voltages and currents under the proposed symmetrical/unsymmetrical modulation technique. These show that the THDs are within the acceptable range in symmetrical and unsymmetrical modes, illustrated in Figures 5a and 5b. Moreover, the THD and modulation index (M) have an inverse relation between them. If input voltage reaches the verge of the low input voltage range ($Vin(+) = Vin(-) = 20\ V$, $V_{o,NPC} = 150\ V$, $B = 3.75$), then the THDs of the voltages are slightly increased whether the proposed topology is operating under symmetrical or unsymmetrical boost mode.

To show the impact of modulation index (M) on THDs of voltage and current, a different small-sized low-pass filter (L_f = 1 mH, C_f = 22 μ F) is also used at the output of the proposed topology. Table 5 shows that THD of the voltage (V_{ab}) increases with decrease of modulation index (M) before and after the LC-filter. Similarly, the THD of the corresponding current (I_a) also increases with decrease of modulation

Table 4. THD of voltages and currents in the proposed 3-level QZS-ANPCI at load, $R = 60\ \Omega$ / phase (Y-connected).

Sr. no.	Terms	Values (RMS)	Proposed QZS-ANPCI (3-level)												Remarks/ IEEE criteria
			Symmetrical boost modulation						Asymmetrical boost modulation						
			Duty ratio (D_0)		$V_{in(+)}$ (v)	$V_{in(-)}$ (v)	THD (%)		Duty ratio (D_0)		$V_{in(+)}$ (v)	$V_{in(-)}$ (v)	THD (%)		
			D_{0P}	D_{0N}			Before LC filter	After LC filter	D_{0P}	D_{0N}			Before LC filter	After LC filter	
1.	V_{ab}, V_{bc}, V_{ca}	74V	0.3	0.3	30	30	75.66%	3.21%	0.1	0.3	60	30	75.8%	3.20%	Theoretical
	I_a, I_b, I_c	0.75A					13.13%	3.21%					13.13%	3.20%	(I_{THD}<5%)
2.	V_{ab}, V_{bc}, V_{ca}	72V	0.3	0.3	30	30	82.00%	4.01%	0.1	0.3	60	30	82.19%	3.99%	Practical
	I_a, I_b, I_c	0.86A					18.25%	3.51%					18.33%	3.43%	(I_{THD}<5%)

index (M). This shows that the output filter always becomes a necessary requirement whenever low THDs are required for improvement of power quality, irrespective of which modulation technique is used. The proposed LC-filter ($L_f = 10$ mH, $C_f = 2\ \mu$ F) has the same impact on modulation index (M) as a small-sized LC-filter. However, the proposed LC-filter has the lowest THDs of current (THD_I=3.9% & THD_I=1%) and voltage (THD_V=27% & THD_V=1%) at maximum modulation index (M=1.15) before and after the LC-filter. It is found that the proposed output filter has a significant reduction in THD of the current before and after the LC-filter as compared to the small-sized output filter.

Table 5. Relationship of modulation index (M) with THDs of voltage and current using small sized LC-filter ($L_f = 1$ mH, $C_f = 22\ \mu$ F).

Sr. no.	Input voltage (V) $V_{in(+)}, V_{in(-)}$	Voltage boost factor (B)	DC-link voltage (V)	Modulation index (M)	THDs (%)		THDs (%)	
					Before LC filter		After LC filter	
					V_{ab}	I_a	V_{ab}	I_a
1.	$V_{in(+)}$=75 V $V_{in(-)}$=75 V	B=1	$V_{0,NPC}$=150 V	M=1.15	27%	38%	1.4%	1.4%
2.	$V_{in(+)}$=60 V $V_{in(-)}$=60 V	B=1.25	$V_{0,NPC}$=150 V	M=1.03	46%	44%	3%	3%
3.	$V_{in(+)}$=50 V $V_{in(-)}$=50 V	B=1.5	$V_{0,NPC}$=150 V	M=0.96	51%	49%	4.8%	4.8%
4.	$V_{in(+)}$=40 V $V_{in(-)}$=40 V	B=1.88	$V_{0,NPC}$=150 V	M=0.89	61%	59%	6.5%	6.5%
5.	$V_{in(+)}$=30 V $V_{in(-)}$=30 V	B=2.5	$V_{0,NPC}$=150 V	M=0.8	72%	65.3%	8.2%	8.2%

7. Experimental results and discussion

A prototype setup of the proposed QZS-ANPCI, built in the research lab, has supported the theoretical formulation and simulation. Figure 6 illustrates the developed prototype hardware setup (1 kW). This prototype

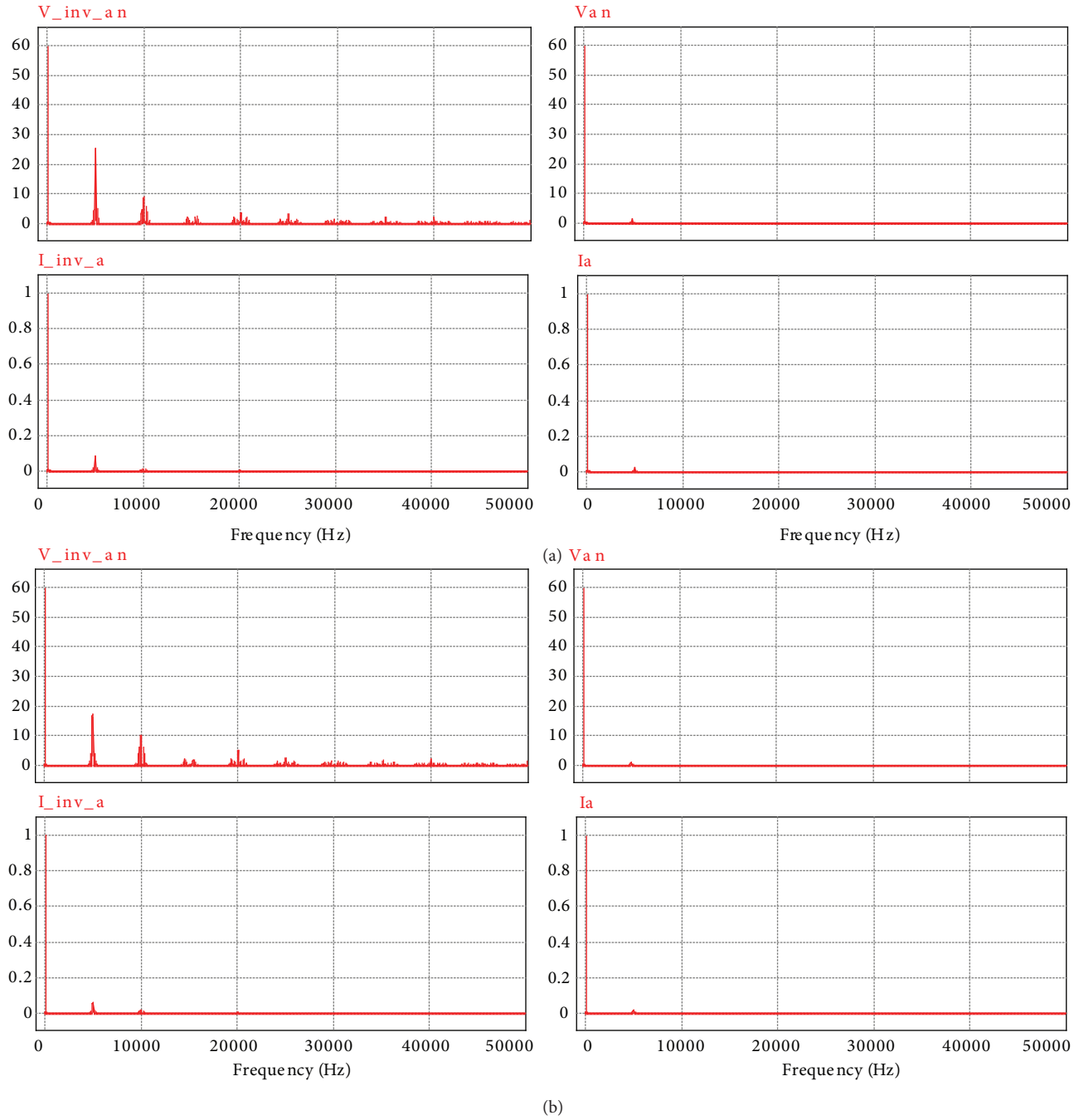


Figure 5. THDs of proposed QZS-ANPCI topology (a) under symmetrical boost mode ($Vin(+) = Vin(-) = 30\ V,\ V_{o,NPC=150V},\ B = 2.5$), (b) under asymmetrical ($Vin(+) = 60V,\ Vin(-) = 30\ V, V_{o,NPC} = 150V, B = 1.67$).

has shown the steady-state and dynamic response results to verify the proposed topology and its control scheme. The experimental prototype setup is also used to validate the proposed modulation.

To implement the digital control scheme, MyRio (NI FPGA, 40 MHz clocking frequency) has been used. For DC-side control loops, capacitor voltages and inductor currents used six ADC channels. The AC output

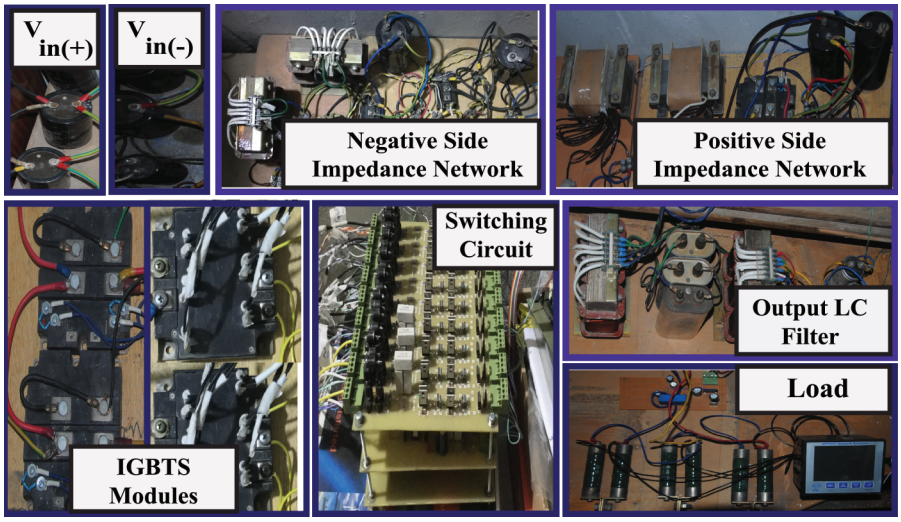


Figure 6. Experimental prototype setup of proposed QZS-ANPCI topology.

voltages (Vab, Vbc) used two ADC channels to create AC-side control. The PI and P regulators were properly tuned using PSIM and MATLAB software.

Figures 7a, 7b, and 7c give the steady-state experimental waveforms operating under symmetrical boost control (at $V_{in(+)} = V_{in(-)} = 30V$). The values of D_{0P} and D_{0N} are automatically set to 0.30 by each DC-side control loop. Eq. (7) also confirms the value of D (at desired $V_{PN} = V_{NN} = 75V$). The modulation index, M, is equal to 0.81 using Eq. (19). Similarly, the equations of capacitor and DC-link voltages provide equal values and those match the practical values. However, there are some voltage drops across nonideal components. The inductor currents I_{L1} and I_{L3} are 5 A, each of which are slightly greater than simulation values.

For unsymmetrical boost control, Figures 7d, 7e, and 7f show practical waveforms (at $V_{in(+)} = 40\ V$, $V_{in(-)} = 20\ V$). Each DC-side control loop automatically generates required values of D_{0P} and D_{0N} to boost input voltages up to 75 V for each (as desired values for $V_{PN}{}^*$ and $V_{NN}{}^*$). The values of D_{0P} and D_{0N} are equal to 0.23 and 0.36, respectively. The derived V_{PN} and V_{NN} expressions also ensure the values of D_{0P} and D_{0N}, respectively (at reference $V_{PN} = V_{NN} = 75V$). The modulation index, M, is 0.74 using the highest ST duty ratio among D_{0P} and D_{0N}. The practical waveforms of capacitors and DC-link voltages match the simulation waveforms. Moreover, the voltage drops across components are negligibly small. Their values are verified from their respective derived expressions. Further, inductor currents, I_{L1} and I_{L3}, are equal to 3.5 A and 6.5 A, respectively. Again, the values of I_{L1} and I_{L3} are slightly more than those of the simulation.

All preceding experimental waveforms confirm that the control parameters (V_{PN} and V_{NN}) maintain the desired values even if both input voltages are lower or distinct in magnitude using the DC-side control system.

On the AC-side, the proposed topology generates line-line voltage of 148 V (peak) and 72 V (RMS) before and after the output filter, as depicted in Figure 7g. The AC voltages are evidently less than simulated AC voltages.

Figures 7h and 7i show the captured DC waveforms when both inputs dynamically step-change magnitudes from 30 V to 20 V. Similarly, Figures 7j and 7k provide AC waveforms when one input dynamically changes magnitude from 30 V to 20 V. These dynamic results confirm that AC and DC side control parameters maintain their voltages level. This validates that the proposed control system is efficient and fast, but there

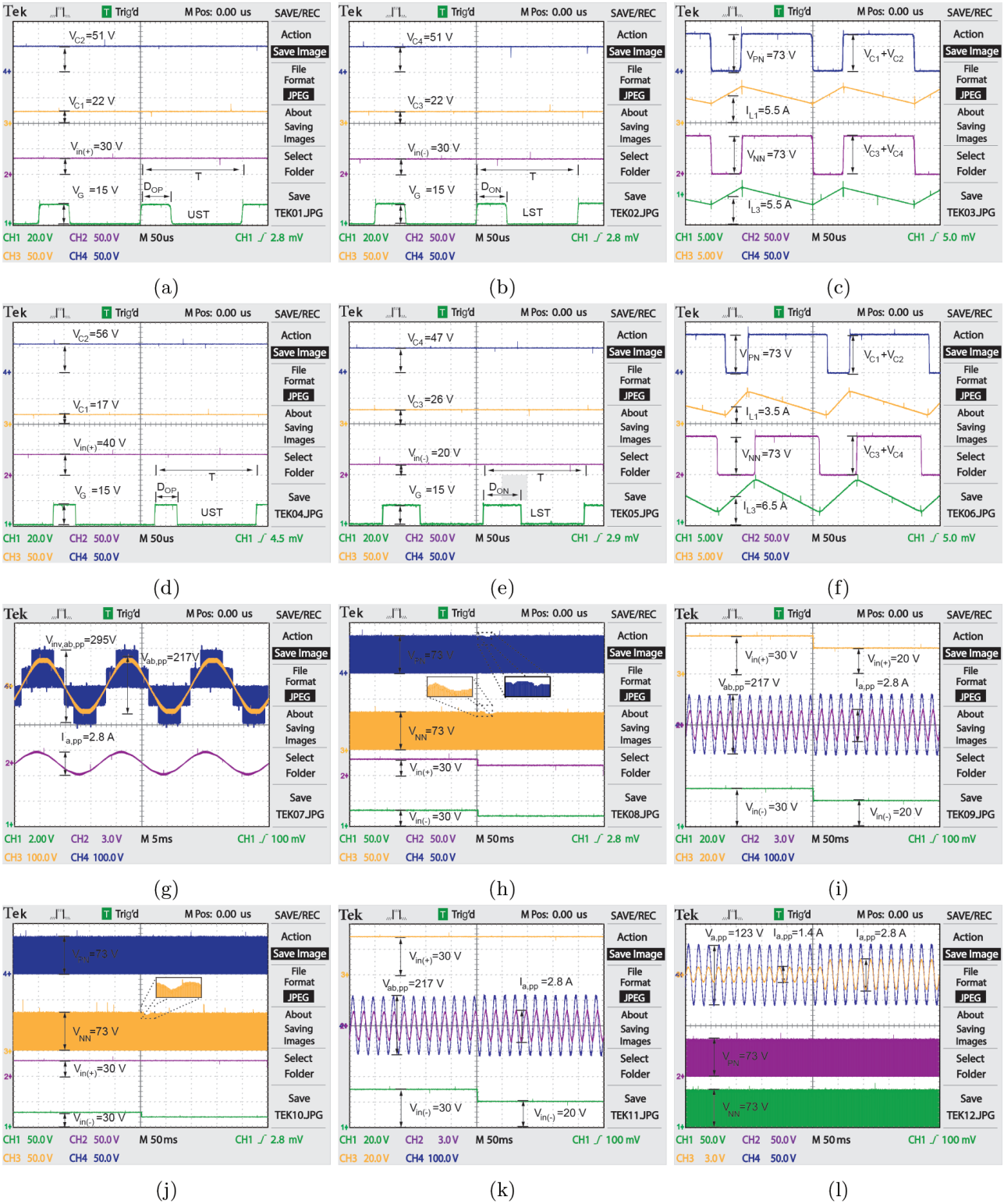


Figure 7. (a) $V_{GE_{UST}}, V_{in(+)}, V_{C1}, V_{C2}$; (b) $V_{GE_{LST}}, V_{in(-)}, V_{C3}, V_{C4}$; (c) $I_{L3}, V_{NN}, I_{L1}, V_{PN}$ in symmetrical boost mode; (d) $V_{GE_{UST}}, V_{in(+)}, V_{C1}, V_{C2}$; (e) $V_{GE_{LST}}, V_{in(-)}, V_{C3}, V_{C4}$; (f) $I_{L3}, V_{NN}, I_{L1}, V_{PN}$ in unsymmetrical boost mode; (g) $Ia, V_{ab}, V_{inv,ab}$ at $R_L = 60\Omega$ in both modes; (h) $V_{in(+)}, V_{in(-)}, V_{NN}, V_{PN}$; (i) $V_{abc}, I_{abc}, V_{in(+)}, V_{in(-)}$ for change of $V_{in(+)} = V_{in(-)} = 30V$ to $20V$; (j) $V_{in(+)}, V_{in(-)}, V_{NN}, V_{PN}$; (k) $V_{abc}, I_{abc}, V_{in(+)}, V_{in(-)}$ for change of $V_{in(+)} = 30V$ to $20V$; (l) $V_{abc}, I_{abc}, V_{PN}, V_{NN}$ for dynamic change of $R_L = 120\Omega$ to 60Ω.

is very little influence on control variables. From a practical point of view, the proposed system is robust and suitable for the application of low voltage RERs.

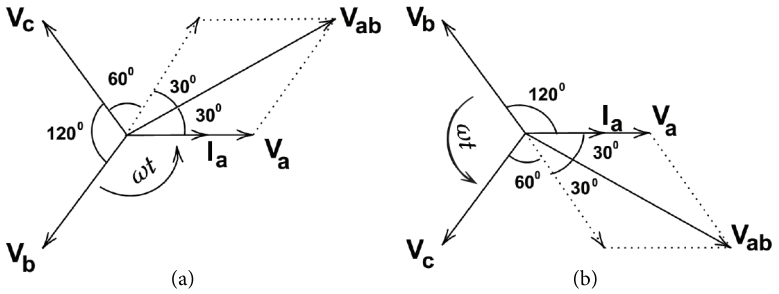


Figure 8. (a) Positive sequence voltages (abc sequence); (b) negative sequence voltages (acb sequence).

Finally, the impact of the sequence of reference voltages (positive or negative) must be discussed.

(1) If reference signals have abc sequence or positive sequence ($V_a = V_M\underline{0°}$, $V_b = V_M\underline{-120°}$, $V_c = V_M\underline{-240°}$), then filtered phase output voltage (V_a) lags phase-phase output voltage (V_{ab}) by 30 degrees as shown in Figure 8a. As the output phase voltage (V_a) and phase current I_a are in the same direction for resistive load ($Z_L = R_L$), therefore I_a lags V_{ab} by 30 degrees as shown by previous AC outputs.

(2) Similarly, if the reference signals have acb sequence or negative sequence ($V_a = V_M\underline{0°}$, $V_b = V_M\underline{120°}$, $V_c = V_M\underline{240°}$), then the filtered phase output voltage (V_a) leads phase-phase output voltage (V_{ab}) by 30 degrees as shown in Figure 8b. In other words, I_a leads V_{ab} by 30 degrees as shown in Figures 9a and 9b.

In both cases, the phase displacement between V_a and I_a is zero and the corresponding power factor (PF) is unity. Moreover, the measured power factor between phase voltage (V_a) and phase current I_a is near unity (about 0.98).

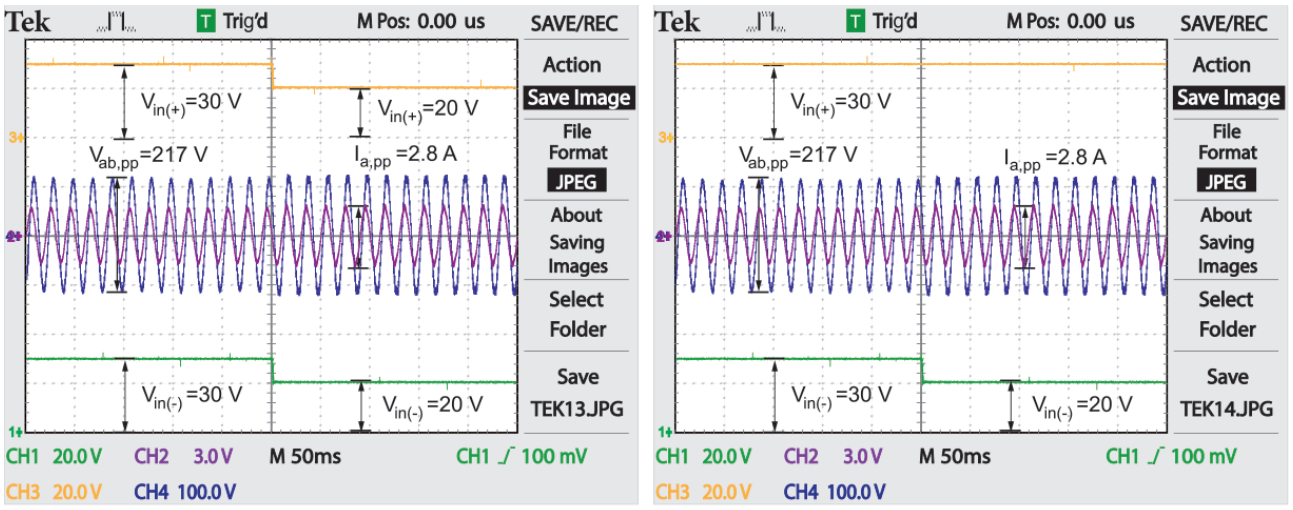
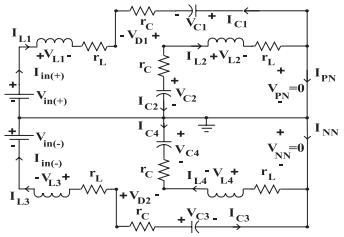
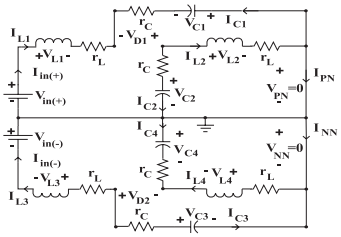


Figure 9. (a) $V_{ab}, I_a, V_{in(+)}, V_{in(-)}$ for change of $V_{in(+)} = V_{in(-)} = 30V$ to $20V$; (b) $V_{ab}, I_a, V_{in(+)}, V_{in(-)}$ for change of $V_{in(+)} = 30V$ to $20V$.

8. Power loss analysis and comparison of efficiency

In this section, we evaluate the power losses and efficiency of the impedance-based QZS-ANPCI topology for both the traditional symmetrical and proposed symmetrical/asymmetrical boost control schemes. The real model of the switching device (IGBTS/MOSFETs) is composed of an internal equivalent drain-to-source resistance (r_{DS}) and its forward voltage drop (V_{FS}), as shown in Table 6. The same table shows the ideal diode connected in series with its parasitic resistance r_D and forward voltage drop V_F. Similarly, the equivalent series resistances (ESRs) of the passive capacitor (r_C) and inductor (r_L) in series with their ideal lossless components present both passive capacitor and inductor components respectively [29–32]. The list of experimental equipment and devices is given in Table 7. The parameters of equipment, used for efficiency and loss calculation, are found from the manufacturer data sheets.

Table 6. Equivalent thermal model of proposed topology for loss and efficiency analysis.

<table>
<tr><td>Symmetrical/unsymmetrical ST state</td><td>Symmetrical/unsymmetrical NST state</td></tr>
<tr><td>  </td><td>  </td></tr>
<tr><td>$P_{11,UST} = 2D_{OP}^2 r_L i_{L1}^2 + 2D_{OP}^2 r_C i_{L1}^2$
$P_{12,LST} = 2D_{ON}^2 r_L i_{L3}^2 + 2D_{ON}^2 r_C i_{L3}^2$</td><td>$P_{21,\ UNST} = 2\left(1-D_{OP}\right)^2 r_L i_{L1}^2 + 2\left(1-D_{OP}\right)^2 r_C (i_{L1}-i_{PN})^2 + \left(1-D_{OP}\right) V_F (2i_{L1}-i_{PN})$
$P_{22,\ LNST} = 2\left(1-D_{ON}\right)^2 r_L i_{L3}^2 + 2\left(1-D_{ON}\right)^2 r_C (i_{L3}-i_{NN})^2 + \left(1-D_{ON}\right) V_F (2i_{L3}-i_{NN})$</td></tr>
<tr><td colspan="2">$A_{11} = \frac{2r_L\left[D_{OP}^2+(1-D_{OP})^2\right](1-D_{OP})^3}{R_L(1-2D_{OP})^2}$ $B_{12} = \frac{4r_C D_{OP}^2(1-D_{OP})^3}{R_L(1-2D_{OP})^2}$
$C_{13} = \frac{r_D(1-D_{OP})^3}{R_L(1-2D_{OP})^2} + \frac{(1-D_{OP})V_F}{V_{in(+)}}$</td></tr>
<tr><td colspan="2">$A_{21} = \frac{2r_L\left[D_{ON}^2+(1-D_{ON})^2\right](1-D_{ON})^3}{R_L(1-2D_{ON})^2}$ $B_{22} = \frac{4r_C D_{ON}^2(1-D_{ON})^3}{R_L(1-2D_{ON})^2}$
$C_{23} = \frac{r_D(1-D_{ON})^3}{R_L(1-2D_{ON})^2} + \frac{(1-D_{ON})V_F}{V_{in(-)}}$</td></tr>
<tr><td colspan="2">Normalized Efficiency=$\eta_{Proposed\ QZS-NPCI} = \frac{\left[\left(\frac{V_{PN}I_{PN}}{P_{11}+P_{21}+V_{PN}I_{PN}}\right)+\left(\frac{V_{NN}I_{NN}}{P_{12}+P_{22}+V_{NN}I_{NN}}\right)\right]}{2} * 100$
Normalized Efficiency=$\eta_{Proposed\ QZS-NPCI} = \frac{\left[\left(\frac{1}{A_{11}+B_{12}+B_{13}+1}\right)+\left(\frac{1}{A_{21}+B_{22}+B_{23}+1}\right)\right]}{2} * 100$</td></tr>
</table>

8.1. Power loss for dual impedance source network

The power conduction loss due to the upper impedance source network in the proposed topology for the NST time period is given as:

$$\begin{aligned} P_{loss,UNST} =& 2\left(1-D_{OP}\right)^2 r_L i_{L1}^2 + 2\left(1-D_{OP}\right)^2 r_C (i_{L1}-i_{PN})^2 + \\ & \left(1-D_{OP}\right)^2 r_D (2i_{L1}-i_{PN})^2 + \left(1-D_{OP}\right) V_F (2i_{L1}-i_{PN}) \end{aligned} \tag{22}$$

Table 7. List of experimental equipment and devices used for efficiency and loss analysis.

Sr. no.	Description of equipment/devices	Parameter from manufacturer data sheet
1.	MITSUBISHI IGBT MODULES CM75TU-12F	$t_{on} = 100ns$ $t_{off} = 300ns$ $r_{DS} = 28m\Omega$
2.	IXYS Fast Recovery Diode DSEP2x61-06A	$V_F = 1.3V$ $r_D = 4.3m\Omega$
3.	Inductors	$20A, 1000uH, r_L = 30m\Omega$
4.	Capacitors (SMH SERIES) ESMH251VSN102MR50T	$300VDC, 1000\ uF$ $ESR = 0.166\Omega$
5.	MOSFETs IRF450 (IGBT driver circuit)	$13A, 500\ V$ $r_D = 0.400Ohm$

Due to the symmetry of upper half and lower half impedance sources, the power loss of the lower lower half impedance source network is equal to the upper half impedance source network for the LNST state as described by the following equation:

$$\begin{aligned} P_{loss,LNST} =& 2\left(1-D_{ON}\right)^2 r_L i_{L3}^2 + 2\left(1-D_{ON}\right)^2 r_C (i_{L3}-i_{PN})^2 + \\ & \left(1-D_{ON}\right)^2 r_D (2i_{L3}-i_{PN})^2 + \left(1-D_{ON}\right) V_F (2i_{L3}-i_{PN}) \end{aligned} \tag{23}$$

The power loss of the upper half impedance network is evaluated during the UST state as given by the following equation:

$$P_{loss,UST} = 2D_{OP}^2 r_L i_{L1}^2 + 2D_{OP}^2 r_C i_{L1}^2 \tag{24}$$

In the same way, the power loss of the lower half impedance source network is equal to the upper half impedance source network for the LST state as described by the following equation:

$$P_{loss,LST} = 2D_{ON}^2 r_L i_{L3}^2 + 2D_{ON}^2 r_C i_{L3}^2 \tag{25}$$

The total power conduction loss for dual quasi-Z-source impedance of the proposed topology is:

$$P_{loss,Z} = P_{loss,UNST} + P_{loss,LNST} + P_{loss,UST} + P_{loss,LST} \tag{26}$$

8.1.1. Power loss for inverter bridge module

The power conduction loss of the inverter bridge module can be calculated for the ST state as:

$$P_{IGBT,\ cond\ loss}^{1} = \frac{1}{2\pi}\int_0^{\pi} V_{conv}(t) i(t) D_{active}(t) d\omega t = \frac{I_m V_{DS} M cos(\theta)}{4} + \frac{I_m^2 r_{DS} M}{2\pi}\left(1 + \frac{cos(2\theta)}{3}\right) \tag{27}$$

Here,

$$i(t) = I_m sin(\omega t + \theta)$$

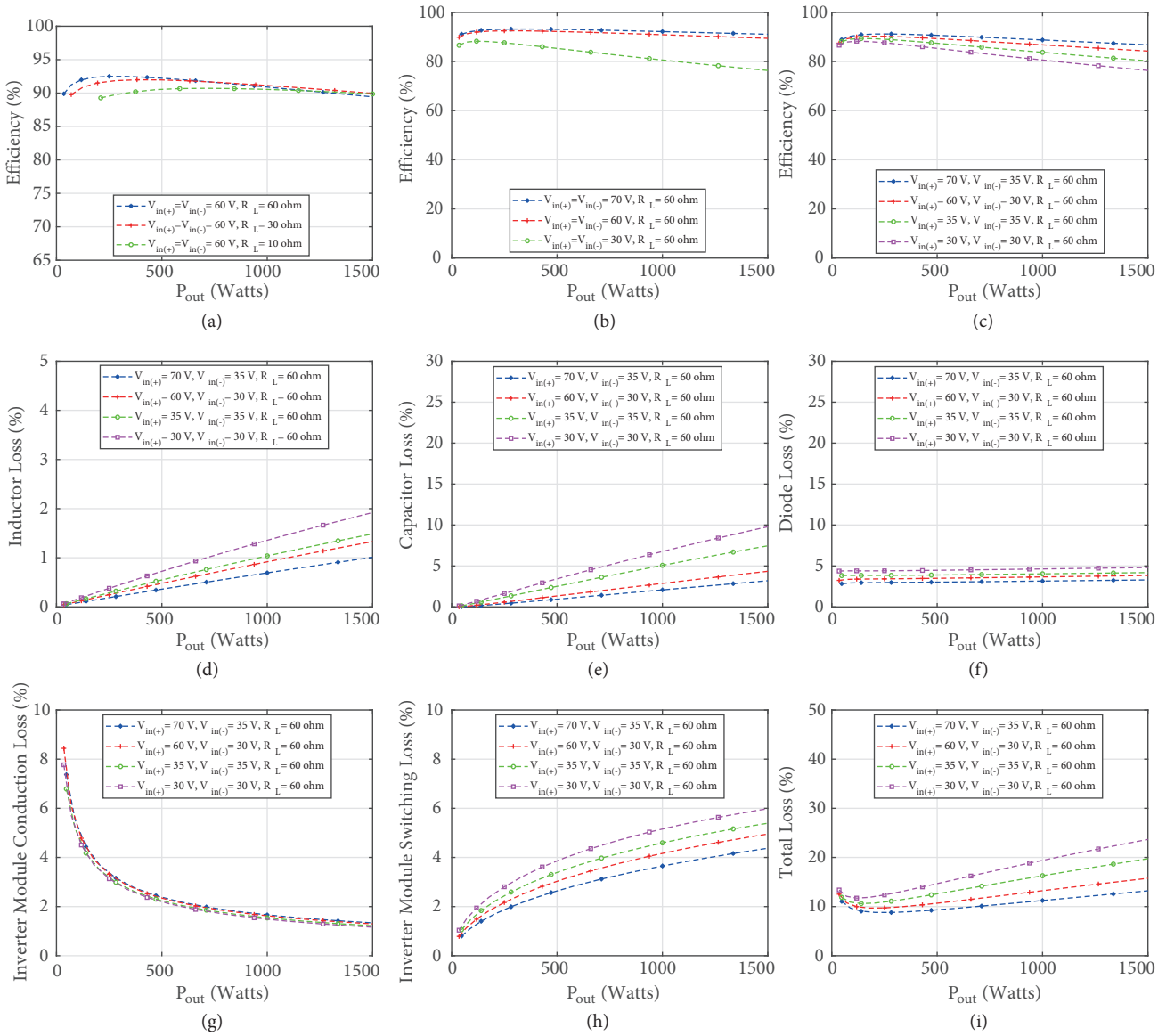


Figure 10. Efficiency at various output powers under symmetrical and unsymmetrical boost control techniques: (a) effect of change of load resistor (R_L); (b) effect of symmetrical change of input voltages ($V_{in(+)} = V_{in(-)}$); (c) effect of symmetrical and unsymmetrical change of input voltages; (d) inductor loss; (e) capacitor loss; (f) diode loss; (g) inverter module conduction loss; (h) inverter module switching loss; (g) total loss.

$$D_{active}(t) = Msin(\omega t)$$
$$V_{conv}(t) = V_{DS} + i(t)r_{DS}$$

Similarly, power conduction loss of the inverter module due to the ST state is given by the following expression:

$$P^{\,2}_{IGBT,\ cond\ loss} = \left[D_{OP}V_F\frac{2i_L}{3} + D_{ON}V_F\frac{2i_L}{3}\right] + \left[D^2_{OP}r_{DS}(\frac{2i_L}{3})^2 + D^2_{ON}r_{DS}(\frac{2i_L}{3})^2\right] \quad (28)$$

The switching losses of active switches in the converter are due to turn-on and turn-off states.

$$P_{IGBT,\ sw\ loss}^{\ on} = \frac{1}{T_s}\int_0^{t_{on}} V_{IGBT}(t)i(t)dt = \frac{1}{12}\ [V_{PN}\ I_{L1} + V_{NN}\ I_{L3}]\, f_s t_{on} \tag{29}$$

$$P_{IGBT,\ sw\ loss}^{\ off} = \frac{1}{T_s}\int_0^{t_{off}} V_{IGBT}(t)i(t)dt = \frac{1}{12}\ [V_{PN}\ I_{L1} + V_{NN}\ I_{L3}]\, f_s t_{off} \tag{30}$$

8.1.2. Total power loss for proposed topology

The total loss for the proposed structure of the QZS-NPCI occurs due to conduction and switching loss, expressed as follows:

$$P_{total,\ loss} = P_{cond\ loss} + P_{sw\ loss} \tag{31}$$

8.1.3. Overall efficiency for proposed topology

Finally, the efficiency for the proposed QZS-NPCI topology can be calculated using the following empirical formula:

$$Efficiency(\eta) = \frac{P_{out}}{P_{out} + P_{loss}} * 100 \tag{32}$$

The efficiency and loss of the proposed QZS-NPCI topology have been evaluated under the traditional and proposed control schemes as shown in Figure 10. The efficiency of the proposed topology has been analyzed under variation of load (R_L), depicted by Figure 10a. It shows that efficiency decreases with increase of the output load. The proposed structure has higher efficiency at high input voltage than that at low input voltage, as illustrated in Figure 10b. Similarly, if two input voltage sources undergo a low voltage situation (unsymmetrically) as depicted by Figure 10c, then one of the input sources remains unaffected. This gives higher input voltage magnitude than that of the proposed topology with single input source variation. Consequently, the efficiency of the proposed structure is higher with two independent sources than that of single source-based proposed structure. Moreover, the unsymmetrical boost control $(V_{in(+)} = 60\ V, V_{in(-)} = 30\ V)$ provides higher efficiency than symmetrical boost control $(V_{in(+)} = 60\ V, V_{in(-)} = 30\ V)$. Furthermore, the variation of losses produced by passive components (inductor, capacitor, diode) and the active switches module in these situations has been derived for detailed loss analysis, as illustrated in Figure 10d through Figure 10h, respectively. The total losses by all components in the proposed topology are summarized under different input voltages in Figure 10i.

9. Conclusion

This paper has presented a proposed buck/boost QZS-ANPCI topology to integrate independent RERs whose voltages are equal or unequal. The proposed modulation (symmetrical/unsymmetrical boost modulation) is compared with conventional FST (symmetrical boost modulation) to evaluate its advantages. The proposed modulation has mitigated the unbalanced input voltages problem in an ANPC inverter. A control strategy has been proposed to make this topology more efficient for different types of RERs. The efficiency and loss analyses

show that the proposed topology has about 92% efficiency at $V_{in(+)} = V_{in(-)} = 70\ V$. Moreover, DC and AC side control loops with PI and P regulators are integrated with the topology so that input voltages of RERs or load variation should not distort the rated DC and AC side control parameters. Furthermore, the THDs of AC currents are evaluated and are within the limits as specified by IEEE Standard-519. The simulation results and experimental setup have satisfactory agreement to prove the proposed system and theoretical postulates. In the future, the buck/boost topology, integrated with the NPC inverter (with 4 legs), can also be developed to mitigate the unbalanced load and neutral point voltage shifting problem.

Acknowledgments/Author Contributions

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References

[1] de Matos JG, e Silva FS, Ribeiro LA. Power control in ac isolated microgrids with renewable energy sources and energy storage systems. IEEE Transactions on Industrial Electronics 2015; 62 (6): 3490-8. doi: 10.1109/TIE.2014.2367463

[2] Peng FZ. Z-source inverter. IEEE Transactions on Industry Applications 2003; 39 (2): 504-10. doi: 10.1109/TIA.2003.808920

[3] Gao F, Loh PC, Blaabjerg F, Gajanayake CJ. Operational analysis and comparative evaluation of embedded Z-source inverters. In: IEEE 2008 Power Electronics Specialists Conference; Rhodes, Greece; 2008. pp. 2757-2763. doi: 10.1109/PESC.2008.4592362

[4] Anderson J, Peng FZ. Four quasi-Z-source inverters. In: IEEE 2008 Power Electronics Specialists Conference; Rhodes, Greece; 2008. pp. 2743-2749. doi: 10.1109/PESC.2008.4592360

[5] Ellabban O, Van Mierlo J, Lataire P. Comparison between different pulse-width-modulation control methods for different Z-source inverter topologies. In: IEEE 2009 13th European Conference on Power Electronics and Applications; Barcelona, Spain; 2009. pp. 1-11.

[6] Siwakoti YP, Peng FZ, Blaabjerg F, Loh PC, Town GE et al. Impedance-source networks for electric power conversion part II: review of control and modulation techniques. IEEE Transactions on Power Electronics 2015; 30 (4): 1887-1906. doi: 10.1109/TPEL.2014.2329859

[7] Choudhury A, Pillay P, Williamson SS. A performance comparison study of space-vector and carrier-based pulse-width-modulation techniques for a 3-level neutral-point-clamped traction inverter drive. In: IEEE 2014 Power Electronics, Drives and Energy Systems Conference; Mumbai, India; 2014. pp. 1-6. doi: 10.1109/PEDES.2014.7041964

[8] Schweizer M, Lizama I, Friedli T, Kolar JW. Comparison of the chip area usage of 2-level and 3-level voltage source converter topologies. In: IECON 2010 - 36th Annual Conference on IEEE Industrial Electronics Society; Glendale, AZ, USA; 2010. pp. 391-396. doi: 10.1109/IECON.2010.5674994

[9] Loh PC, Gao F, Blaabjerg F, Feng SY, Soon KN. Pulsewidth-modulated Z-source neutral-point-clamped inverter. IEEE Transactions on Industry Applications 2007; 43 (5): 1295-308. doi: 10.1109/TIA.2007.904422

[10] Loh PC, Lim SW, Gao F, Blaabjerg F. Three-level Z-source inverters using a single LC-impedance network. IEEE Transactions on Power Electronics 2007; 22 (2): 706-711. doi: 10.1109/TPEL.2007.892433

[11] Loh PC, Gao F, Blaabjerg F, Lim SW. Operational analysis and modulation control of three-level Z-source inverters with enhanced output waveform quality. IEEE Transactions on Power Electronics 2009; 24 (7): 1767-1775. doi: 10.1109/TPEL.2009.2014651

[12] Husev O, Roncero-Clemente C, Romero-Cadaval E, Vinnikov D, Stepenko S. Single phase three-level neutral-point-clamped quasi-Z-source inverter. IET Power Electronics 2014; 8 (1): 1. doi: 10.1049/iet-pel.2013.0904

[13] Shults T, Husev O, Blaabjerg F, Roncero C, Romero-Cadaval E et al. Novel space vector pulse width modulation strategies for single-phase three-level neutral-point-clamped impedance-source inverters. IEEE Transactions on Power Electronics 2019; 34 (5): 4820-4830. doi: 10.1109/TPEL.2018.2859194

[14] Mo W, Loh PC, Blaabjerg F, Wang P. Trans-Z-source and Γ-Z-source neutral-point-clamped inverters. IET Power Electronics 2014; 8 (3): 371-377. doi:10.1049/iet-pel.2014.0725

[15] Yu D, Cheng Q, Gao J, Tan F, Zhang Y. Three-level neutral-point-clamped quasi-Z-source inverter with reduced Z-source capacitor voltage. Electronics Letters 2016; 53 (3): 185-187. doi: 10.1049/el.2016.3930

[16] Sahoo M, Keerthipati S. A three-level LC-switching-based voltage boost neutral-point-clamped inverter. IEEE Transactions on Industrial Electronics 2017; 64 (4): 2876-2883. doi: 10.1109/TIE.2016.2636120

[17] Chen HC, Liao JY. Modified interleaved current sensorless control for three-level boost power factor correction converter with considering voltage imbalance and zero-crossing current distortion. IEEE Transactions on Industrial Electronics 2015; 62 (11): 6896–6904. doi: 10.1109/TIE.2015.2435695

[18] Mahdavikhah B, Prodic A. Low-volume power factor correction rectifier based on nonsymmetric multilevel boost converter. IEEE Transactions on Power Electronics 2015; 30 (3): 1356–1372. doi: 10.1109/TPEL.2014.2317723

[19] Krishna R, Soman DE, Kottayil SK, Leijon M. Pulse delay control for capacitor voltage balancing in a three-level boost neutral point clamped inverter. IET Power Electron 2015; 8 (2): 268–277. doi: 10.1049/iet-pel.2014.0103

[20] Ho AV, Chun TW. Single-phase modified quasi-Z-source cascaded hybrid five-level inverter. IEEE Transactions on Industrial Electronics 2018; 65 (6): 5125-5134. doi: 10.1109/TIE.2017.2779419

[21] Lee SS, Lee KB. Dual-T-type seven-level boost active-neutral-point-clamped inverter. IEEE Transactions on Power Electronics 2019; 34: 6031-6035. doi: 10.1109/TPEL.2019.2891248

[22] Ye Z, Wang T, Mao S, Chen A, Yu D et al. A PWM strategy based on state transition for cascaded H-bridge inverter under unbalanced DC sources. IEEE Journal of Emerging and Selected Topics in Power Electronics (in press). doi: 10.1109/JESTPE.2019.2893936

[23] Xing X, Zhang C, Chen A, He J, Wang W et al. Space-vector-modulated method for boosting and neutral voltage balancing in Z-source three-level T-type inverter. IEEE Transactions on Industry Applications 2016; 52 (2): 1621-1631. doi: 10.1109/TIA.2015.2490142

[24] Park Y, Sul SK, Lim CH, Kim WC, Lee SH. Asymmetric control of DC-link voltages for separate maximum power point trackers in three-level inverters. IEEE Transactions on Power Electronics 2013; 28 (6): 2760-2769. doi: 10.1109/TPEL.2012.2224139

[25] Floricau D, Popescu CL, Popescu MO, Floricau E, Spataru L. A comparison of efficiency for three-level neutral-point-clamped and active-neutral-point-clamped voltage source converters. In: IEEE 2009 Compatibility and Power Electronics Conference; Badajoz, Spain; 2009. pp. 331-336. doi: 10.1109/CPE.2009.5156055

[26] Rodriguez J, Bernet S, Steimer PK, Lizama IE. A survey on neutral-point-clamped inverters. IEEE Transactions on Industrial Electronics 2010; 57 (7): 2219-2230. doi: 10.1109/TIE.2009.2032430

[27] Shinde U, Kottagattu S, Kadwane S, Gawande S. Grid-connected quasi-Z-source inverter with battery. Turkish Journal of Electrical Engineering & Computer Sciences 2018; 26 (4): 1847-1859. doi: 10.3906/elk-1703-123

[28] Liu Y, Ge B, Ferreira FJ, de Almeida AT, Abu-Rub H. Modeling and space-vector pulse-width-modulation control of quasi-Z-source inverter. In: IEEE 2011 11th International Conference on Electrical Power Quality and Utilisation; Lisbon, Portugal; 2011. pp. 1-7. doi: 10.1109/EPQU.2011.6128914

[29] Babaei E, Alilu S, Laali S. A new general topology for cascaded multilevel inverters with reduced number of components based on developed H-bridge. IEEE Transactions on Industrial Electronics 2014; 61 (8): 3932-3939. doi: 10.1109/TIE.2013.2286561

[30] Pan L. LZ-source inverter. IEEE Transactions on Power Electronics 2014; 29 (12): 6534-6543. doi: 10.1109/TPEL.2014.2303978

[31] Barater D, Concari C, Buticchi G, Gurpinar E, De D et al. Performance evaluation of a three-level active-neutral-point-clamped photo-voltaic grid-connected inverter with 650-V SiC devices and optimized pulse-width-modulation. IEEE Transactions on Industry Applications 2016; 52 (3): 2475-2485. doi: 10.1109/TIA.2016.2514344

[32] Guan QX, Li C, Zhang Y, Wang S, Xu DD et al. An extremely high efficient three-level active neutral-point-clamped converter comprising SiC and Si hybrid power stages. IEEE Transactions on Power Electronics 2018; 33 (10): 8341-8352. doi: 10.1109/TPEL.2017.2784821