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Design of a range-segmented CMOS current-mode exponential circuit

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Abstract: A CMOS current-mode exponential circuit is designed by plugging candidate circuits into a Taylor's approximation circuit to make a multiple-segment circuit. The selection of candidate circuits is dependent on a large linearity range in each segment. The proposed range-segmented circuit is different from all segments constructed only by quadratic circuits or only by linear circuits. The proposed circuit was simulated using UMC 0.18 μm CMOS technology. The output linearity of the circuit is 56.7 dB for gain error less than 0.5 dB, and the –3 dB bandwidth of the circuit is between 69 and 150 MHz for input range from –63 to 198 μA.

Key words: Exponential circuit, multiple-segments circuit, current-mode circuit, quadratic circuit

1. Introduction

CMOS current-mode circuits have some advantages, such as high bandwidth, low voltage swing, and low parasitic capacitance effects. Therefore, they can be widely used in circuit design in various fields such as signal generation circuits [1–3], variable gain amplifiers [4, 5], fuzzy function circuits [6], and neural network circuits [7]. These applications are expected to have a wide input range. Exponential circuits were used in the past for the design of variable gain amplifiers [4, 5]. Now, due to the development of machine learning, exponential circuits have more opportunities to be designed as activation functions which require a wide input range and high bandwidth.

In order to have the advantage of a wide input range, CMOS circuits operating in a weak inversion region to improve the input range were designed [2, 3, 8]. However, the bandwidths of these circuits are less than 110 kHz. For high bandwidth, CMOS circuits must operate in saturation, which is a well-known design for its square law, but it cannot achieve higher-order nonlinear circuit design to increase the input range. In [9], the authors used a fourth-order circuit to enlarge the input range, but the circuit became more complex. The authors [10, 11] used four current squaring circuits and several current mirrors to construct a fourth-order circuit with a range of up to 78 dB. In another approach, the authors used the pseudoexponential method, which can construct a fourth-order circuit and have a more compact circuit [12, 13]. Some authors [14] used a pade approximation to make a high-order circuit design. However, these fourth-order circuits and high-order circuits are difficult to achieve accuracy of less than 0.5 dB, except for [11, 13].

Another research trend is to use multisegment circuit design to meet high precision requirements [15]. In [16], the authors used a zero-crossing detector to make two segments for increasing the input range. In [17–19], the authors used piecewise linear to design high-order circuits. This paper is intended to design an exponential circuit for achieving wide input range, high bandwidth, and high accuracy. Therefore, we also use

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multisegment design to improve accuracy and mix linear circuits and quadratic circuits to improve input range and bandwidth. We compare the linearity results of the exponential circuit by plugging a linear circuit and a quadratic circuit, respectively, to determine which one can be selected in each segment design. Consequently, several segments are implemented in succession.

2. Current-mode exponential circuit

2.1. Current-mode linear circuit and quadratic circuit design

For building our circuit design, we need to use a simple linear circuit and a quadratic circuit as candidate circuits in order to be used as plug-in devices in each segment. We use a current mirror as a linear circuit, and use a simple circuit described below as a quadratic circuit.

The drain currents of $M1$ and $M2$ in Figure 1 are derived in [20]:

$$I_1 = KV_0^2(1 - \frac{I_{in}}{4KV_0^2})^2 \tag{1}$$

$$I_2 = KV_0^2(1 + \frac{I_{in}}{4KV_0^2})^2, \tag{2}$$

where $V_0 = \frac{V_{DD}-|V_{tp}|-V_{tn}}{2}$ could be considered a constant voltage, the transconductance parameters K_p and K_n are designed as $K = K_p = K_n$. Assume that $I_0 = KV_0^2$ and $I_{in} = I_0 x$. Eqs. (1) and (2) can be expressed as (3) and (4), respectively.

$$I_1 = I_0(1 - \frac{x}{4})^2 \tag{3}$$

$$I_2 = I_0(1 + \frac{x}{4})^2. \tag{4}$$

Figure 1 shows a quadratic circuit with currents I_1 and I_2.

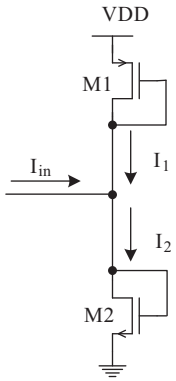

Figure 1. Current-mode quadratic circuit.

2.2. Exponential circuit design

In order to simplify a circuit design, we use a second-order Taylor expansion to approximate an exponential function. By expanding a second-order Taylor expansion at $x = 0$, we have

$$e^x \approx 1 + x + \frac{1}{2}x^2 \tag{5}$$

We can design a current-mode circuit shown in Figure 2 to implement the exponential function using quadratic circuits. In Figure 2, I_{out} will be

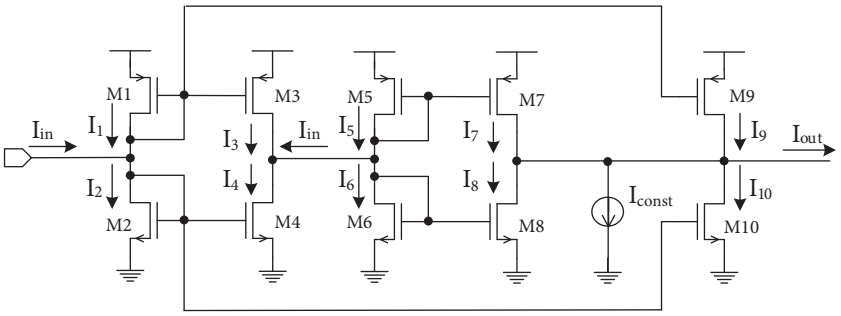

Figure 2. Current-mode exponential circuit of second-order Taylor expansion.

$$I_{out} = I_7 - I_8 + I_9 - I_{10} - I_{const}. \tag{6}$$

If we design $I_7 = 2I_5$, $I_8 = I_6$, $I_9 = \frac{11}{8}I_1$ and $I_{10} = \frac{11}{8}I_2$ using current mirrors, and use a current sink $I_{const} = \frac{7}{8}I_0$, I_{out} becomes

$$I_{out} = 2I_5 - I_6 + \frac{11}{8}(I_1 - I_2) - \frac{7}{8}I_0. \tag{7}$$

By matching M1 to M5 and M2 to M6, we have $I_5 = I_1$ and $I_6 = I_2$, respectively. Consequently,

$$I_{out} = I_2 - 2I_1 - \frac{11}{8}I_0 x - \frac{7}{8}I_0. \tag{8}$$

Based on the quadratic circuit in Figure 1, we substitute (3) and (4) into (8). I_{out} will be

$$I_{out} = \frac{1}{8}I_0(1 + x + \frac{1}{2}x^2). \tag{9}$$

If we set $I_k = \frac{1}{8}I_0$, I_{out} can be approximated from (5) as

$$I_{out} \approx I_k e^{\frac{I_x}{I_0}}. \tag{10}$$

Therefore, Figure 2 is a current-mode exponential circuit. The simulation result of the Taylor's approximation circuit using UMC 0.18 μm CMOS technology is shown in Figure 3. We observe that the input range is from –39 to 21 μA for gain error less than 0.5 dB. However, the linearity is only 13.03 dB as shown in Figure 4.

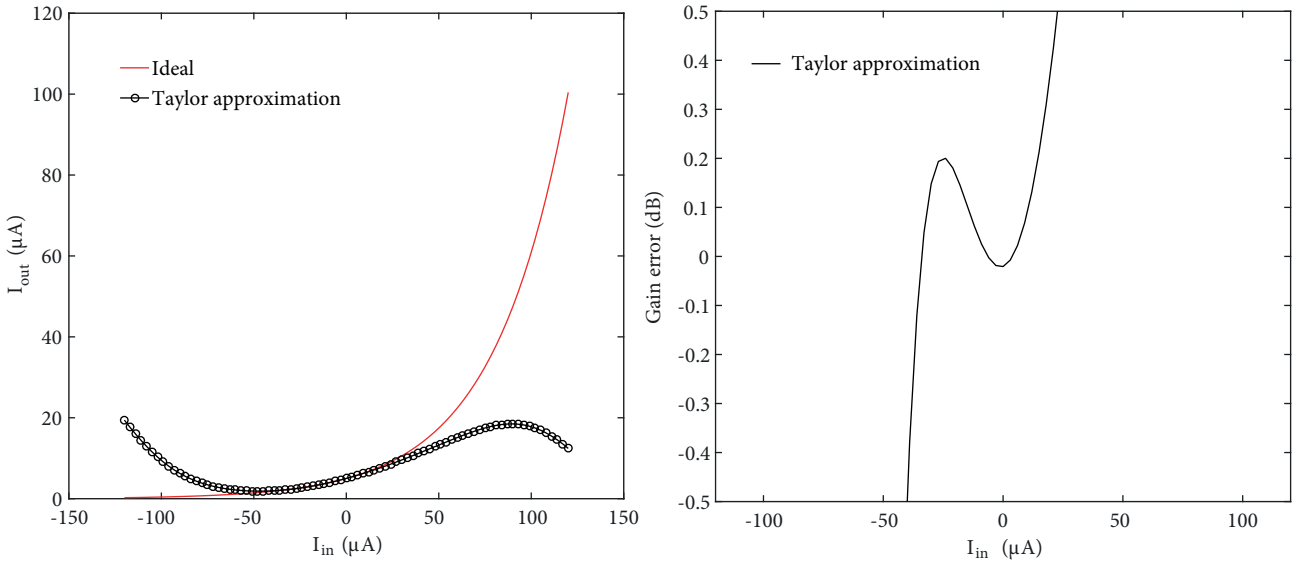

Figure 3. Simulation results and gain error of second-order Taylor expansion.

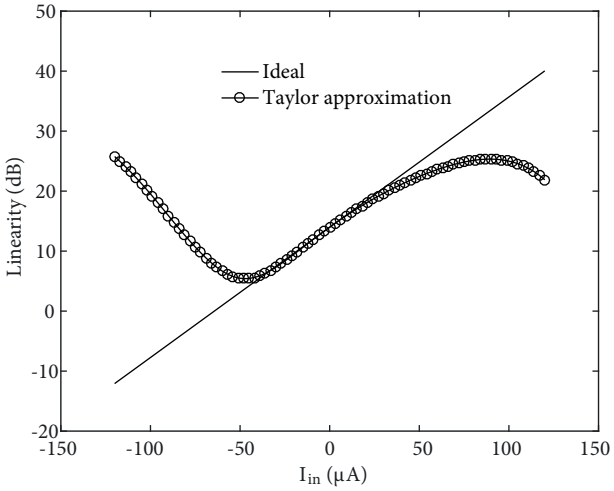

Figure 4. Linearity of second-order Taylor expansion.

3. Range-segmented circuit

For extending the linearity at the limitation of output gain error less than 0.5 dB, we could inject or elicit current to or from I_{out} to decrease the gain error. Four candidate circuits shown in Figure 5 includes two quadratic circuits designed in Section 2.1 and two linear circuits constructed by current mirrors. The flow-in circuits shown in Figures 5a and 5b will inject current into I_{out}, and the flow-out circuits shown in Figures 5c and 5d will elicit the current from I_{out}. We select the candidate circuit to plug into a designed circuit by comparing their contribution ranges.

For example, if $I_{in} \geq I_A$, the gain error will be greater than 0.5 dB shown in Figures 6a and 6b. Thus, if we plug the linear flow-in circuit of Figure 5a into a designed circuit like that in Figure 2 to make a circuit like that shown in Figure 7, then the gain error will be less than 0.5 dB for $I_{in} \leq I_B$ shown in Figure 6a. Therefore,

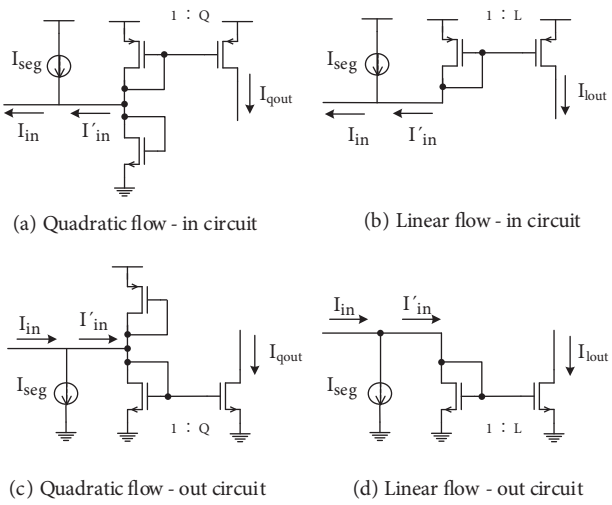

Figure 5. Four candidate circuits: (a) linear flow-in circuit, (b) quadratic flow-in circuit, (c) linear flow-out circuit, (d) quadratic flow-out circuit.

the input range is extended to I_B due to plugging the linear flow-in circuit. Similarly, if we use quadratic flow-in circuit shown in Figure 5b instead of linear flow-in circuit shown in Figure 5b to make a circuit like that shown in Figure 8, then the input range will extend to I_C shown in Figure 6b.

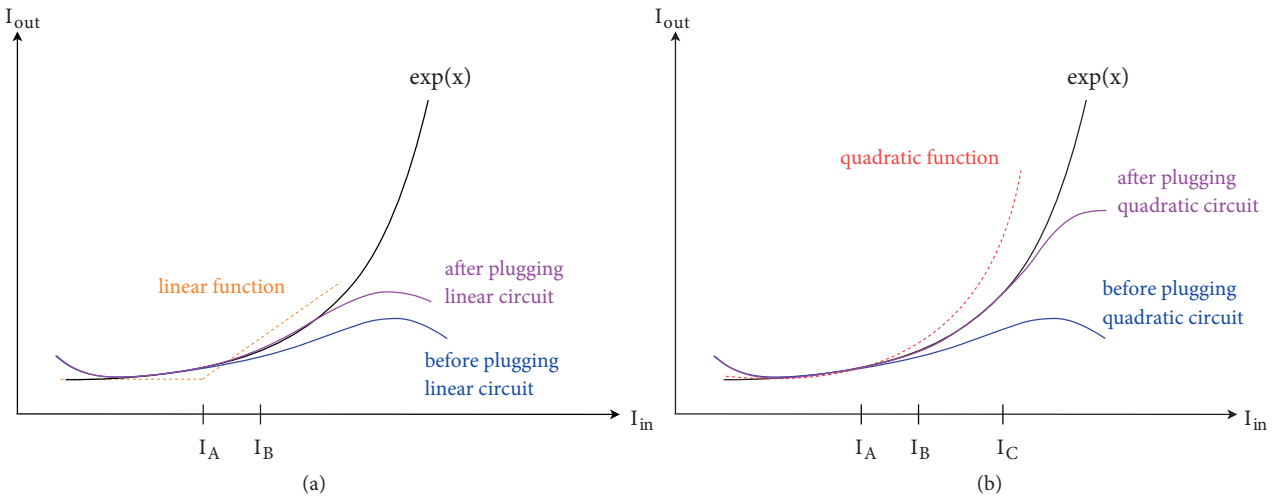

Figure 6. Simulation representation of two plugging circuits: (a) before and after plugging a linear circuit, (b) before and after plugging a quadratic circuit. In this figure, plugging a quadratic circuit could extend a larger range.

If $I_C \geq I_B$, then the quadratic flow-in circuit shown in Figure 5b will be the best selection to make an extending segment circuit. Otherwise, the best selection circuit will be the linear flow-in circuit shown in Figure 5a. For example, if the simulation result is as described in Figure 9, we will select the linear circuit as the plug-in circuit because the quadratic circuit only contributes an input range up to I_B shown in Figure 9a. Therefore, the extended segment is from I_A to I_C shown in Figure 9b. Based on the range-segmented method, we can design a wide-range multiple-segment circuit.

We observe that the error of I_{out} in Figure 6 is close to the quadratic function. In Figure 9, we observe that the linear function is closer to the output error than the quadratic function. Therefore, the range-segmented

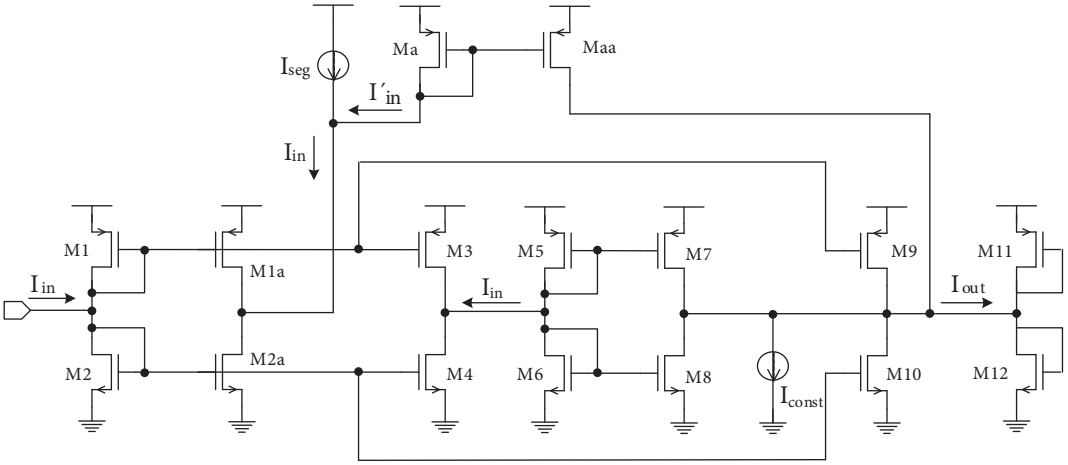

Figure 7. Exponential circuit plugged with one linear flow-in circuit.

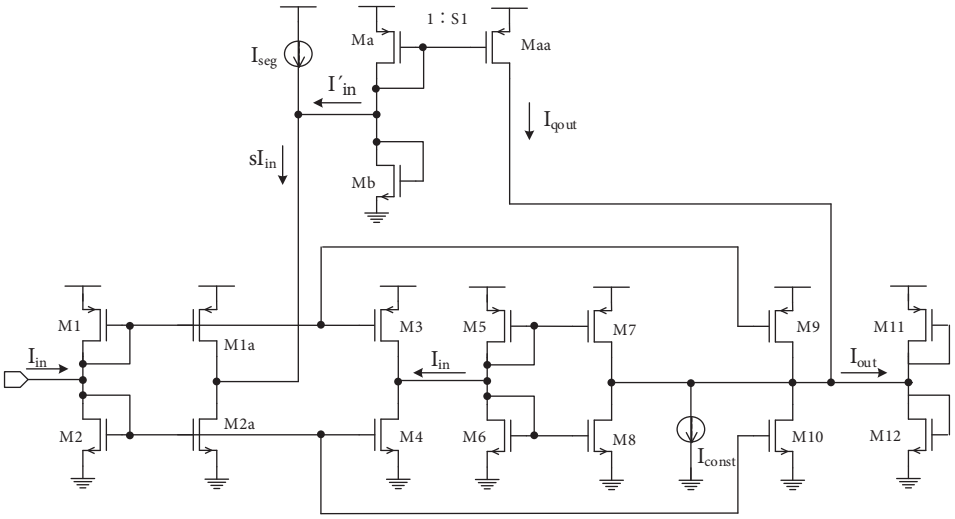

Figure 8. Exponential circuit plugged with one quadratic flow-in circuit.

method is to observe the trend of the simulation error in each segment to determine whether the segment is most suitable for plugging a linear circuit or a quadratic circuit. When observing that the simulation output is less than the ideal value, we use the flow-in circuit to increase the output value, otherwise the flow-out circuit shown in Figures 5c or 5d is used to reduce the output value.

4. Design and simulation results

The range-segmented circuit design is dependent on simulation results for each extending segment. We design a range-segmented exponential circuit using UMC 0.18 μm CMOS technology. When using any candidate circuit in Figure 5, we need to resize some transistors, and adjust the I_{seg} to make a suitable output. For example, in the first segment, when plugging a linear circuit like that shown in Figure 7, the resizing results are shown in Table 1.

I_{seg} in Figure 7 is like a switch, if $I_{in} > I_{seg}$, the current mirror pair Ma and Maa is on. The linear circuit will inject a multiple of I'_{in} into I_{out}. If we plug a quadratic circuit like that shown in Figure 8, the resizing results are shown in Table 2.

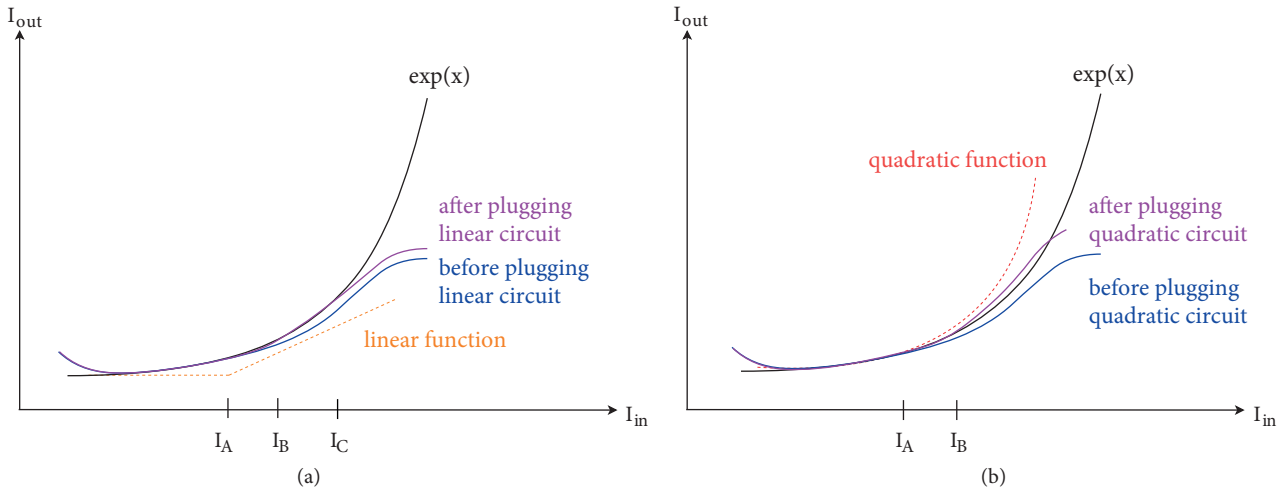

Figure 9. Simulation representation of two plugging circuits: (a) before and after plugging a quadratic circuit, (b) before and after plugging a linear circuit. In this figure, plugging a linear circuit could extend a larger range.

Table 1. Linear circuit resizing of the first segment.

	Design value	Resizing result
I_{seg}	21 μA	21 μA
Ma (W/L)	5.5 μm/0.8 μm	9.0 μm/0.8 μm
Maa (W/L)	1.1 μm/0.8 μm	0.7 μm/0.8 μm

Table 2. Quadratic circuit resizing of the first segment.

	Design value	Resizing result
I_{seg}	21 μA	28 μA
M1a (W/L)	5.5 μm/0.8 μm	1.8 μm/0.8 μm
M2a (W/L)	1.1 μm/0.8 μm	0.36 μm/0.8 μm
Ma (W/L)	5.5 μm/0.8 μm	1.8 μm/2.0 μm
Mb (W/L)	1.1 μm/0.8 μm	0.36 μm/2.0 μm
Maa (W/L)	5.5 μm/0.8 μm	7.5 μm/2.0 μm

From Figure 8 and Table 2, we have $sI_{in} = 0.3I_{in}$, and $I'_{in} = 0.3I_{in}$–I_{seg}. From Figure 1 and Eq. (1), we have $I_{qout} = s1KV_0^2(1 - \frac{I'_{in}}{4KV_0^2})^2$, where s1 is the current mirror scale. I_{qout} will inject into I_{out}. Table 3 summarizes simulation results for each segment plugged with a linear circuit and a quadratic circuit.

Table 3. Range results of the five segments.

	Segment 1	Segment 2	Segment 3	Segment 4	Segment 5
Linear circuit (μA)	21 to 42	78 to 105	105 to 120	177 to 198	–45 to –39
Quadratic circuit (μA)	21 to 78	78 to 93	105 to 177	177 to 186	–63 to –39

Therefore, in the first segment, we select the quadratic circuit as the plug-in circuit. In this segment, we

extend the input range from 21 μA to 78 μA. The types of flow-in or flow-out for each segment are shown in Table 4.

Table 4. Segmented results and flow direction of the five segments.

	Segment 1	Segment 2	Segment 3	Segment 4	Segment 5
Linear circuit	×	flow-in	×	flow-in	×
Quadratic circuit	flow-in	×	flow-in	×	flow-out

The final range-segmented circuit is implemented in Figure 10. The plug-in circuit of the first segment introduces a multiple of I_{in} into the quadratic flow-in circuit by M1a and M2a. Therefore, a small quadratic current will flow into I_{out} to reduce the error.

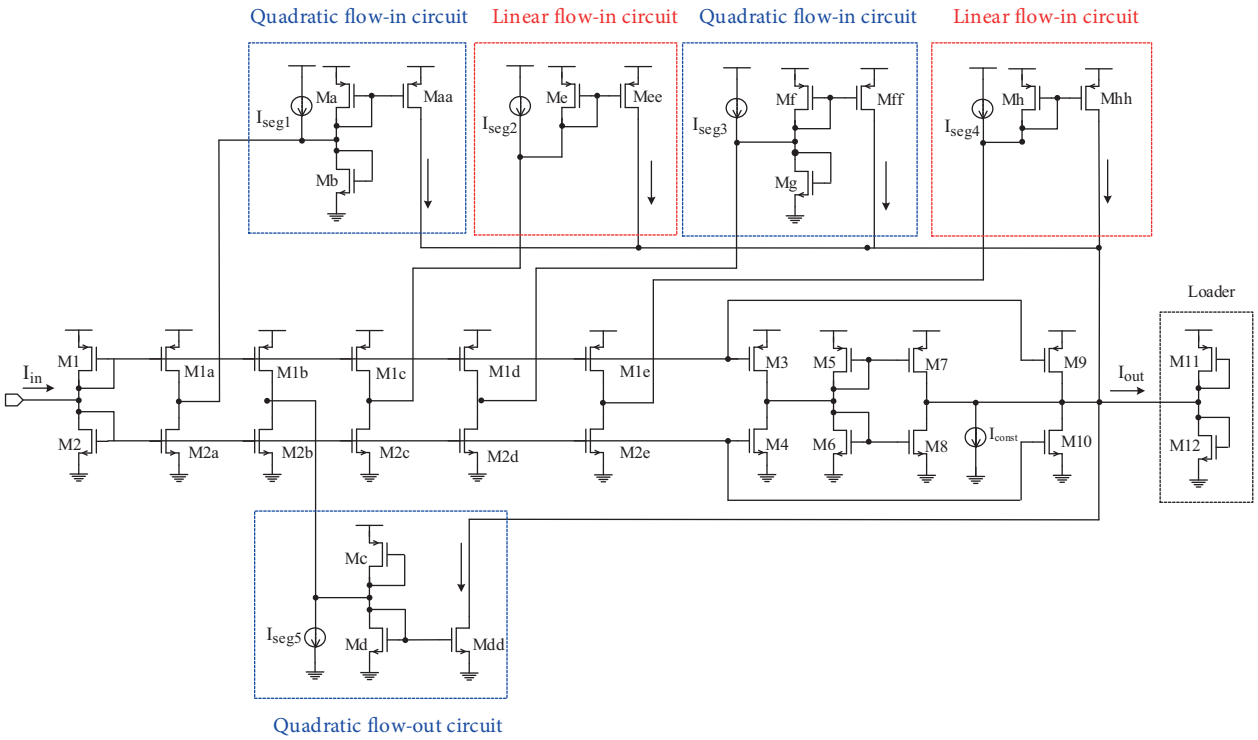

Figure 10. Proposed exponential circuit.

The plug-in circuit of the second segment transfers I_{in} to the linear flow-in circuit via M1c and M2c, and producing a small linear current flowing into I_{out} to reduce the error. Similarly, the plug-in circuits of the third and fourth segments are designed to complement the current of I_{out} in accordance with the above design. The plug-in circuit of the fifth segment is to reduce the error by pulling out some small quadratic current from the I_{out} current by quadratic flow-out circuit when I_{out} is greater than the ideal value. The size of each transistor is presented in Table 5.

Simulation results in Figure 11 show the output result and gain error of the proposed circuit. We can see the gain error less than 0.5 dB for input range from –63 to 198 μA. Figure 12 shows that the linearity is up to 56.7 dB for gain error less than 0.5 dB.

In order to show that the range-segmented circuit has better linearity, we replace all the segments with

Table 5. Size of transistors.

MOS	W/L ($\mu m/\mu m$)	MOS	W/L ($\mu m/\mu m$)	MOS	W/L ($\mu m/\mu m$)	MOS	W/L ($\mu m/\mu m$)	MOS	W/L ($\mu m/\mu m$)
M1	5.5/0.8	M8	1.1/0.8	Ma	1.8/0.8	Mdd	3.7/0.8	Mf	2.25/0.8
M2	1.1/0.8	M9	6.7/0.8	Mb	0.36/0.8	M1c	5.5/0.8	Mg	0.5/0.8
M3	5.5/0.8	M10	1.6/0.8	Maa	7.5/2.0	M2c	1.1/0.8	Mff	40.0/0.8
M4	1.1/0.8	M11	12.0/0.8	M1b	1.1/0.8	Me	5.5/0.8	M1e	5.4/0.8
M5	5.5/0.8	M12	4.0/0.8	M2b	0.22/0.8	Mee	3.6/0.8	M2e	1.1/0.8
M6	1.1/0.8	M1a	1.8/0.8	Mc	1.1/0.8	M1d	2.25/0.8	Mh	5.4/0.8
M7	11.0/0.8	M2a	0.36/0.8	Md	0.22/0.8	M2d	0.5/0.8	Mhh	20.0/0.22

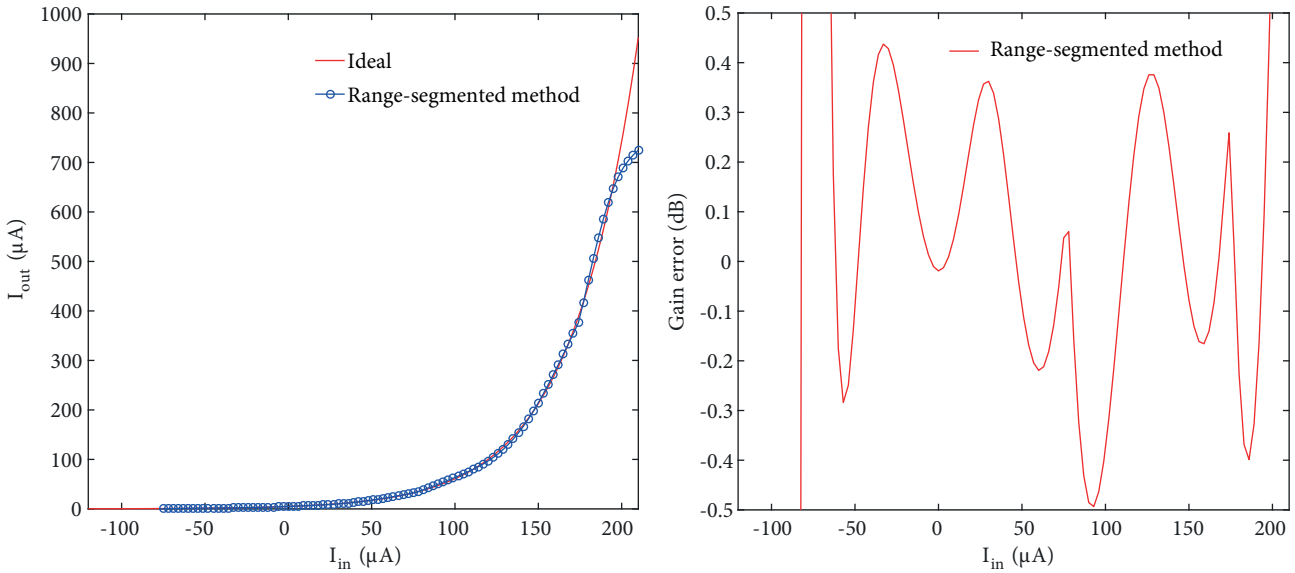

Figure 11. Simulation results and gain error of the proposed exponential circuit.

a linear circuit and simulate it. Then we use quadratic circuit to replace all segments and do the simulation. The results are shown in Figure 13. Table 6 shows the input range and linearity of these circuits.

Table 6. Linearity comparison of different methods.

Methods	Input range (μA)	Linearity (dB)
Taylor	–39 to 21	13.03
Linear (all segments)	–45 to 132	38.4
Quadratic (all segments)	–63 to 111	37.7
Range-segmented method	–63 to 198	56.7

Among these circuits, the linear circuit and the quadratic circuit perform similarly, while the range-segmented circuit is relatively superior. When we observe the simulation results of Table 3, we will find that segment 1 and segment 3 have larger range extension, while segment 2 and segment 4 are smaller. In addition

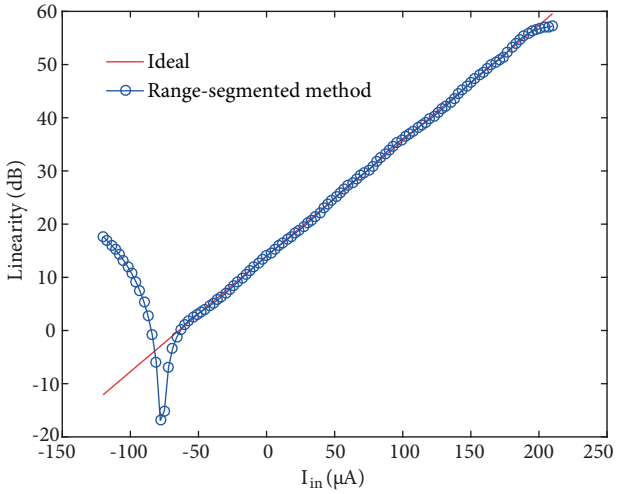

Figure 12. Linearity of the proposed exponential circuit.

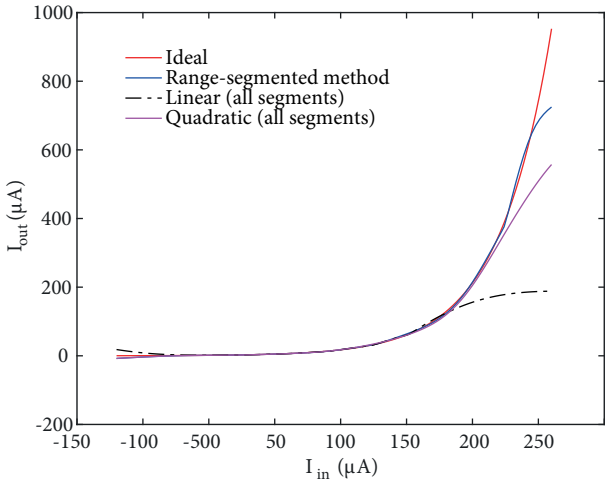

Figure 13. Simulation results of all linear-segments method, all quadratic-segments method, and range-segmented method.

to that segment 5 is the flow-out circuit, our quadratic flow-in circuit (segment 1 and segment 3) has a larger range extension than the linear flow-in circuit (segment 2 and segment 4). However, it is observed from Table 6 that not all segments adopt a quadratic circuit to get better results. This may be because the high accuracy limit makes the quadratic circuit lose its advantage in some cases as shown in Figure 9a.

To verify the variation of the proposed circuit, we used the Monte Carlo method to simulate the output of the circuit. The standard deviations of the threshold voltage (V_t) and current factor (β) of NMOS and PMOS for 0.18 μm technology from [21] are:

$$\sigma(\Delta V_{tn}) = \frac{5.0}{\sqrt{WL}} \quad (mV) \tag{11}$$

$$\sigma(\Delta V_{tp}) = \frac{5.49}{\sqrt{WL}} \quad (mV) \tag{12}$$

$$\frac{\sigma(\Delta \beta_n)}{\beta_n} = \frac{0.99}{\sqrt{WL}} \quad (\%) \tag{13}$$

$$\frac{\sigma(\Delta \beta_p)}{\beta_p} = \frac{1.04}{\sqrt{WL}} \quad (\%) \tag{14}$$

The Monte Carlo simulation results are shown in Figure 14 using 3σ and 30 Monte Carlo runs. In this simulation, we observe that about 73% of the relative error are within $\pm 5\%$ in Figure 15. The maximum relative error is at $\pm 8\%$, which occurred only twice. We observe Figure 11 that the error has eight peaks under 0.5 dB, and five of them are close to ± 0.5 dB. If there are small variations in these positions, it will bring a large error as shown in Figure 15.

Table 7 compares the performance parameters of the proposed circuit with the reported exponential circuits in the literature. It can be seen that the proposed circuit, including five extending segments, exhibits a linearity of 56.7 dB.

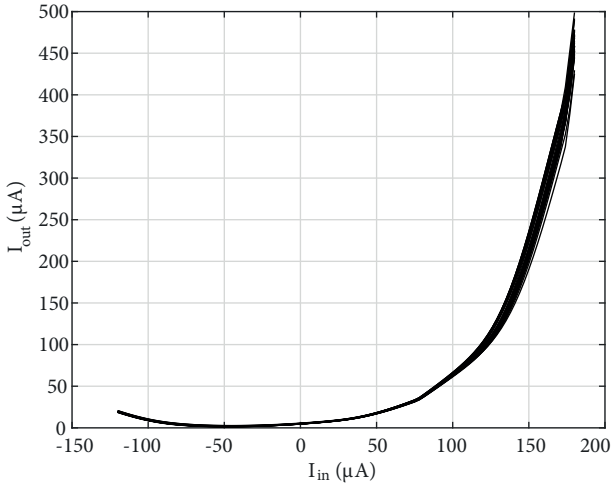

Figure 14. Monte Carlo simulation results of the proposed exponential circuit.

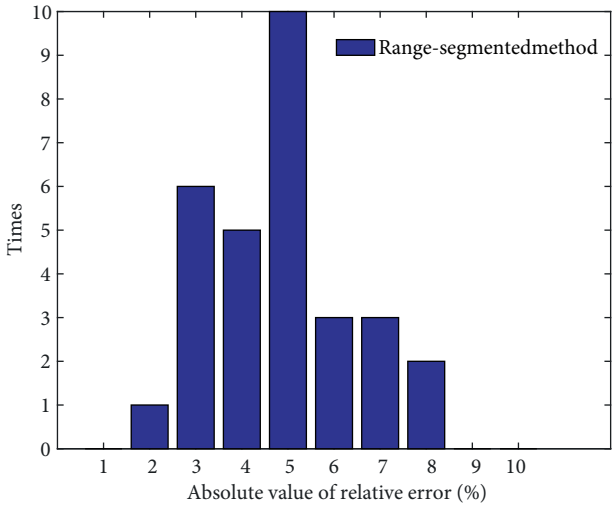

Figure 15. Counts of relative error for 30 Monte Carlo runs.

Table 7. Performance comparison of literature.

	[8]	[12]	[3]	[16]	[19]	[14]	[13]	[11]	This work
Linearity (dB)	40	70	96	46	41.1	52.6	66	78	56.7
Gain error (dB)	±0.75	±1	±0.5	±0.5	±1.05	±1	±0.5	±0.5	±0.5
Bandwidth (MHz)	NA	NA	0.105	NA	168.8	NA	31	67	69-150
Supply (V)	1.5	1.0	±0.75	1.2	2.5	3.3	±0.75	1.5	1.8
Power (mW)	NA	0.08	0.00613	0.45	0.535	NA	0.17	0.328	1.27
Process (nm)	350	350	350	130	130	350	180	180	180
Transistor count	80	64	77	67	56	NA	49+3I_{in}*	36+2I_{in}**	35+6I_{seg}***

*There are also three additional I_{in}. If the current mirror is used to copy I_{in}, then six transistors are required.
**There are also two additional I_{in}. If the current mirror is used to copy I_{in}, then four transistors are required.
***There are also six current sources or current sinks in the circuit. We need to include 12 transistors in the calculation.

Although it is not comparable to the linearity for transistors operating in weak-inversion [3], it has a bandwidth from 69 to 150 MHz. Circuits in [14, 16, 19] have the same high frequency characteristics as our circuit for operating in the saturation region. In [19], six-segment PWL is used in the design circuit, and our circuit uses only five segments, but has better linearity. Although [16] has the same accuracy as this work, its linearity is only 46 dB. [8] and [14] have no better performance in linearity and gain error. In [12], the circuit has better linearity and low power dissipation, but the accuracy is kept at 1 dB. Recent related researches have high linearity and high accuracy, as shown in [11, 13], their circuits also have fewer transistors. However, the performance of the bandwidth cannot be as high as 150 MHz as in this paper.

5. Conclusion

This paper presents a CMOS current-mode exponential circuit with range-segmented technology, which is suitable for extending a linearity range and high accuracy requirement. We use the selection method between linear circuit and quadratic circuit to get the largest input range. The proposed circuit including five extending

segments exhibits a linearity of 56.7 dB. Although it is not comparable to the linearity for transistors operating in weak-inversion, it has a bandwidth from 69 MHz to 150 MHz. The proposed circuit not only has a high linearity range but also has a high bandwidth and a high accuracy less than 0.5 dB.

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