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# Design of a substrate integrated waveguide matrix amplifier

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**Abstract:** Developments in microwave systems have increased the need for matrix amplifiers, which provide both high gain and wide frequency bands. The aim of this paper is to design a novel $2 \times 4$ matrix amplifier with a substrate integrated waveguide (SIW)-based power divider and combiner and a microstrip gain equalizer in the X and low Ku frequency bands. The proposed amplifier can be easily integrated with any microstrip, rectangular waveguide, or SIW-based circuits. The analysis and design of the amplifier is performed using two full wave simulators with different computational techniques (finite element method and finite integration technique) to verify the results. Simulation results show that the amplifier provides 16 dB gain with less than 4 dB ripple and more than 10 dB of input and output return losses in the frequency band of 8–15 GHz. This amplifier can be used as a wide band and high gain block in many microwave applications.

**Key words:** Matrix amplifier, substrate integrated waveguide, gain-bandwidth improvement, distributed structure

## 1. Introduction

The substrate integrated waveguide (SIW) structure offers the significant feature of integration capability that has great importance in advanced microwave and millimeter wave applications. Its importance is because of the need to realize the nonplanar circuits, particularly rectangular waveguides, in a planar configuration that is compatible with existing planar construction methods (e.g., printed circuit boards (PCB) low-temperature co-fired ceramics, high-temperature co-fired ceramics, and microwave integrated circuits). SIW structures have attracted great attention in developing high-frequency systems due to the mentioned feature and other advantages including the ability of high power transmission, high quality factor, easy and low-cost implementation process, and low radiation losses in high frequency. So far, various passive and active circuits have been implemented using SIW structures, such as filters [1], diplexers [2], passive and active antennas [3, 4], power dividers [5], oscillators [6], and amplifiers [7–11]. In this paper a matrix amplifier is analyzed and designed using the SIW structure.

The designed SIW amplifiers of previous studies did not have enough gain and bandwidth for some applications [7–9]. The amplifiers of [7] and [8] had only 10 dB gain and their frequency band included merely the X band. The amplifier of [9] had an extremely sloped gain, which is useless for practical applications. Matrix amplifiers are a suitable solution when both wide frequency band and high gain are required, because they combine the additive process of the distributed structure and the multiplicative process of the cascaded multistage amplifier [12]. On the other hand, the size of components at higher microwave frequencies becomes

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small and consequently the tolerable power and output power decrease. Hence, to achieve the higher power requirements of telecommunication systems, the input power should be divided and then combined after amplification in several distinct paths. These points show the importance of multitransistor amplifiers in high frequency systems. So far, these amplifiers have often been designed on microstrip lines and using rectangular waveguides in some cases, but until now, no effort has been made to design a matrix amplifier on a SIW structure. The purpose of this research is to take advantages of SIW structure features, including integration capability, low radiation losses, high quality factor, and the ability of high power transmission, to design a matrix amplifier working in X and low Ku frequency bands.

## 2. Design procedure

The first step in SIW-based designs is calculating the basic SIW parameters. An appropriate starting point is considering the SIW structure as a quasirectangular waveguide and calculating the equivalent width of the SIW ($a_e$), which by using the formula obtained in [13] is equal to:

$$a_e = a - 1.08d^2/p + 0.1d^2/a. \tag{1}$$

As shown in Figure 1, a, d, and p represent the center-to-center distance of SIW sidewall vias, the diameter of vias, and the distance between vias in a row, respectively.

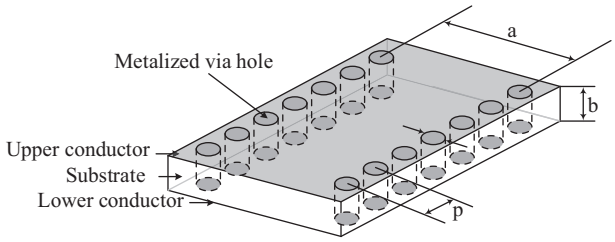


**Figure 1**. Substrate integrated waveguide structure.

In [14] an analysis was conducted to select the appropriate design parameters for practical applications that limit d and p as follows:

$$0.05 < p/\lambda_c < 0.2, \tag{2}$$

$$1 < p/d < 2. \tag{3}$$

Therefore, d and p are selected as d = 0.8 mm and p = 1.3 mm, so that their values satisfy the limitations.

The only modes that can propagate in this structure are $TE_{m0}$ modes. $TE_{mn}$ (n$\neq$0) and $TM_{mn}$ modes cannot be guided because the dielectric gaps created by the vias' separations will damp these modes. Consequently, the dominant mode is $TE_{10}$. Since the amplifier is designed for X and low Ku frequency bands (8–15 GHz), the cutoff frequency of the dominant mode of the structure should be set near 8 GHz to guarantee the single mode performance of the SIW. The cutoff frequency is considered as 7.5 GHz, which can be calculated as follows:

$$f_{c,TE_{10}} = 7.5GHz = c_\epsilon/2a, \tag{4}$$

from which we have $a_e = (c/\sqrt{\epsilon_r})/(15 \times 10^9) = (3 \times 10^8)/(\sqrt{3.55} \times 15 \times 10^9) \approx 10.6$ mm.

$\epsilon_r$ represents the relative permittivity of the substrate and $\mu_r$ represents the relative permeability of the substrate. By using 1 and 4 and the values of d and p, the width of the SIW structure can be calculated as $a = 10.6 + 1.08 \times (0.8^2/1.3) - 0.1 \times (0.8^2/a) \rightarrow a \approx 11.1$ mm.

The appropriate parameters of the SIW structure for the intended purpose are thus obtained. In this paper, the utilized substrate is RO4003 with height of 20 mil, loss tangent of 0.0027, and dielectric constant of 3.55. The four-stage distributed SIW amplifier reported in the literature has a sloped power gain that varies from 11 dB at the beginning of the frequency band to 2 dB at the end of the frequency band [9]. This is because the achievable gain of microwave transistors typically falls off as the frequency increases. Therefore, an equalization filter with positive gain slope is needed to achieve a flat power gain. Using this equalizer will decrease the gain to very low values. To solve this problem, two or more distributed amplifiers should be connected. In a matrix amplifier, several distributed amplifiers are cascaded in a matrix structure, instead of simply connecting the individual amplifiers in series. Matrix implementation has advantages such as eliminating many losses associated with the long interstage transmission line, dimensions reduction, etc. [12]. Therefore, a novel 2×N matrix amplifier is designed in this paper. The general structure of a matrix amplifier is shown in Figure 2. In order to take advantage of SIW features, the input and output lines are designed with this structure, and microstrip lines are used in the center line to easily transmit the power between transistors blocks.

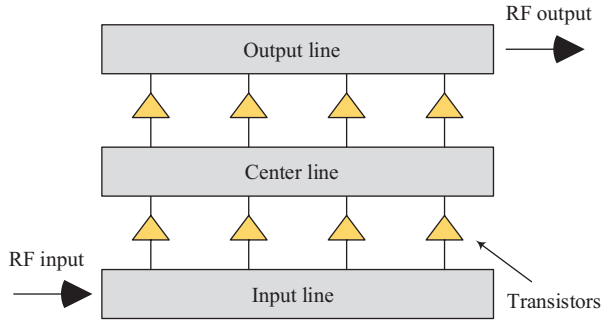


**Figure 2**. General structure of a matrix amplifier.

What determines the gain limit of a 2×N matrix amplifier is the transistors' physical characteristics, which will determine the gain in the first step and then losses and the value of N. The achievable gain of microwave transistors falls as the frequency increases, so in order to have a flat gain in a wide frequency band, the gain should be restricted. Furthermore, the slope of the gain of a matrix structure increases with the increase of N. This is another factor that has a significant role in the gain. Thus, the optimal N should be chosen to have the maximum gain. To address the issue, we can consider the gain of a 2×N matrix amplifier, which can be calculated using the following formula [15]:

$$A(\omega) = \frac{1}{2} g_{m1} g_{m2} Z_0 \frac{N Z_{0c} R_{ds1}}{(N Z_{0c} + 2R_{ds1})} \frac{\exp[-\frac{N}{2}(A_{d2} + A_{g1})] \sinh[-\frac{N}{2}(A_{d2} - A_{g1})]}{\sqrt{(1 + (\omega/\omega_{g1})^2)}\sqrt{(1 + (\omega/\omega_{g2})^2)}\sqrt{(1 - (\omega/\omega_c)^2)} \sinh(\frac{A_{d2} - A_{g1}}{2})}, \quad (5)$$

where:

$$\omega_{g2} = \frac{1}{R_{i2} C_{gs2}}, A_{g1} = \frac{(\omega^2 R_{i1} C_{gs1}^2 Z_g)}{2}, and A_{d2} = \frac{Z_d}{(2R_{ds2})}. \quad (6)$$

The gain of the 2×N matrix amplifier with our employed transistors in the first and second stages is shown in Figure 3 for various N values.

As can be seen, the transistors are not capable of providing a high constant gain in a wide frequency band, so the gain (which can be then flattened using equalizers) would be limited to its value at the end of the frequency band. Additionally, the slope of gain changes is increased with the frequency increase. The optimal N to have the maximum gain can be obtained by differentiating $A(\omega)$ with respect to N and setting the result equal to zero and solving the equation. The optimal N for our frequency band is shown in Figure 4. The optimum N in the center frequency is approximately 4, which is why a $2 \times 4$ structure is designed in this paper.

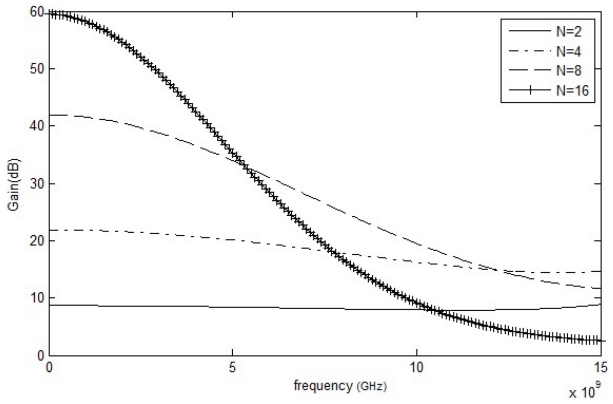


**Figure 3**. The gain of the $2 \times N$ amplifier for various values of N.

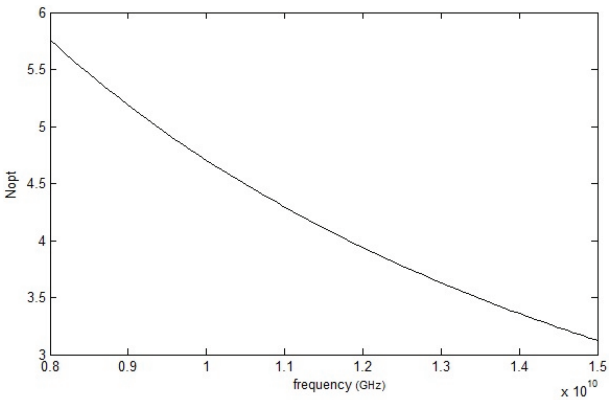


**Figure 4**. Optimum N in the frequency band of 8–15 GHz.

As mentioned, the active component in the first stage is the NE3210S01 transistor, which is a low noise PHEMT, and in the second stage TGF2025 is used, which is a discrete PHEMT with higher output power than NE3210S01. Our aim is to design a SIW matrix amplifier with a maximally flat gain and high input and output return losses in the entire frequency band (8–15 GHz). The amplifier is shown as separate building blocks in Figure 5 and each block will be analyzed in detail in the following subsections.

### 2.1. Active components blocks

In active components blocks, the connection between transistor legs and microstrip lines of the drain and gate should be modeled properly in order to consider the effects of grounding vias and the electromagnetic coupling between adjacent lines. The proposed model to place the NE3210S01 is shown in Figure 6. In this model the connecting microstrip lines, which are of length 2 mm after placement at appropriate distances, are analyzed by the ADS momentum full wave simulator, and then their S-parameters are called as a 6-port block and the transistors are connected to the amplifier circuit via this block instead of direct connection. The same approach is used for the first active components' block in Figure 5. The connecting lines of all four transistors are placed at proper distances and are full-wave analyzed. After embedding the transistors, the S-parameters are called as an 8-port block in the total structure. In this model, the source electrodes' connection to the ground is also modeled by some vias.

The transistors of second stage (TGF2025) are very small, in the size of 100 $\mu$m, so a tapered microstrip structure is used to connect the narrow lines to wide ones. The proposed structure is shown in Figure 7. At the second active components' block in Figure 5, ADS full wave analysis, embedding transistors, and finally calling the 8-port block in the total structure is performed in the same way as detailed above.

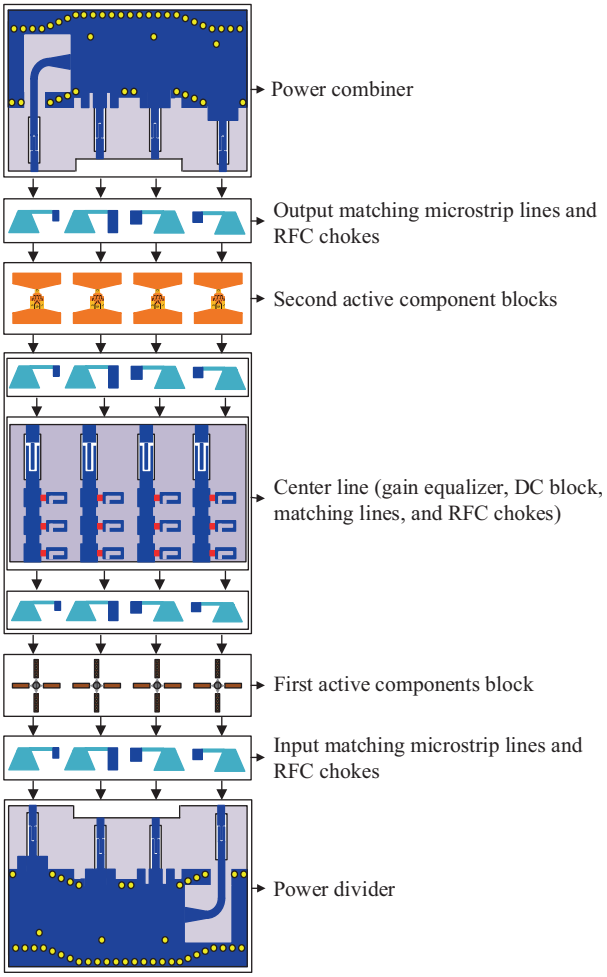


**Figure 5**. Building blocks of proposed matrix amplifier.

### 2.2. Power divider and power combiner

In order to simplify the design with the aim of synchronization of output powers of different paths, the same structure is used for both the power divider and power combiner in input and output blocks.

The proposed structure of the power divider shown in Figure 8 has one SIW input port and four microstrip output ports, designed in such a way that a quarter of total input power is delivered to each output port. For better power transmission from the SIW structure to microstrip line, two narrow gap lines (length of $L_{gapi}$ and width of $W_{gapi}$, i=1, 2, 3) has been created on the two sides of the microstrip line. These gaps develop a quasi-CPW structure in the length of $L_{gapi}$ that contributes to the conversion of surface current lines of the SIW to the microstrip line currents. Furthermore, the return losses in the input and output ports are improved by locating some vias near the SIW to microstrip converters. When the dominant TE10 mode reaches these discontinuities (end-to-end metalized posts = vias) in the SIW structure, degenerated TEn0 modes get excited in the place of discontinuities. These nonpropagating modes save magnetic energy in the surrounding area. The saved magnetic energy can be shown as an equivalent parallel inductance whose magnitude depends on frequency and size and position of the vias. Consequently, changing the position of vias affects their equivalent inductance values. Thus, these inductive discontinuities, which resemble short-circuited stubs, can be used

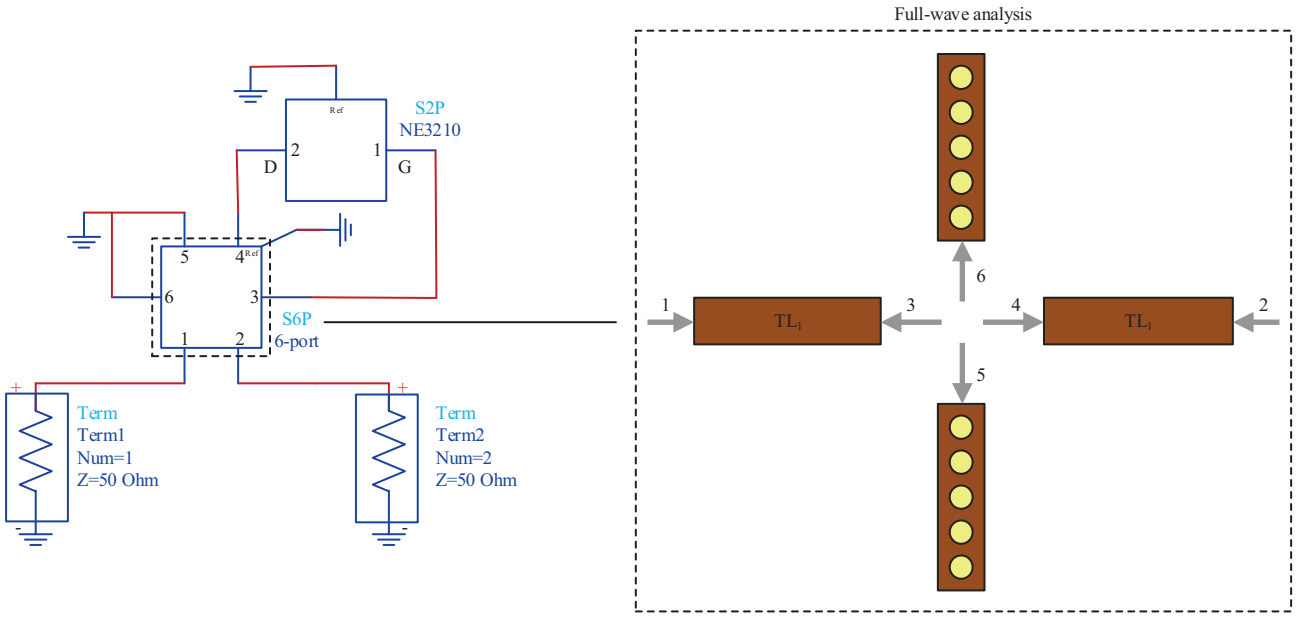


**Figure 6**. The proposed model to connect the NE3210S01 legs to the microstrip lines.

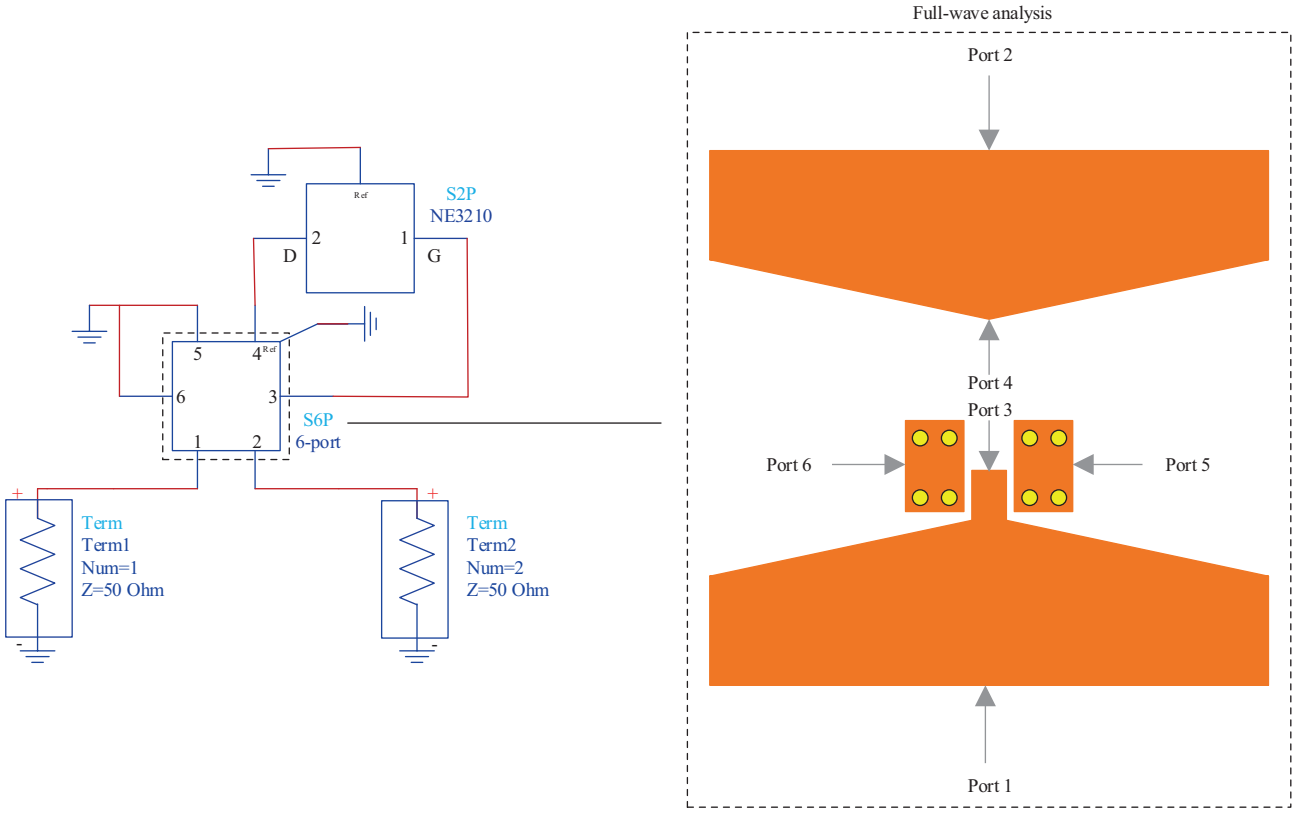


**Figure 7**. The proposed model to connect the TGF2025 to the microstrip lines.

as matching circuits. They are in fact matching vias. This configuration is used for matching purposes and the positions of the vias are optimized to acquire the best return losses in the input and output ports. The last stage of the power divider is actually an appropriate converter from the SIW to microstrip line whose microstrip output is placed along the other outputs via a 90° bend. This converter is designed in such a way that it transmits all remaining power to the last output port.

Also, according to the achievements in [16] for improving tapered converters, two vias are located on the two sides of the converter at the end of the power divider to improve the return losses.

On the other hand, the synchronization of outputs should be considered because it has a significant importance in these designs. Using the firm bend shown in Figure 6 contributes to the equalization of the electrical lengths of all four amplifying paths, which leads to output synchronization.

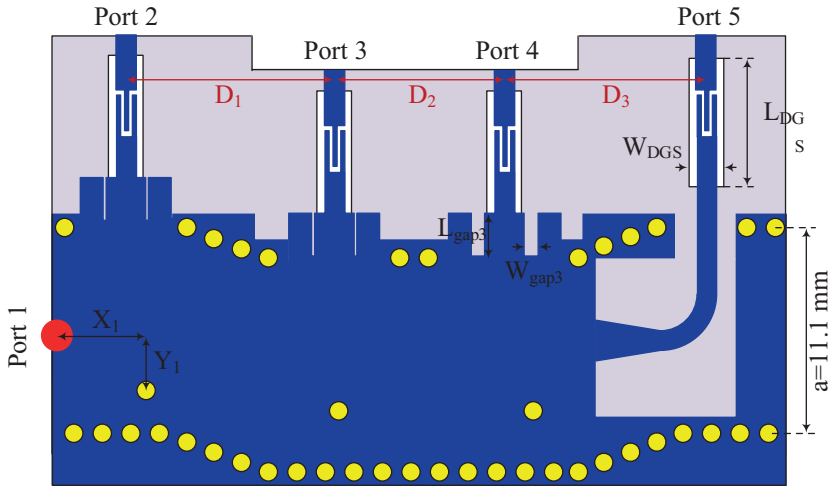


**Figure 8**. Detailed configuration of power divider.

The other point is connecting the proposed power divider to the active component block. As is clear, the upper conductor of the SIW structure is connected to its ground layer. Since direct feeding of the transistor causes a potential difference between the ground layer and the upper conductor of the gate and drain microstrip lines, it is not possible to directly connect the SIW to these lines. A DC block network should be used at the end of each path of the power divider. These DC block networks are implemented in a CRLH microstrip line configuration that operates as a band-pass filter. It consists of an interdigital capacitor and a DGS structure, where changing their parameters (including the length and width of the interdigital capacitor fingers and the DGS structure dimensions) can set the appropriate center frequency and bandwidth of the filter. The designed and utilized DC block network has more than 15 dB of input return loss and less than 0.6 dB of insertion loss in the frequency band of 8–15 GHz. Eventually, the final structure of Figure 6 is simulated for several values of parameters demonstrated in Table 1 and is optimized based on maximum return loss and equality of powers in four microstrip outputs. The optimal values are also represented in Table 1.

**Table 1**. Optimal values of parameters of the power divider.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| $D_1$ | 10.39 mm | $L_{gap1}$ | 3.08 mm | $W_{gap1}$ | 0.2 mm | $X_1$ | 5.05 mm | $Y_1$ | 3.0 6mm |
| $D_2$ | 8.71 mm | $L_{gap2}$ | 3.1 mm | $W_{gap2}$ | 0.2 mm | $X_2$ | 15.42 mm | $Y_2$ | 3.6 mm |
| $D_3$ | 10.39 mm | $L_{gap3}$ | 3.1 mm | $W_{gap3}$ | 0.77 mm | $X_3$ | 24.64 mm | $Y_3$ | 3.6 mm |

### 2.3. Gain equalizer

The required gain equalizer should provide a gain with a positive slope in order to make up for the gain fall of the transistors with frequency increase. Due to the similarity of the frequency response of gain equalizers to that of resonators, a resonator structure can be used in this block. Various methods have been proposed to implement such gain equalizers [17–19]. The employed structure in this paper, shown in Figure 9a, is a modified structure of the previous equalizers mentioned above. It consists of 3 series microstrip branches loaded by thin layer resistances. The detailed structure of the resonance branch is shown in Figure 9b. Through several simulations by full-wave simulator HFSS it is found how changing the dimensions of resonance branches (including S, W, and L shown in Figure 9b) and the resistance value (R) changes the frequency response of the structure and the result is shown in the Figure 10. As can be interpreted from the curves, center resonance frequency increases with increasing L and W and decreasing S. Reducing R would also increase the Q-factor, which means an increase in the minimum value of S21. Correspondingly, changing these parameters, the intended center resonance frequency and Q-factor could be adjusted.

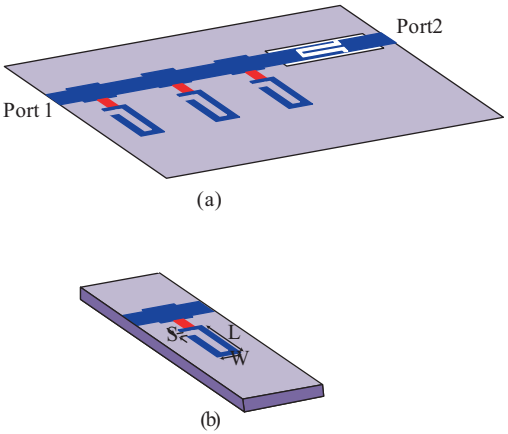


**Figure 9**. (a) Proposed gain equalizer with DC block network, (b) detailed structure of a resonance branch.

Since the amplifier is designed for the 8 to 15 GHz frequency band, the center resonance frequency of the gain equalizer is adjusted at 8 GHz so the power loss would be minimal. The Q-factor is also adjusted in such a way that the equalizer provides a gain with approximately the same slope compared to the gain of the amplifier without it, but in the opposite direction. Putting series resonance branches and optimizing the lengths and widths of microstrip lines between the branches, the required bandwidth and return losses are obtained. The return loss of the proposed equalizer is more than 10 dB all over the frequency band. A DC block is also included in this block to separate it electrically from subsequent blocks. The optimized parameters of the equalizer are shown in Table 2.

**Table 2**. Optimal values of parameters of the equalizer.

| L | W | S | R |
|---|---|---|---|
| 3.3 mm | 1 mm | 0.36 mm | 90 ohm |

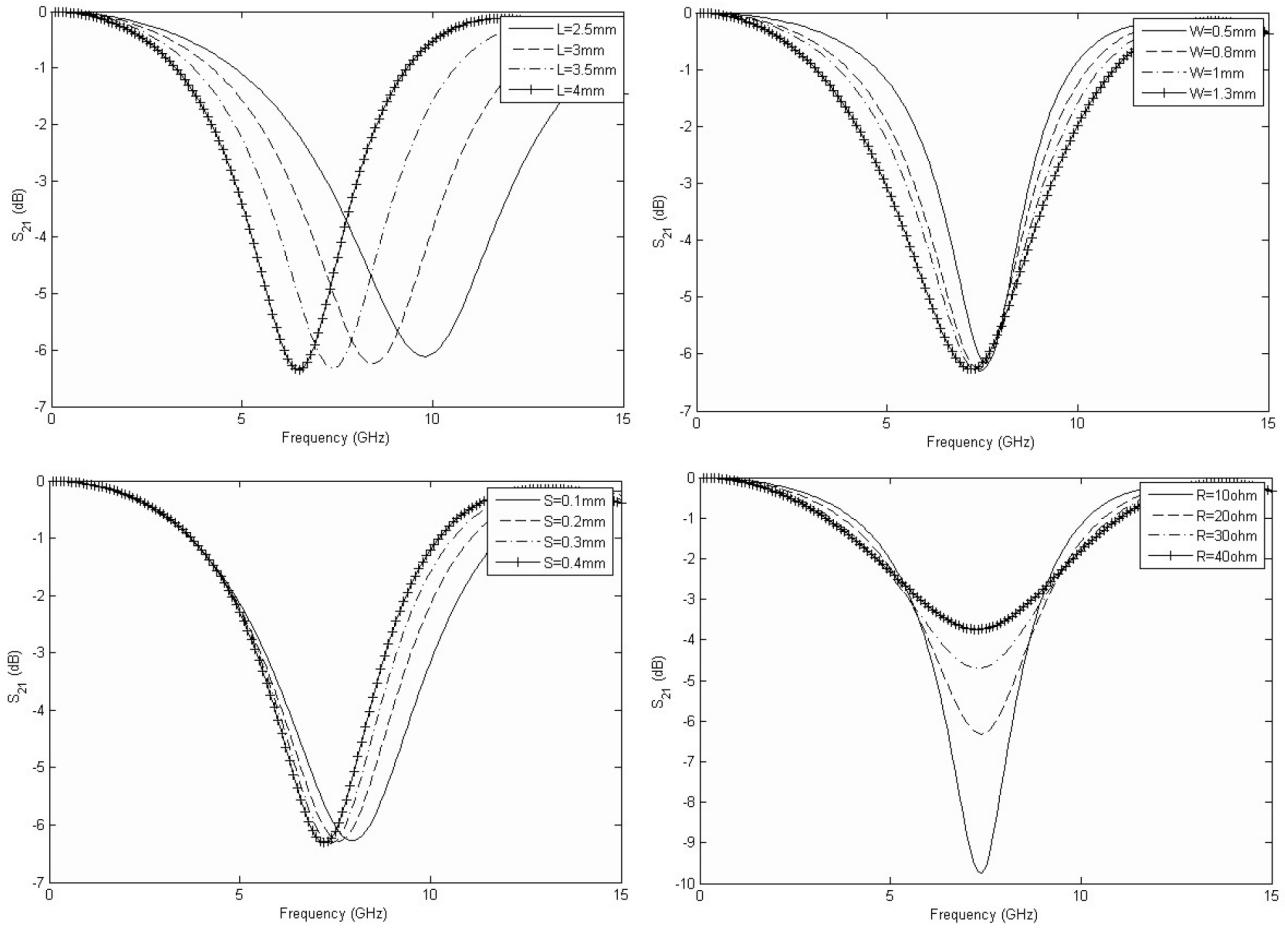


**Figure 10**. Frequency response of the resonance branch for various L, S, W, and R.

### 2.4. Microstrip matching networks and final amplifier design

Finally, the active component blocks are connected to the adjacent blocks by four microstrip matching networks that can be observed in Figure 5. Simple microstrip lines are used here instead of single or double stub impedance matching, aiming at minimizing the radiation losses. These lines are of variable dimensions and their lengths and widths are optimized based on maximum power gain with minimum ripple and maximum return losses in input and output ports. This optimization, performed in ADS, is done for several power dividers and the best response is selected. The major issue that should be considered in optimizations is choosing the lengths in such a way that ends in equal lengths of the final four paths of the amplifier. In addition, the RFC chokes are inserted in these blocks. These chokes are employed in order to prevent the leakage of the RF signal to the DC bias circuit. Lastly, the full wave analysis of these four blocks is accomplished by ADS momentum and their S-parameters are used in final amplifier S-parameter calculations.

After simulating the blocks in the HFSS software, their S-parameters are exported to the ADS software in order to connect them to the active components and calculate S-parameters for the end-to-end model of the amplifier. Moreover, for verification of the proposed method, the blocks are simulated in the CST simulator as well. The CST is based on the finite integration technique, unlike the HFSS, which is based on the finite element method. The simulation results for the two simulators are shown in Figure 11. Good agreement is

observed between them. The designed amplifier has more than 16 dB of gain with less than 4 dB ripple in the frequency range of 8.2–14.7 GHz and the return losses on the input and output ports are more than 10 dB in nearly the entirety of this frequency band. The simulation of the noise figure is shown in Figure 12. The NF of the amplifier is under 6 dB from 8.2 GHz to 14.7 GHz. The stability factor is also shown in Figure 13, and as can be observed there, it is larger than 1 at all frequencies. The designed amplifier is thus unconditionally stable over the entire frequency band. The matrix configuration has also increased the linear achievable output power compared to those achieved by SIW amplifiers in [7–9]. According to the utilized transistors' output powers, the maximum output power that can be obtained from this matrix amplifier is 28 dBm. Interested researchers can easily fabricate and use this amplifier in microwave systems.

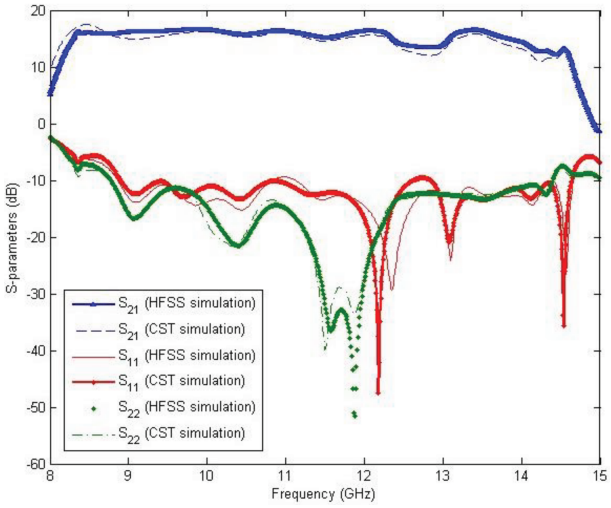


**Figure 11**. S-parameters of the amplifier.

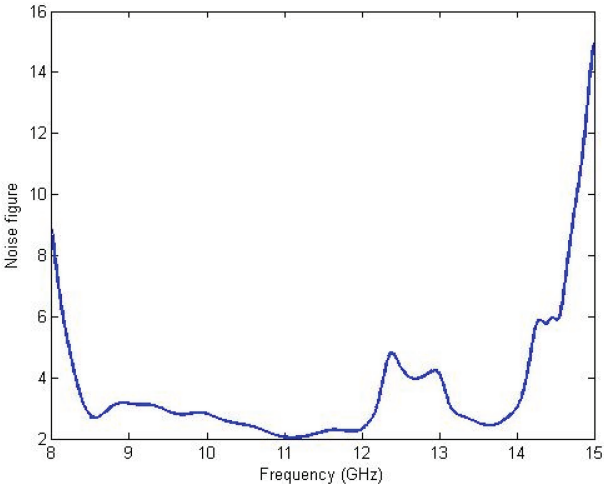


**Figure 12**. Noise figure of the amplifier.

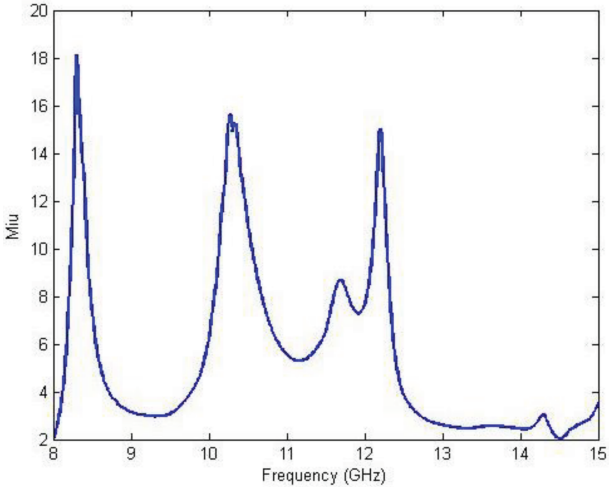


**Figure 13**. Stability factor of the amplifier.

Since power considerations limit the linear operating region of microwave transistors, the power should be investigated in order to determine the dynamic range of the amplifier. For the transistors of the first stage (NE3210S01) with the bias point that is selected ($V_{DS}$ = 2 V, $I_D$ = 10 mA) and in the center frequency (12

GHz), output power in the 1 dB gain compression point ($P_{1dB}$) is 14 dBm, which is obtained by 4dBm of input power ($P_{IN,1dB}$). Practically, transistors would operate in the linear part if their input power is less than $P_{IN,1dB}$, so the maximum linear output power would be less than $P_{1dB}$ as well. Hence, the maximum achievable linear power of the NE3210S01 transistor is considered 12 dBm. Since the first stage's transistors' output power, which is amplified and comparatively high, would be the input power of those in the next stage, the transistors of the second stage must be chosen among transistors with higher $P_{1dB}$.

For the transistors of the second stage (TGF2025) in its bias point ($V_{DS} = 8$ V, $I_D = 40$ mA) and in the center frequency (12 GHz), $P_{1dB}$ is equal to 24 dBm and $P_{IN,1dB}$ is 10 dBm. In order to work in the dynamic range, the maximum output power of the TGF2025 transistors is considered as 22 dBm. The maximum input and output powers of the transistors and the end-to-end amplifier are shown in Figure 14. In order to guarantee the linearity of the amplifier, the maximum input power could be 2 dBm and the maximum output power that can be obtained is 28 dBm.

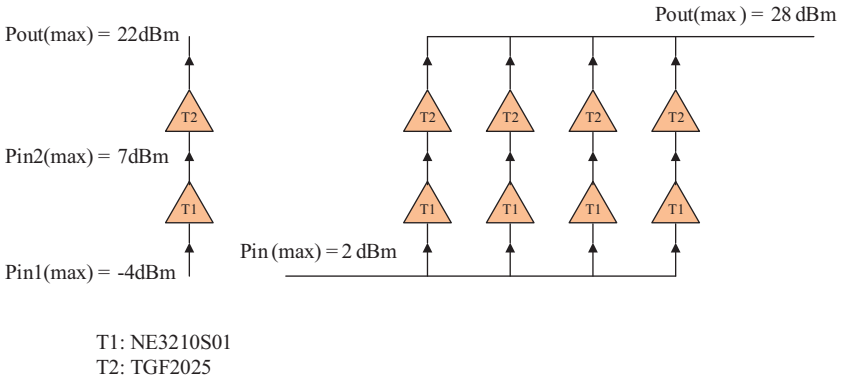


**Figure 14**. Maximum input and output powers.

## 3. Conclusion

In this paper, for the first time a SIW-based matrix amplifier has been presented that provides a high gain and wide frequency band for microwave applications. To design the proposed matrix amplifier, a SIW-based power divider has been introduced and analyzed that has been used as a power combiner at the end of the amplifier as well. By using the new technique of addition of two vias to the conventional tapered transition at the end of the power divider, its return loss is improved. Also, by changing the position of three vias embedded in the power divider and the size of gaps created near its output ports, the maximum return losses and the equality of powers at the four output ports are achieved. Using the SIW in this design leads to a lower radiation loss compared to its microstrip peer. Furthermore, an equalizer is used to flatten the power gain. Eventually, we achieve an amplifier that features a gain of 16 dB with less than 4 dB of ripple in the wide frequency band of 8.2–14.7 GHz, and its input and output return losses are more than 10 dB in the entire frequency band. So far, no SIW amplifier has been designed that can provide such a high gain and broad bandwidth, so the proposed matrix amplifier can be used in SIW-based microwave systems that need a gain block with high gain and wide bandwidth.

The results of this work are compared to those of previous studies [7–9] in Table 3. As can be interpreted, the bandwidth of the proposed amplifier is increased by 75 percent compared to the proposed amplifiers of [7] and [8]. Moreover, the power gain of the proposed amplifier is more by 6 dB. On the other hand, although the

distributed amplifier of [9] is designed to work in the frequency band of 8 to 15 GHz, it presents a sloped gain, which varies from 11dB at 8GHz to 2dB at the end of the frequency band. The proposed amplifier of this project is obviously improved regarding both gain magnitude and ripple. Furthermore, the maximum achievable linear output power is considerably increased compared to previous SIW amplifiers. In fact, the maximum achievable power of the proposed amplifier is 630 mW which is twelve, eleven, and ten times more than those of amplifiers in [7], [8], and [9], respectively.

**Table 3**. Comparing the results of this paper with previous works.

| | Frequency band (GHz) | Gain (dB) | Maximum linear output power (dBm) |
|---|---|---|---|
| Ref. [7] | 8-12 | 10 (<2 dB ripple) | 12 |
| Ref. [8] | 8-12 | 10 (<2 dB ripple) | 15 |
| Ref. [9] | 8-15 | 2 < gain < 11 | 18 |
| This work | 8-15 | 16 (<4 dB ripple) | 28 |

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