Heat flux capacity measurement and improvement for the test of superconducting logic circuits in closed-cycle cryostats

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Abstract: With the current progress of superconducting integrated circuits, circuit complexities have reached more than 100,000 Josephson junctions. At the laboratory environment, circuit tests are generally being conducted at liquid Helium environments. With the commercialization of the superconducting integrated circuit-based systems and/or price increase of liquid Helium, utilization of the closed-cycle systems will be inevitable. Even though it is possible to implement closed-cycle systems with quite substantial excess cooling powers after all the wirings and peripheral circuits, one point not to be overlooked is the power density at the superconducting chips. We have observed that the circuits designed for operation at liquid Helium bath have much higher power densities that exceed the heat flux capacities of closed-cycle cryocoolers. We have measured that the heat flux capacities of closed-cycle systems are about 0.1 W/cm^2 when the chip is in vacuum. Thus, if the power density in any of the bias resistors are higher than these values, it is difficult to keep the chip in superconducting state. With the positive feedback from a local hot spot under current bias, the chip rapidly heats up due to Joule heating. To increase the limit of power density, we propose an encapsulation method that increases the heat flux capacity of the system. With the encapsulation, the heat flux capacity of the system is increased to about 0.4 W/cm^2.

Key words: Superconductivity, single flux quantum, power density, heat flux capacity

1. Introduction

The use of a cryogenic environment for the superconductor applications is inevitable. Due to the limited resources of Helium and its rising price, as well as practical reasons, the use of the liquid Helium (LHe) may still be favorable at laboratory applications, but it is not feasible for industrial applications. Due to advances in cryogenics technology, coolers get more efficient and smaller. Especially the one-stage coolers that are used for high-temperature superconductor devices have been improved over years [1,2]. Unfortunately, one stage coolers only could get to ~ 35 K and low temperature superconductor circuits need at least two stages to reach 4.2 K [3]. In addition, use of closed-cycle cryocoolers enables the user to utilize intermediate temperature levels for mounting auxiliary components such as interface circuitry or filters.

Successful operation of single flux quantum (SFQ) circuits in closed-cycle refrigeration systems have already been demonstrated by groups from USA, Japan, and Europe. For instance, Hashimoto et al. used a 4-K two-stage 1-W Gifford-McMahon cryocooler in order to demonstrate the function of SFQ 2×2 switch chip

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at 40 GHz [4]. Webber et al. used a Gifford-McMahon cryocooler for a DC voltage reference from Josephson junctions at the frequency of 20 GHz for fully automatic voltage standard system [5]. In the paper they report that when the chips are moved to a closed-cycle system from LHe, even without applying microwave power, some cells could not be biased to their operating current without going normal. They also demonstrate the function of SFQ receiver with about 11,000 junctions for 7.7 GHz satellite receiver with a power consumption of about 2 mW [6,7]. There is also a review on a 4-stage 4-K Stirling-type pulse-tube cooler by Lockheed-Martin from this group at Hypres that demonstrates the stability of cryocoolers for SFQ circuits and the advantage of multistage systems for mounting auxiliary components and HTS filters at different temperatures [8]. In the paper they demonstrate the operation of a 10-bit binary counter that contains fewer than 1000 Josephson junctions. Yoshikawa et al. also show the functionality of GM type cryocooler with high-throughput and high-bandwidth SFQ circuits. They demonstrate a flip-flop circuit with very good BER at 10 GHz frequency [9]. The circuit had 591 junctions with a bias current of 90 mA. Ortlepp et al. showed the cryocooler capabilities for precise measurements [10]. When we check the above reports about the cooling of superconducting chips by using closed-cycle refrigerator systems, we see that the circuits are either very small to face the cooling problems of the cryocooler systems or performance degradations have been faced in large circuits. In this paper, we report that one of the main limiting factors on the complexity of the chips to be tested is not the excess cooling power of the cryostat but power density of the chips and heat flux capacity of the system. Then we propose a packaging method to increase the heat flux capacity for large superconducting integrated circuits in a closed-cycle refrigerator system.

2. Cryocooler

For superconductor logic applications, a low-noise environment with sufficient cooling power at 4.2 K temperature is needed. We chose the pulse tube cooler that has one order of magnitude smaller vibration than GM type and no moving metal parts [4,11]. Therefore, it has longer maintenance-free operation period and lower vibrating noise. With 500 mW cooling power at 4.2 K it provides sufficient cooling power even after all the cabling, damping, and additional shielding.

To further reduce the vibration of the chip holder, mechanical damping braids were installed at the first and second stages as shown in Figure 1. The earth magnetic field can cause magnetic noise if the cooler has vibrating parts. These damping braids have reduced the vibration of the 4.2 K stage one order of magnitude, from 40 μm to less than 4 μm, but also reduced the second stage cooling power from 500 mW to 250 mW. Figure 1 shows the block diagram of the cryocooler. Temperature stability of 2nd stage at 4.2 K is about 10 mK over a 20-hour period. For the wiring we used 20 phosphor-bronze bias lines and 40 high frequency lines. From 2nd stage to 1st stage, coplanar transmission lines and from 1st stage to room temperature coaxial cables are used. High frequency lines consume about 16 mW from the excess cooling power of the 2nd stage. The chip-holder is placed inside a three-layered μ-metal magnetic shield which is connected to second stage. The magnetic shield brings the magnetic noise level down to $\sim$3 nT as measured by a fluxgate magnetic sensor. The thermal radiation from second stage, magnetic shield, and the joule heating from bias wires consume about 65 mW in total at second stage, which leaves about 185 mW of excess cooling power at the chip holder.

3. Problem definition

Even though the SFQ chips have extremely low power consumptions in orders of few mW, some joule heating occurs due to the on-chip bias resistances and causes a considerable power density. This heat dissipation is
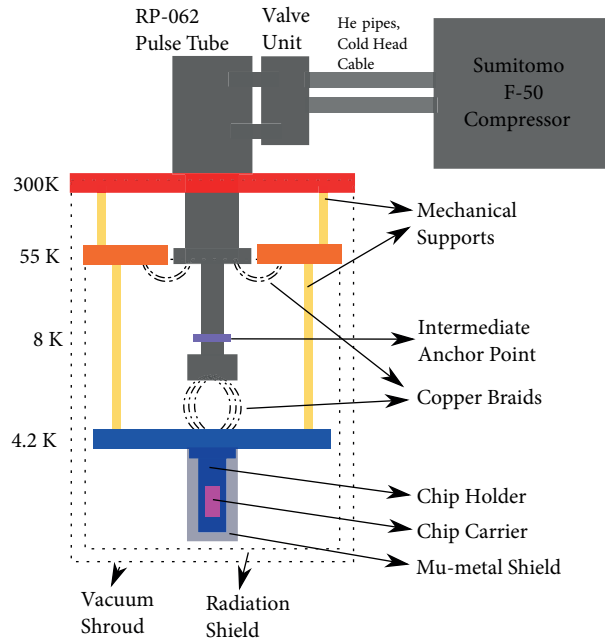
Figure 1. Schematic of pulse-tube cryocooler

mainly generated close to the surface of the chip. In LHe-based cryostats, the chip is in direct contact with the LHe, which results in a low thermal resistance between the chip surface and the cold medium. LHe has a heat flux capacity per area in the order of a few W/cm^2 [12]. Therefore, the removal of the heat due to the on-chip bias and shunt resistors in the circuits is sufficiently fast and there would be no thermal gradient between the circuits and cold medium.

However, in closed-cycle refrigerator systems, not only the cooling power is limited but also it is not easy to benefit from the available cooling power since heat flux capacity is much lower than that of LHe-based systems. The chip is connected to the copper holder by silver paste to insure good thermal contact. Since the chip is in the medium of vacuum, the heat generated on the surface of the chip could be removed either via the substrate (in our case it is silicon) or via the wire bonds that provide bias currents or I/O interface to the circuits. As the temperature approaches 4K, carrier density in the silicon substrate decreases and the heat conductance of the substrate would decrease as expected [13]. In addition, when the Niobium (Nb) material of the circuits becomes superconductor, the surface heat conductance of the chip would be low; therefore, the heat removal from the wire bonds at the sides of the chip would not be effective enough [14]. During our experiments that requires about 1 A bias current, we realized that we must overcome the power density problem of the chip in vacuum. Otherwise, positive feedback caused by the heat at bias resistors would force the temperature of the circuits to raise much higher levels than the critical temperature (T_C) of Niobium. This could damage the circuit and make the chip unusable.

As reported by Webber et al. a relatively large circuit with 4096 Josephson junctions could not be biased to their operating current without going normal even though the circuits operated in LHe and there is available excess cooling power in the system. They report that this anomalous operation could not be completely understood but they discussed some possible causes as the following: a) bulk chip temperature, b) macroscopic temperature gradients, c) heating on microscopic scale. To overcome problem a, they changed the adhesive bond to low temperature solder. For problem b, they tested the spring-finger contact resistances and saw that

the resistance values are negligible. For problem c, they have increased the dimensions of vias to provide better contact between the Niobium layers [5]. During our experiments, we faced similar problems and tried different types of epoxies and solders for chip to 4.2 K stage contact and found that silver paste is the best solution. We also measured the contact resistances of all the contacts including spring contacts and wire bond to chip contacts and reached a similar conclusion that they have negligible effect. Finally, we increased the size and number of vias for better heat conduction between the Nb layers. However, all these modifications had marginal effect in the cooling power limit of the chips.
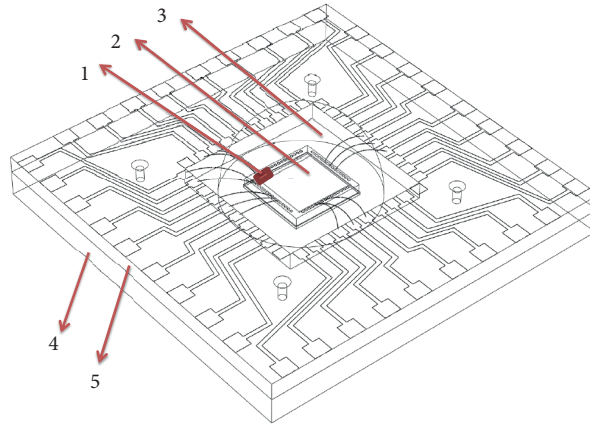

Figure 2. Chip packaging of the test circuit used for power measurements. 1) The series SQUID that work as temperature sensor. 2)The chip with circuit on it. Silicon substrate thickness is 0.3 mm. Active layers are on the top 2.7 μm 3) Epoxy at the surface of the chip. 4) Copper layer that the chip is connected to. 5) PCB with gold paths on it so we can wire bond the chip to it.

4. Quantitative investigation of the problem

To measure the amount of heat dissipation and heat removal capacity of the system, we used an on-chip test resistor with value 1.15 kΩ and a sample chip with single flux quantum circuits that can withstand 1 A under 2.5 mV bias voltage. We used two different wire bond diameters of 25 μm or 75 μm to see the effect of the heat removal through the wire bonds. On this chip, we also included series array of superconducting quantum interference devices (SQUID) with 300 DC-SQUIDs to monitor the surface temperature of the chip based on the I-V characteristic of the SQUID array. Figure 2 shows the package setup for the chip used in heat dissipation and removal measurements. The chip is directly in contact with the copper plate which is in contact with the cryostat second stage plate at 4.2 K.

As the temperature on the chip surface rises due to bias current, the I-V characteristic of the series SQUIDs would change accordingly. The relation between the critical current of the SQUIDs and the temperature of the chips is described in Eq. (1):

$$\frac{J_C\left(T\right)}{J_C(0)} = \left[1 - \left(\frac{T}{T_C}\right)^2\right]\sqrt{1 - \left(\frac{T}{T_C}\right)^4}, \tag{1}$$

where T is the Josephson junction temperature, T_c is the critical temperature of the superconducting material, $J_c(T)$ and $J_c(0)$ are the critical current densities of the Josephson junction at temperatures T and 0 K, respectively. The equation is the estimation of the temperature effect on London penetration depth and critical

magnetic field dependency of type II superconductor material. The I-V curve of the series DC-SQUID was measured with a data acquisition card and the temperature of the system were calculated based on Eq. (1) [15]. The critical current of the junctions at 4.2 K when there is no applied current is about 100 μA. With no applied bias current to the SFQ chip, we can consider that the chip surface and the SQUID temperature is at 4.2 K. Knowing that the critical temperature of our Niobium thin films are about 9.1 K, the temperature of the chip surface could be calculated based on the percentage drop of the critical current after biasing the SFQ chips.

With the application of 400 mA of bias current, the critical current level drops to 38% of the initial value at 4.2 K. A 38% drop in the critical current corresponds to a surface temperature of about 7.2 K based on Eq. (1). This result is not expected as the power consumption of the chip under 400 mA bias current is just 1 mW while the excess cooling power of the 4.2 K stage is much more than that. To find out the origin of this unexpected result, we investigated the heat generating parts of the system. Figure 3 shows the electrical resistances that bias current must go through to reach the circuit on the chip. The calculations for Joule heating are done based on this model. Since the power at first stage is very high, R_{B1} is neglected in calculations and half of the R_{B3} assumed to load the 4.2 K stage. The Joule heating that affects the temperature of the 4.2 K stage is due to $R_{B3}/2$, $R_{Contact}$, and $R_{Bond-wire}$ with a total resistance is about 0.92 Ω. This joule heating at the bias wires decreases the excess cooling power of the 2nd stage by about 36 mW to about 150 mW when 400 mA is applied from 4 bias wires. This value is still much higher than the power consumption of the SFQ chip which is about 2 mW.

To confirm the above calculations, we directly connected the bias wires to the ground plate of the system so that we can measure the Joule heating effect of the wires only. When applied 100 mA from each bias wire,
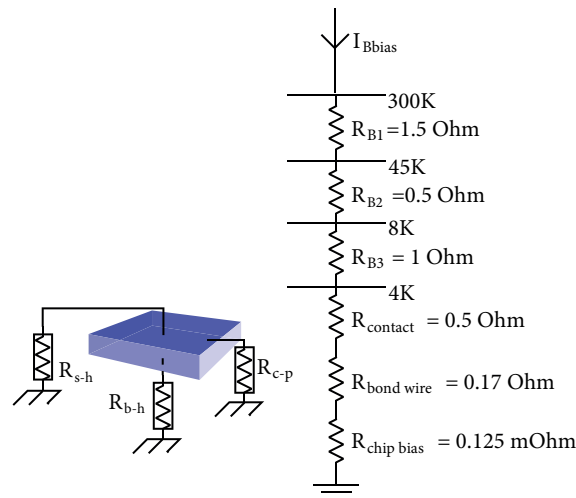

Figure 3. Left: the thermal resistance from the circuit on the chip surface to the environment. Right: Electrical resistance for one line (8 lines) of bias current path. R_{B1}, R_{B2}, R_{B3} are the portion of bias wire resistance from 300 K to 45 K, 45 K to 8 K, and 8 K to 4.2 K stages respectively. $R_{contact}$ is contact resistance between the chip holder and spring contacts, $R_{bond-wire}$ is the resistance of the bond wires from chip to chip holder, $R_{chip-bias}$ is the effective resistance on the chip due to the bias resistors. R_{P-H} is the thermal resistance between the bottom of the chip and copper plate, R_{C-P} is the thermal resistance of the bod wires from chip to chip holder, R_{S-H} is the surface the thermal resistance between the chip surface and copper plate. For the value of $R_{contact}$, when the spring contacts are first installed the contact resistance is about 10 mΩ. Over the operation of about 100 cycles some of the contacts may have a resistance as much as 0.5 Ω. An average value of 0.25 Ω is considered.

we get a Joule heating effect of about 9 mW from each wire as shown in Figure 4. For the case of 400 mA, total Joule heating is about 36 mW which is in line with the calculation. To see the effect of heating due to the circuit elements on the chip, we used a simple 1.15 kΩ on-chip resistor fabricated by the same foundry process to generate heat on the surface. The area of the resistor was about 1.05×10^{-3} cm^2. Then we measured the resistance in four-probe configuration [16]. Resistance of the Molybdenum around 4.2 K is quite linear with a sheet resistance of 1.2 $\Omega/\square$ in our fabrication process [17]. As the temperature of the on-chip resistor increases sharply, we understand that the temperature of the chip surface deviates from 4.2 K after about 2.5 mW input power as shown in Figure 5. At this point, the superconducting lines that connect the resistor to contact pads switch to normal state and hence a sharp increase of the resistance occurs. Since the bias current of the resistor at these powers are about 2.2 mA, Joule heating in the bias wires is negligible and the system has about 161 mW excess cooling power. However, the chip surface cannot be kept at 4.2 K while the 2nd stage of the cryostat is at 4.2 K.

Then we applied a bias current of 400 mA to the superconducting chip from 4 bias wires of 100 mA each while monitoring the temperature of the chip with the SQUID sensor. We see that the temperature of the chip is 7.2 K whereas the excess cooling power of the system is 17 mW at 4.2 K. Under a 400 mA bias current, power consumption of the chip is 1 mW.

Considering that the thermal contact of the chip to the 2nd stage is made by silver epoxy enabling a good thermal contact, both measurements of resistance and SFQ circuits are not expected results. Total heat generated on the bias wires and chip is much lower than the estimated excess cooling power of 161 mW and 132 mW respectively. Thus, we conclude that the main limit is not the excess cooling power but the power density of the devices under test. When we calculate the power density of the test resistor at 2.5 mW, we find it as 0.42 W/cm^2 at 9.1 K.

We think that after the power density of the chip exceeds the heat flux capacity of the cryocooler, heat is accumulated at the chip surface switching the superconducting Nb lines to normal state and under constant bias current, positive feedback occurs. Such problems are not observed by the groups that measure their superconducting chips in LHe bath as the heat flux capacity of LHe is much higher than a cryostat. In the literature, the heat flux capacity of LHe is reported to be about a few W/cm^2 [12].

5. Proposed cryo-packaging for increased heat flux capacity

As explained in the previous section, even a 2.5 mW power on the chip creates a thermal gradient between the chip surface and the second stage. We associate this result due to the limited heat flux capacity of the cryostat in vacuum. After some point, Niobium exits its superconducting state and causes a positive heating feedback under constant bias current and the chip to heat up rapidly. To increase the complexity of the devices that can be tested in a closed-cycle cryocooler environment, one option is to decrease the local power density on the chip and the other is to increase thermal conducting path of the chips to the environment.

One method was to increase the diameter of the bond wires so that the Joule heating in the bond wires would decrease and thermal link to the package would increase. Thus, we changed the bond wire diameters from 25 μm to 75 μm. As shown in Figure 4, the diameter of the bond wire has no considerable effect on the break point of the power vs. current line, and both breaks happened at the same current of about 40 mA. One clue that these break points are associated with the chip itself is that the curves that are obtained by directly bonding the wires to copper holder follow the usual joule heating characteristics as shown in Figure 4. After the break point, the cases that the wires are connected to the chip holder ground follow the profile of Joule
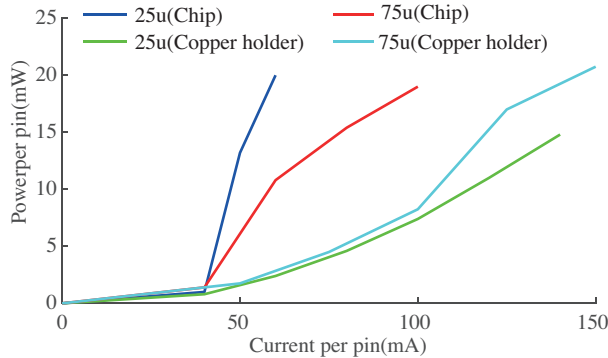
Figure 4. The Joule heating measurement results of a single 25 μm and 75 μm diameter wire versus bias current. Legend labeled with "Chip" is the case wire bonds are made to chip contacts and legend labeled with "Copper Holder" is the case wire bonds are directly connected to the ground without any chip in the system.
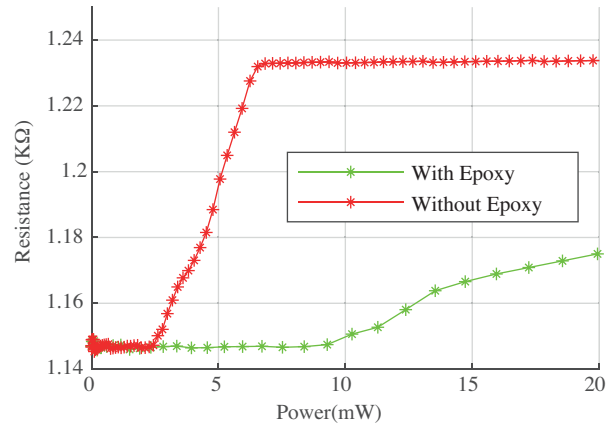

Figure 5. Resistance versus Temperature plot of the 1.15 kΩ Molybdenum resistor place placed on the chip. The area of the resistor is about 1.05×10^{-3} cm2. The points of sharp increase in the resistance correspond to the critical temperature of the on-chip Niobium wires. At 9.1 K, the resistance measurement shows not only the resistance of the test resistor but also the normal state Nb wiring.

heating ($\propto$ I^2) while the other case in which the bonds connected on chip surface are much sharper. This result demonstrates that the limiting factor of the bias current in an SFQ chip is the heat flux capacity of the system in vacuum not the Joule heating of the bias wires.

To solve this problem, we decided to cover the chip surface with a layer of epoxy to create a direct thermal link between the chip and the holder to decrease the chip surface to holder thermal resistance (R$_{S-H}$). For this purpose, we covered the chip with an epoxy that can withstand the 4.2 K temperature without cracking. The thermal expansion of the epoxy should not put stress on the wire bonds, the chip, or the junctions themselves. We tried GE varnish, Apiezon N grease, epoxy glass, and Stycast 2850 FT. GE varnish and Apiezon N grease's viscosity was not suitable to cover the wire bonds and surrounding of the chip and epoxy glass cracked after cooldown. Thus, we continued with Stycast 2850FT epoxy (Thermal conductivity: 1.25 W/m.K). Figure 6 shows the chip package for the cooler before and after applying epoxy on the surface.

Figure 7 shows the power density of the on-chip test resistor vs. resistor temperature difference from 4.2 K with and without epoxy. Temperature of the resistor is estimated as the following: resistance of the resistor is measured by using a Keithley 2604B sourcemeter with 4-point probe configuration under a bias current of negligible Joule heating that corresponds to 4.2 K (1146.9 Ω). Then the resistance value is measured at the bias current where the linearity of the resistance vs bias current is destroyed in Figure 5. This value corresponds to the chip temperature where the nearby on-chip Nb bias lines switch to normal state at 9.1 K (1147.4 Ω). Then these two points are interpolated to determine corresponding temperature values to the measured resistances under different bias currents and Joule heating. As shown in Figure 7, after the application of epoxy to the test resistor, heat flux capacity of the system for the same ΔT has increased about 5 times.

Then, we used the packaging method shown in Figure 6 to bias an SFQ logic circuit that contains about 10,000 Josephson junctions and requires 1 A bias current at 2.5 mV. We used 8 bias wires to supply the current for the bias resistors and monitored the chip temperature with the on-chip SQUID sensor. Measurement of Figure 4 was repeated with epoxy and the results shown in Figure 8 was obtained. As shown, the heat flux capacity
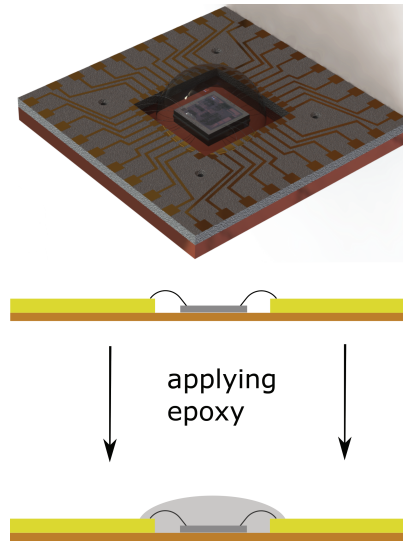
Figure 6. The chip before and after applying epoxy on it. The bottom plate (orange) is the copper plate and the top plate (yellow) is the PCB that contains the signal and bias lines. The chip is placed on the copper plate with silver paste for low thermal resistance between the copper plate and chip. The temperature of the copper plate kept constant at 4.2 K.

Table. Power density (PD) vs temperature gradients (ΔT) of the SFQ chip for the case of average and worst case power densities under 300 mA and 800 mA bias current.

Test device	Bias (mA)	PD (W/cm2)	ΔT w/o epoxy (K)	ΔT with epoxy (K)
SFQ chip (Average)	300	0.12 (⑤)	2 (▷)	0.03 (◁)
SFQ chip (Average)	800	0.95 (③)	4.8 (△)	0.1 (▽)
SFQ chip (R with worst PD)	300	0.38 (④)	1.55 (□)	0.7
SFQ chip (R with worst PD)	800	2.50 (②)	5	2.1 (◇)

and hence the current bias limit of the system increased substantially. Without the epoxy, the maximum bias current that we could apply while the chip remained around 4.2 K was about 300 mA (8*38 mA) and after the application of epoxy, the maximum bias current was about 0.8 A (8*100 mA).

In the chip, there are 2159 logic cells. Total number of bias resistors is 3530, ranging from 5.7 Ω to 37 Ω. Total area of the bias resistor layers is 3.7×10^{-5} cm^2. For the case of 800 mA bias current, average power density of the chip is 1.39 W/cm^2 at a ΔT of 4.8 K and 0.1 K for the case of without and with epoxy respectively (indicated with $\triangle$ and $\triangledown$ in Figure 7 and Table 1). However, just observing the average power density of the bias resistors may be misleading since the local power densities may be higher at some locations. The bias limit of the SFQ chip is mainly determined by these bias resistors due to the local heating and positive feedback. Thus, we calculated the power density distribution of the on-chip resistors for 300 mA and 800 mA as shown in Figure 9. As the limiting factor, we consider the resistor with highest power density. The worst case power densities for 300 mA and 800 mA are calculated to be 0.38 W/cm^2 (ΔT= 1.55 K without epoxy ($\square$) and 0.7 K with epoxy) and 2.5 W/cm^2 (ΔT= 5 K without epoxy and 2.1 K ($\lozenge$) with epoxy) as indicated in Figure 7 and Table 1. In the figure, we also added the heat flux capacity of the boiling liquid Helium for reference [12]. As shown, heat flux capacity of LHe is about an order of magnitude higher than that of the sample in vacuum even with epoxy.
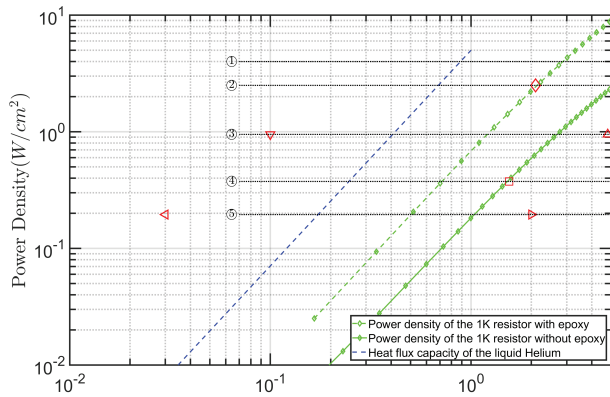
Figure 7. Measurement of heat flux capacity of the cryostat for the 1.15 kΩ resistor with and without epoxy. Dashed line denotes the heat flux capacity of the boiling liquid Helium for reference [12]. ①: Average PD of the SFQ chip under 1 A bias current. ②:PD of the resistor with the highest PD in the SFQ chip at 800 mA bias ③:Average PD of the SFQ chip under 800 mA bias current. ④:PD of the resistor with the highest PD in the SFQ chip at 300 mA bias ⑤:Average PD of the SFQ chip under 300 mA bias current. Markers in the plot are explained in Table 1.

Figure 8. The power consumption graphs per current of each pin by different coverings of the chip.

6. Conclusion

As Helium is getting rarer, closed-cycle refrigerator-based systems have a good potential to replace the LHe systems in research and commercial facilities. In this work, we report the analysis and efforts to increase of the heat flux capacity of a closed-cycle refrigerator system in vacuum for superconducting integrated circuit testing. Experimental results show that the heat flux capacity in vacuum is the main limiting factor of the system even though there is excess cooling power at the 4.2 K plate. Application of epoxy to the chip surface increases the heat flux capacity of the system about 5 times. Hence, the maximum bias current of the circuits that can be tested has increased from 300 mA to 800 mA in our specific case. Even after epoxy packaging, the heat flux capacity of a closed-cycle system is about an order of magnitude lower than that of LHe bath. Thus, to further increase the complexity of the devices that can be tested in a closed-cycle refrigerator system, designers should also keep in mind the power density of the bias resistors and keep it below the heat flux capacity of the test setup. In our case, 0.1 W/cm^2 without epoxy and 0.4 W/cm^2 with epoxy would be a reasonable value. The proposed method is not only applicable to large cryogenics circuits but also to circuits with small bias currents implemented close to sensitive devices such as cryo-detectors and qubits.
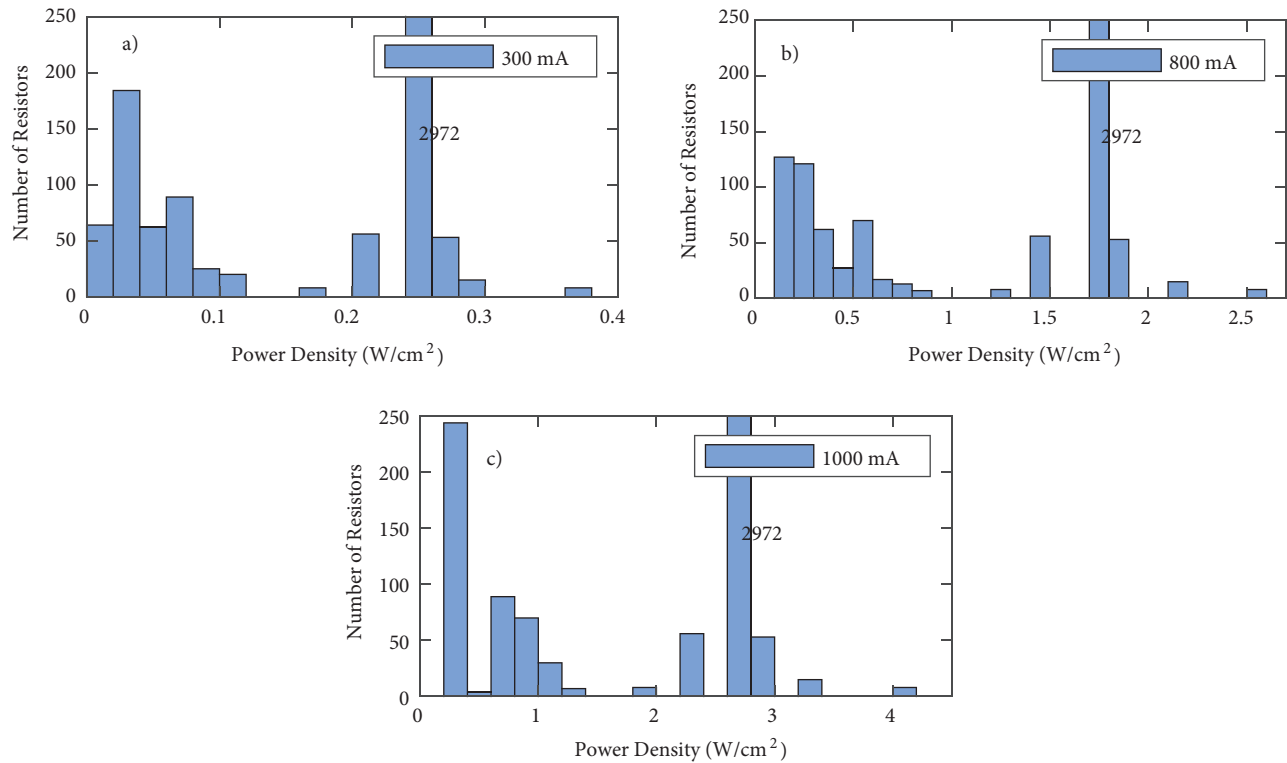
Figure 9. Power density distribution for the case of 300 mA, 800 mA, and 1000 mA bias currents. Highest count is 2972; however, y scales are limited to 250 for clarity, and 1000 mA is the design value for the SFQ chip.

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