Turkish Journal of Electrical Engineering & Computer Sciences

http://journals.tubitak.gov.tr/elektrik/

Research Article

Turk J Elec Eng & Comp Sci
(2019) 27: 4456 – 4471

doi:10.3906/elk-1906-153

An optimized harmonic elimination method based on synchronized microcontroller architecture

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Received: 21.06.2018 • **Accepted/Published Online:** 29.03.2019 • **Final Version:** 26.11.2019

Abstract: This paper proposes an optimized synchronous PWM method for harmonic elimination in a quasi square wave inverter. The synchronized PWM method enables online harmonic computation and PWM pulse generation in a multitasking digital controller to eliminate lower order harmonics. The multitasking digital controller reduces the look-up table requirement and helps in realizing efficient implementation to eliminate dominant harmonics. This method offers a simple scalable solution for combined fifth and seventh harmonic elimination using two low-cost eight-bit PIC microcontrollers (PIC18F4550, PIC18F452). Experimental results are demonstrated for a single-phase three-level inverter. The proposed method achieves 90% reduction of fifth and seventh harmonic components from a quasi square wave inverter output.

Key words: Pulse width modulation, synchronized architecture, harmonic elimination, fast Fourier transform

1. Introduction

Inverters form an important part of power electronic converters. The output voltage of an inverter is controlled with the pulse width modulation (PWM) technique. The performance of an inverter is influenced by the choice of PWM scheme used. PWM schemes can be classified as carrier-modulated PWM, space vector PWM, and programmed PWM. The programmed PWM scheme optimizes the objective function to eliminate the unwanted harmonics present in the output spectra. Selective harmonic elimination schemes were initially proposed in [1]. The works reported in [1–8] involve solving numerous transcendental equations based on the concept of Fourier series. The majority of the methods reported for harmonic elimination involve a static computation approach. The solutions are often determined offline and stored in a look-up table. The elimination of low order dominant harmonics present in output spectra reduces current ripple and improves overall performance. The choice of elimination is implemented for line-to-line voltage or line-to-neutral voltage. A regular sampled PWM implementation using an algebraic equation for harmonic elimination with a microprocessor was discussed in [9]. An extensive look-up table and interpolation-based approach for quasi square continuous control were presented in [10]. The advent of digital components such as microprocessors and high-speed memories have opened the way for advanced control devices based on novel algorithms for elimination of harmonics in the output voltage. Microprocessor-based control is used for efficient implementation of PWM strategies in real time to reduce cost and hardware burden. Several alternative microprocessor implementations for the regular-sampled harmonic elimination PWM technique were discussed in [10–12]. The harmonic elimination angles computed are stored in

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Erasable Programmable Read Only Memory (EPROM). The required elimination angles are fetched from the look-up table based on the desired frequency. The subharmonics and harmonics were eliminated using a direct look-up table method with a processor in [11]. The discrete frequencies for the look-up table are computed in this approach. Values of the samples for the corresponding frequency are to be stored in Read Only Memory (ROM) to achieve accuracy. Software timing critical loops are also used for real-time sampling, which prevents the processor from performing other tasks. A real-time implementation of harmonic elimination of selective harmonic elimination for MLI was reported in [12]. Loop unrolling and static profiling strategies were discussed in [13–16]. An improved selective harmonic elimination with online harmonic elimination was discussed in [17]. A selective harmonic elimination PWM technique-based hybrid asynchronous PSO–Newton–Raphson (APSO-NR) algorithm for the elimination of undesired harmonics in a cascaded H-bridge multilevel inverter was discussed in [18]. The work reported in [19] defined a fitness function for applied optimization techniques in terms of lower order harmonic elimination. The work in [20] investigated the critical parameter design technique for a cascaded H-bridge (CHB) with selective harmonic elimination (SHE)/compensation (SHC) for single-phase systems. Several single-phase full-bridge converters connected in series with quasi square wave converters to eliminate harmonic voltages from the net output voltage of a hybrid converter were discussed in [21].

This paper presents an optimized synchronous PWM method for harmonic elimination with an eight-bit PIC microcontroller, which aids the controller in performing multitasking operations involving software timing critical loops simultaneously. The method improves the ease of implementation and speed of execution and reduces memory storage. The proposed method enables an eight-bit microcontroller to perform online harmonic computation of fifth and seventh dominant harmonics and to generate PWM patterns for online harmonic elimination. This work provides detailed analysis of the proposed synchronized microcontroller architecture method for optimum harmonic elimination. The method is validated with a single-phase three-level NPC inverter. Section 2 explains the motivation behind the proposed architecture. Mathematical analysis is discussed in Section 3. Section 4 describes the proposed synchronized microcontroller architecture. The implementation details are mentioned in Section 5. Section 6 explains experimental results. Section 7 concludes the paper.

2. Motivation

Numerous power electronic devices are used for enhancing power quality in industrial applications. The dominant low order harmonics associated with power electronic devices must be reduced to improve the quality of the waveform. In selective harmonic elimination methods, the harmonics are reduced with precomputed angles stored with a microcontroller. The standard methodology in offline computation involves prestoring of required PWM switching patterns in the memory of the processor. The method of storing sample values is highly inefficient. A new set of gating signals needs to be recomputed each time for a change in the phase of the waveform. These disadvantages are overcome by the implementation using an online computation approach. The variation in harmonics needs to be computed and eliminated in real time. Hence, real-time computation is required to achieve harmonic elimination in real time. In most online methods the control algorithm is implemented on a fixed frequency waveform. Computing overhead for the voltage control algorithm is incurred for each harmonic to be eliminated in the phase voltage waveform. The real-time computation should satisfy the criteria of computation overhead, data storage, and hardware requirements in a cost-effective manner. The task can be segregated in a single PIC microcontroller. A single microcontroller is assigned for computation of harmonic content and generation of corresponding gate signals for the phase voltage waveform to cancel the harmonic contents. The reduction of the response time for detecting multiple harmonic contents,

storage management for the look-up table, and real-time computation for software timing critical loops form a challenging requirement to be implemented with a microcontroller. This paper aims to implement an optimized computation algorithm for performing online dominant harmonic elimination with a PIC microcontroller, which optimizes memory and integrates multiple software timing critical loops. The method avoids solving nonlinear transcendental equations but uses trigonometric functions stored in the look-up table.

3. Mathematical analysis

The mathematical analysis of the proposed method is presented based on a quasi square waveform as shown in Figure 1. The quasi square wave output varies from A to –A over an interval of T. The waveform is free from even and triplen harmonics because of the symmetry. The odd harmonics are present in the waveform. The harmonic content can be expressed as the sum of sines according to Fourier theory. This provides analysis of the quasi square wave of n degrees of conduction. The amplitude and phase of the corresponding harmonic contents can be computed with the help of Fourier analysis. The Fourier series component of a pulsed waveform of width T/2 with an amplitude of A as shown in Figure 1a can be expressed as below:

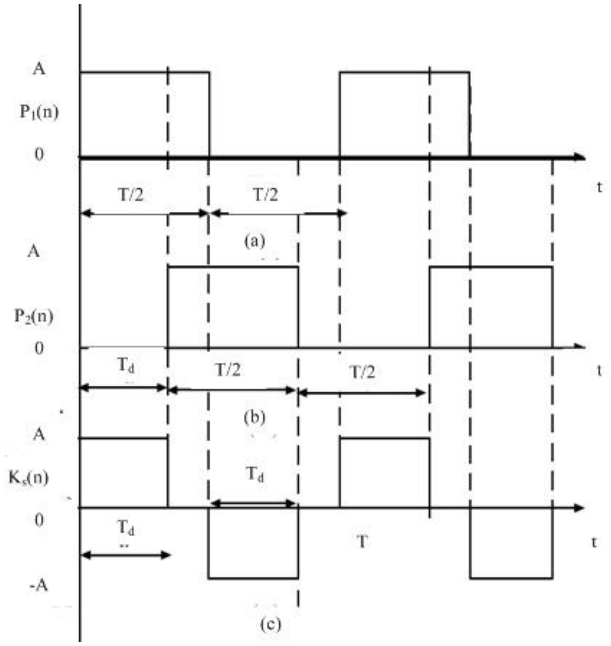


Figure 1. (a) Pulsed waveform; (b) shifted pulse waveform; (c) quasi square waveform.

$$\begin{aligned} P_1(n) &= \frac{-A\jmath}{\pi n}; n = odd \\ &= 0; otherwise. \end{aligned} \tag{1}$$

The shifted pulsed waveform as shown in Figure 1b can be described by Eq. (2):

$$P_2(n) = \frac{-A\jmath}{\pi n} e^{-\jmath n\omega_0 T_d};\ n = odd. \tag{2}$$

The difference between the pulsed waveform and shifted pulsed waveform in Figure 1a and Figure 1b results in a quasi square output as shown in Figure 1c. T_d represents the shifted duration from the origin. The net

difference of Eqs. (1) and (2) provides the Fourier series components of a resulting square wave of width T_d with an amplitude A. The quasi square wave analysis indicates that the components of the Fourier series are in exponential form with time shift (T_d):

$$K_s(n) = P_1(n) - P_2(n), \tag{3}$$

$$K_s(n) = \frac{-A}{\pi n}(sin(n\omega_0 T_d)) + \jmath(1 - cos(n\omega_0 T_d)). \tag{4}$$

For 120 degree conduction the value of T_d is T/3. Eq. (4) can be expressed as follows:

$$K_s(n) = \frac{-A}{\pi n}(sin(\frac{2 * \pi * n}{3}) + \jmath(1 - cos(\frac{2n\pi}{3})). \tag{5}$$

The above theory can be illustrated by an example. The quasi square wave is generated using a PIC microcontroller experimentally with a conduction period of 6.67 ms, which corresponds to 120 degree conduction. The conduction duration for 120 degrees is T/3. The square wave amplitude can be further evaluated as:

$$|K_s(n)| = \frac{A}{\pi n}\sqrt{2 - 2cos(\frac{2n\pi}{3})}. \tag{6}$$

Similarly, the phase of the waveform can be obtained from the following equation:

$$\theta_{KS}(n) = tan^{-1}\left(-\frac{1 - cos(n\frac{2*\pi}{3})}{sin(n\frac{2*\pi}{3})}\right). \tag{7}$$

The generalized expression of θ for the nth component is obtained from Eq. (7).

The magnitude of the fifth and seventh harmonics is evaluated from $|K_s(n)|$ by replacing n = 5 and 7, respectively:

$$|K_s(5)| = A\frac{0.346}{\pi}, \tag{8}$$

$$|K_s(7)| = A\frac{0.2471}{\pi}. \tag{9}$$

4. Proposed synchronized microcontroller architecture

The block diagram of the proposed synchronized microcontroller architecture is shown in Figure 2. The frame (control signals) of the compensator should be synchronized with the frame (control signals) of the main inverter. This is achieved by the generation of synchronization signals by the main inverter. The main inverter produces encoded gating signals to indicate the output level. Samples are taken at a regular interval of 1.2 ms for 16-point real FFT computation. The proposed method involves online computation of the magnitude of the dominant harmonic in every cycle but phase detection for the corresponding harmonic frequency is computed once during initialization. As real FFT produces complex conjugate FFT coefficients, only dominant fifth and seventh harmonic computation is achieved with 16-point real FFT implementation.

Higher order harmonics can be further computed and compensated using a 64-point real FFT algorithm, which requires a high-end processor for higher sampling rate and higher data storage. Compensator signals are

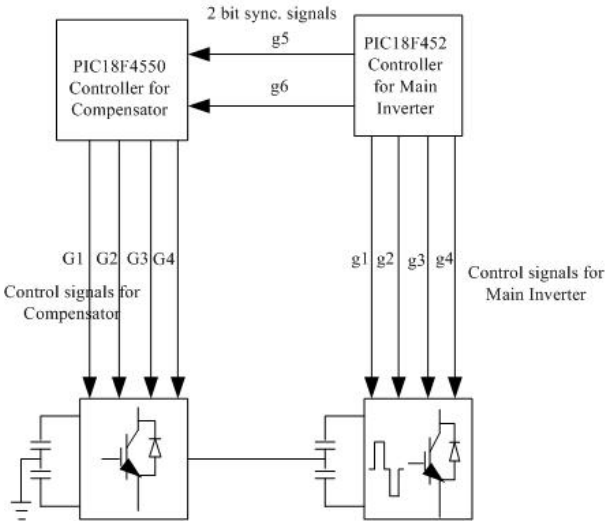


Figure 2. Proposed synchronized microcontroller architecture.

computed for the corresponding harmonics after the amplitude and phase are computed. The output of the compensator is fed to the input of the inverter with the proposed topology. Compensator signals for the first 14 samples are generated in a direct manner with microcontroller delay routines. In the case of the processor platform, the approach to implement this architecture combining the two software timing critical loops running on the same microcontroller is a very difficult task while meeting real-time requirements of applications. This is solved in the following manner by the proposed topology. The optimized timing for this method is shown in Figure 3. Sixteen samples are taken at a regular interval of 1.2 ms. The compensator signals corresponding to the first 14 sampling instants are generated in a direct manner with microcontroller delay routines. Compensator signal generation for the 15th and 16th samples coincides with the second loop, which is FFT computation and signal generation. Compensator signals for the 15th and 16th samples are generated in an indirect manner with the help of loop unrolling and a static profiling strategy while running FFT computation on the microcontroller platform.

There are two basic parts in the FFT computation algorithm for quasi square applications in real time. Samples need to be collected at a regular interval of 1.2 ms for computation of compensator values with 16-point FFT. The second part deals with the compensator signal generation for the corresponding compensator values generated in the first loop. The 16-point real FFT is implemented in real time in an optimized fashion, which needs nine integer multiplications and eighty integer additions. The phase of the corresponding harmonic signal is computed by exploiting the half-wave symmetry of the waveform. The pulse generation for compensator switches for a single cycle of FFT computation is shown in the timing diagram in Figure 3. The g5 and g6 signals represent the synchronized pulse generated and G1, G2, G3, and G4 represent the compensator gate pulses. The computation of the bits should be based on the conditions given in Table 1 and the durations are computed by an eight-bit PIC microcontroller using the control algorithm.

4.1. Description of power circuit configuration

The three-level neutral point clamped (NPC) voltage source inverter (VSI) topology has the advantage of not providing potential at the midpoint (floating neutral) of the capacitors under zero voltage conditions. Therefore,

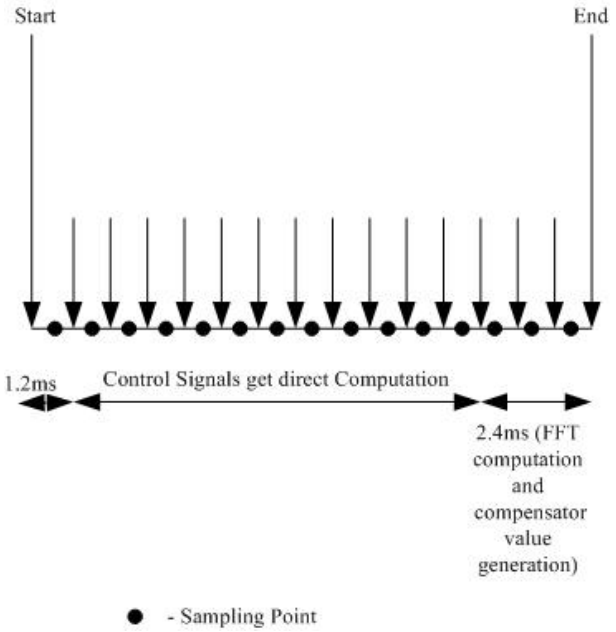


Figure 3. Timing diagram for the proposed method.

Table 1. Gating signals generation.

Gating signals	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
g5	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
g6	0	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0
G1	0	0	1	1	0	0	1	0	1	1	0	0	1	1	0	1
G2	0	0	1	1	0	0	1	0	1	1	0	0	1	1	0	1
G3	1	1	0	0	1	1	0	1	0	0	1	1	0	0	1	0
G4	1	1	0	0	1	1	0	1	0	0	1	1	0	0	1	0
Duration (microseconds)	7	18	8	17	18	15	47	42	7	18	8	17	18	15	46	42

a three-level NPC VSI topology for the main and compensating inverter is considered in this work to implement the proposed synchronized architecture for dominant harmonic elimination. The compensating inverter is connected in cascade with the main inverter. The addition of the antiphase harmonic voltage components generated by the compensator takes place in this configuration. The hardware-in-the-loop addition with the compensator reduces the corresponding harmonics generated in the main inverter. Multiple harmonic frequencies can be computed using a single compensator and added at the common nodal point as shown in Figure 4. This addition gives an added advantage of providing filter-less operation in circuits. Each compensator needs a single driver configuration. The main inverters are fed from a single DC supply while the compensating inverters are supplied from another DC supply. The proposed method removes the requirement of separate capacitors for each harmonic component and combines multiple harmonic frequencies with a single compensator. The computation and elimination of the harmonic components are achieved in real time.

5. Design implementation

Design implementation of the method is realized in the following stages.

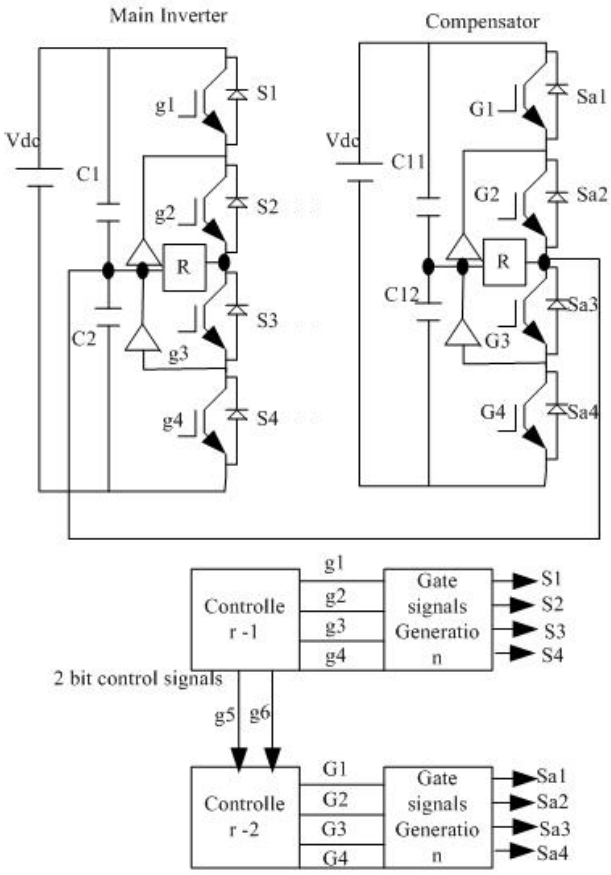


Figure 4. Power circuit diagram in the proposed method.

5.1. Frame synchronization

The output of the main inverter and the corresponding compensator output has to be synchronized to eliminate dominant harmonics. Start of frame (SOF) is defined as the instant when 00 to 10 transitions are detected in the two-bit synchronizing signals. The compensator waits for SOF detection after the generation of compensator pulses. This delay is reduced to the smallest extent and delay is negligible. Hence, the overhead of synchronization is at bare minimum. The same two-bit synchronizing signals are provided to all the compensators corresponding to the same phase. This can be illustrated with an example. The pulse generation for compensator switches for a single cycle of FFT computation follows the logical conditions as provided in Table 1. Logical condition 1 corresponds to ON duration and 0 corresponds to OFF duration of a switch. The ON time duration mentioned in Table 1 in microseconds corresponds to the pulse width for the corresponding logical condition. The switching sequence occurs in accordance with the logical conditions specified in Table 1. The switching pattern shown in Table 1 is the characteristic sequence obtained from online computation and therefore a generalized sequence is determined from this table. g5 and g6 signals represent the synchronized pulse generated by the main inverter and G1, G2, G3, and G4 are compensator gate pulses. The computation of the bits should be based on the conditions mentioned in Table 1 and their durations are computed by an eight-bit controller using the control algorithm. The duration of pulses in Table 1 corresponds to the compensator voltage in the timing diagram. The durations of pulses generated by the compensator voltage are shown

in Table 1 in the second column. A duration of 18 μ s is shown in the column and logical conditions of G3 and G4 are one and one, respectively. The lower switches, G3 and G4, are turned on and the applied voltage is negative as seen from the second voltage pulse of the compensator voltage in the timing diagram. G1 and G2 are turned on for 8 μ s and positive voltage is generated as seen from the third voltage pulse in the timing diagram. The time period for the switching pulse is 1.25 ms as 16-point FFT is used. The complete design implementation of the proposed method is shown in Figure 5. The generation of two-bit synchronized signals as shown in Figures 6a and 6b are obtained from the experimental prototype. Figure 6a shows the compensator pulses and Figure 6b shows the two-bit synchronizing signal along with the compensator signals.

5.2. Computation of memory requirement

Phases of the corresponding harmonic components are determined during the initialization phase and the resolution is limited to an integer degree. A sampled sine wave is shown in Figure 7a. Memory requirement is computed with the help of the look-up table and 360 entries are stored for each harmonic for the corresponding 360 degrees. Each value consists of 8 bits. The value stored is 100 $\sin(\omega t)$ + 100. This approach reduces the look-up table size and the value can be stored with an eight-bit value. The same strategy is used for floating-point computing arithmetic to reduce the cache data requirement. The look-up table is referenced 32 times to generate the final compensator value with the detected phase value corresponding to the harmonic component to remove dominant harmonics with 16-point FFT. The fundamental equation of the FFT can be obtained from the DFT approach. The DFT of any wave can be obtained as:

$$X(k) = \sum_{0}^{N-1} \left(x(n) \left(cos(\frac{2\pi nk}{N}) + \imath sin(\frac{2\pi nk}{N}) \right) \right). \tag{10}$$

For the 16-point approach N = 16 and hence Eq. (10) can be written as follows:

$$X(k) = \sum_{0}^{15} \left(x(n) \left(cos(\frac{2\pi nk}{16}) + \imath sin(\frac{2\pi nk}{16}) \right) \right). \tag{11}$$

. Hence, (360 $\times$ 2) bytes are needed for look-up table storage for 16-point dominant harmonic removal and (360 $\times$ 9) bytes are needed for look-up storage of 64-point harmonic removal. x(n) indicates the signal value at the sampling instants.

5.3. 16-Point FFT optimization

The coefficients of 16-point real FFT are stored in the look-up table. Integer optimization is used to implement 16-point real FFT. The integer dimension is limited to two bytes to the port application in an eight-bit micro-controller. No floating point variables are used. The 16-point FFT is implemented using nine multiplications and eighty additions.

A single active compensator is used to eliminate the corresponding fifth and seventh harmonics present in the quasi square output waveform. The active compensator control signals are generated using the two synchronizing signals from the main inverter. The microcontroller computes and generates the corresponding fifth and seventh harmonic control signals. The variations of harmonic amplitude for different DC bus voltage and harmonic values are plotted and observed. It can be seen that the relationship shown in Figures 7b and 7c are linear. The magnitude and phase variation of the fifth and seventh harmonics are shown in Figure 7d. This relationship is taken into account for PWM computation.

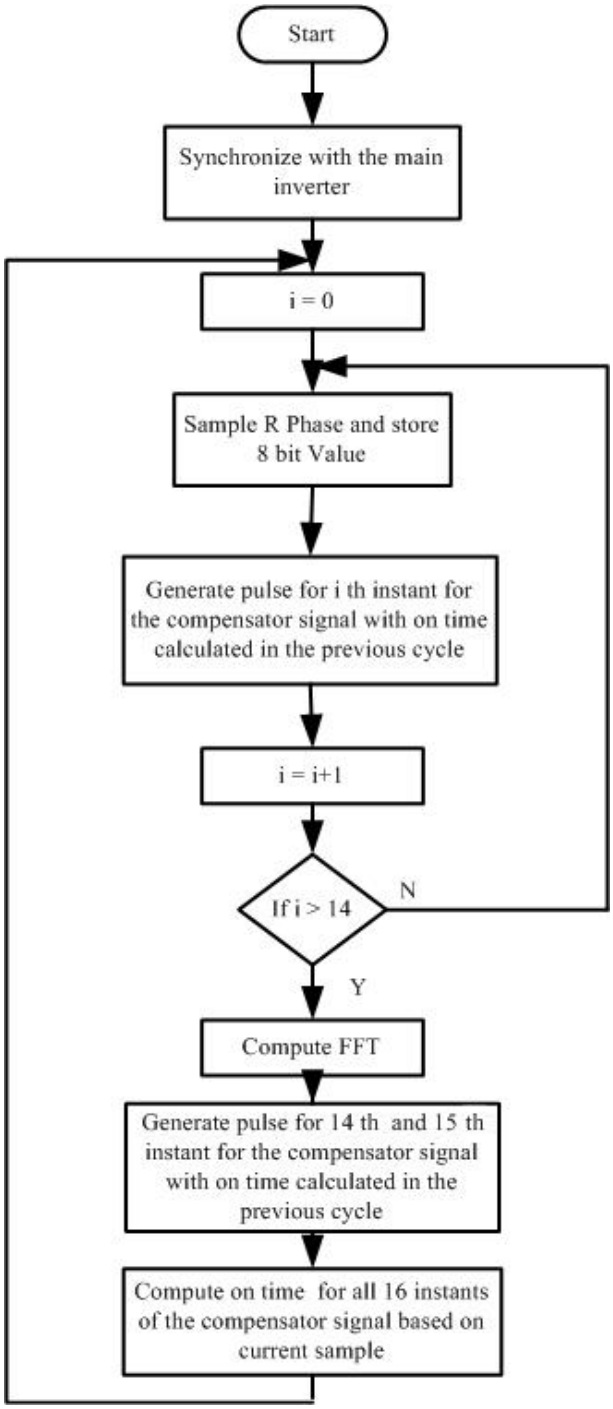
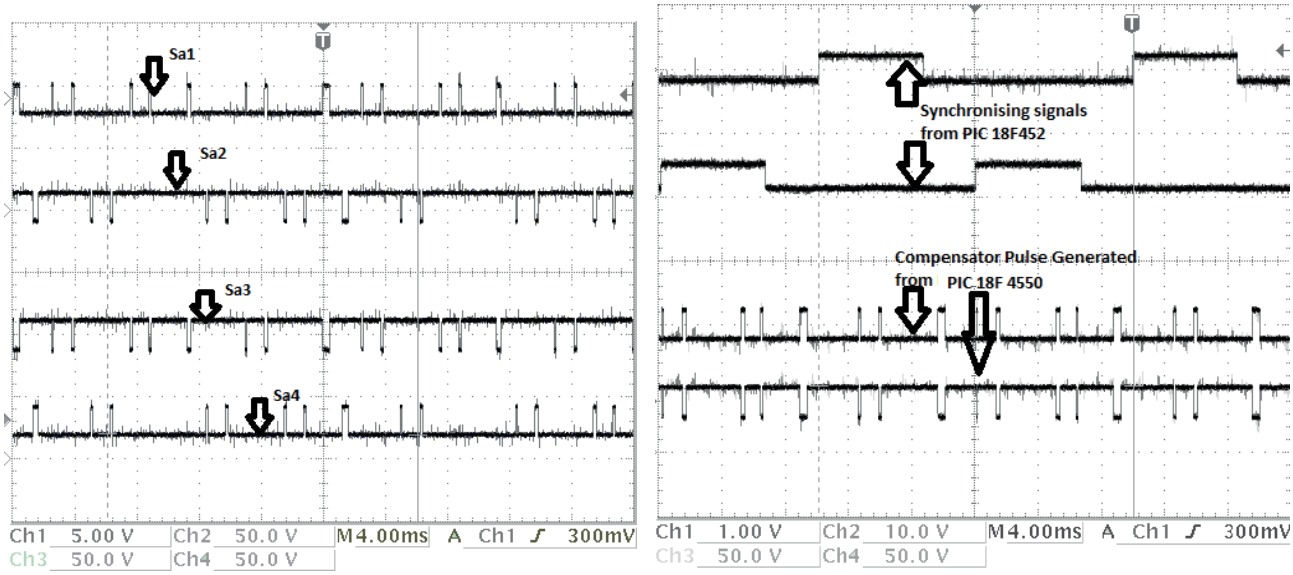


Figure 5. (a) Compensator pulse; (b) Synchronizing pulses and compensator signal generation.

5.4. Phase detection

Phase detection is done initially once during the initialization as per Eq. (7) from FFT coefficients. The knee of the tangent curve is around 72 degrees. Hence, arctan is used for calculating the phase as the maximum phase is limited to 72 degrees (360/5) in this case.



(a) (b)

Figure 6. Plots (a) Sampled sine wave; (b) variation of harmonic amplitude plot with harmonic magnitude; (c) variation of harmonic amplitude plot with harmonic magnitude with DC link voltage; (d) variation of magnitude and phase of fifth and seventh harmonics with variation in width of quasi square wave.

5.5. Integration of multiple software timing critical loops

ON time of the PWM pulses is computed by the controller in real time and the corresponding PWM pulses need to be generated simultaneously. This is normally achieved by the hardware PWM module available with the microcontroller. The number of hardware PWM modules is restricted to two in an eight-bit microcontroller. It is a challenging task to integrate multiple software timing critical loops with a microcontroller. A novel idea is incorporated in the proposed approach. First, fourteen compensator pulses are generated with delay routine in busy wait mode. The last two pulses for the 15th and 16th samples are generated in the following manner. Static profiling is used to track computation time and code hooks are placed with a step size. Code hooks are located at specified points to generate the compensator pulses. A loop unrolling technique is used to provide space for code hooks. An example of a code hook is given below.

if (15th pulse instant $<$ current instant)

set the compensator output voltage to capacitor midpoint voltage (ground)

6. Simulation and experimental results

The PSpice simulation and experimental results are presented in this section. The simulation output voltage waveform of the main inverter, compensating inverter, and compensator inverter along with their corresponding FFT spectra are shown in Figure 8. Figure 8a shows the quasi square waveform and Figure 8b represents the FFT spectrum of Figure 8a. Figure 8c shows the compensator output and Figure 8d shows the corresponding FFT spectrum. Figure 8e shows the compensated output and Figure 8f represents the corresponding FFT spectrum.

The experimental analysis is verified on a prototype of a three-level NPC inverter as shown in Figure 9. The hardware arrangement is done on a single-phase three-level neutral point clamped inverter by using a

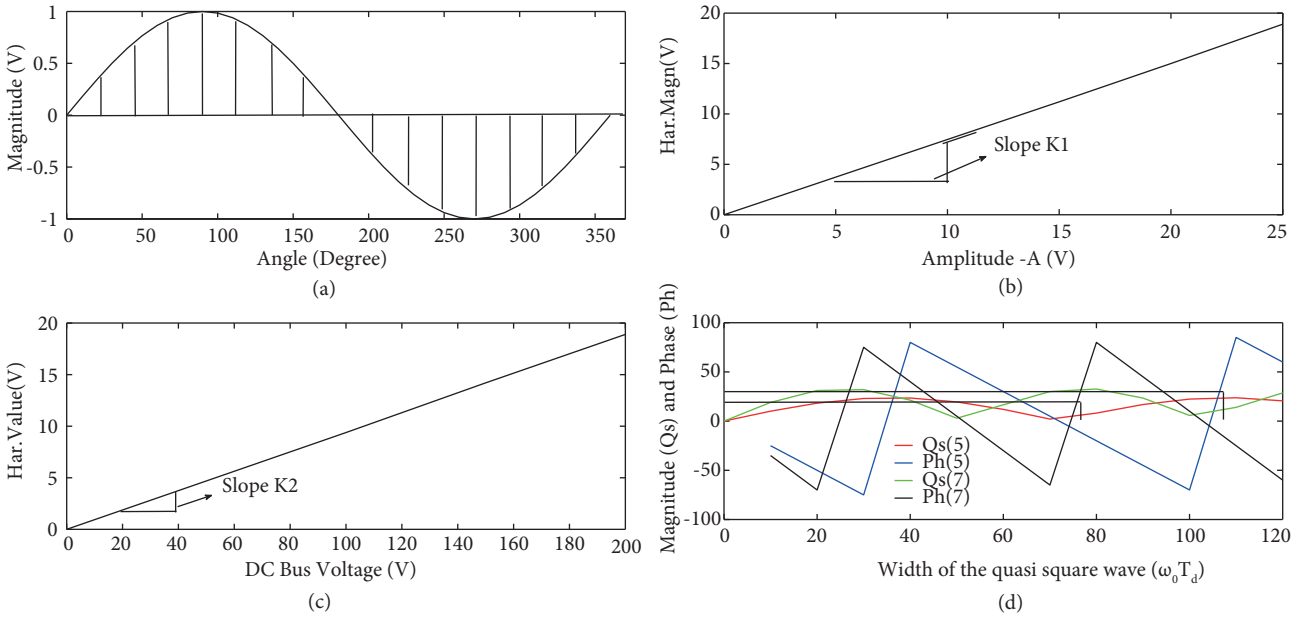


Figure 7. Flow chart showing FFT computation and compensator value generation.

resistive load and applying a DC link voltage up to 100 V. The resistive load is used in the experimental setup with various values. PIC 18F4550 is used as a low-cost eight-bit controller to compute FFT and to generate compensating pulses for dominant lower order harmonics. The PLL enabling option in the microcontroller makes FFT computation simple and generates synchronized pulses. PIC 18F452 is used as a controller for the main inverter. The synchronizing pulses generated by the controller for the main inverter are sent to the controller for the compensator for computing the FFT. The experiment is carried out using the proposed synchronized microcontroller architecture for fifth and seventh harmonic elimination together. The synchronization of signals between the main inverter and the compensator is achieved and the corresponding compensator signals are generated. The proposed method is verified on a three-level NPC topology as discussed previously. The output of the main inverter is a quasi square wave and contains dominant lower order harmonics. The experimental waveforms of the main inverter, compensating inverter, and compensator inverter along with their respective FFT spectra are presented in Figures 10–12. Figure 10a demonstrates the phase voltage of the main inverter and Figure 10b represents the FFT spectrum, showing the magnitude of lower order harmonics. Figure 11a shows the compensator voltage and the corresponding spectrum is depicted in Figure 11b. Figure 12a illustrates the output voltage of the main inverter after compensation and the FFT spectrum is given in Figure 12b. It is observed that the corresponding FFT spectrum demonstrates the reduction in the dominant fifth and seventh harmonics to a significant level. The comparative spectrum analysis in Figure 10b and Figure 12b of the compensated waveform shows reduction in the values of the fifth and seventh harmonic components.

The percentage harmonic reduction is achieved by normalized computation as per Eq. (12). The percentage reduction is computed as:

$$H_R = \frac{(M_N - C_N)}{M_N}, \tag{12}$$

where H_R is harmonic reduction, M_N is the normalized harmonic value of the main inverter, and C_N is the ormalized harmonic value of the main inverter after compensation.

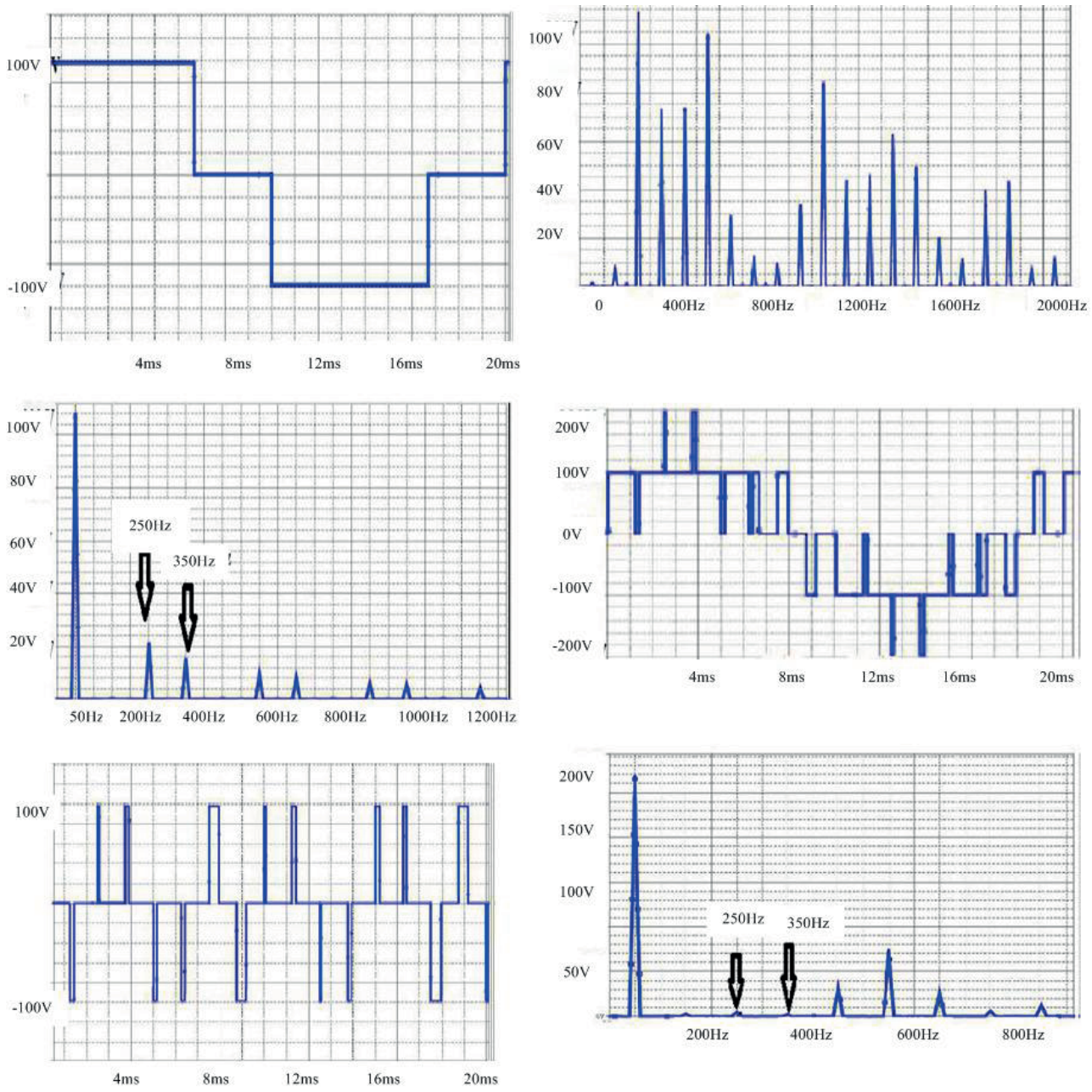


Figure 8. Simulation results: (a) main inverter waveform; (b) FFT spectrum of main inverter; (c) compensating inverter waveform; (d) FFT spectrum of compensating inverter; (e) main inverter waveform after adding compensating inverter; (f) FFT spectrum of main inverter with addition of compensating inverter.

The normalized harmonic value, which is the ratio of current value to the fundamental, is used for comparison. The normalized value remains the same for different ranges of DC bus voltage values and load conditions and the computation values in Table 2 show a reduction of 90% in magnitude. Total harmonic distortion (THD) is the summation of all harmonic components of the voltage or current waveform compared against the fundamental component of voltage or current wave:

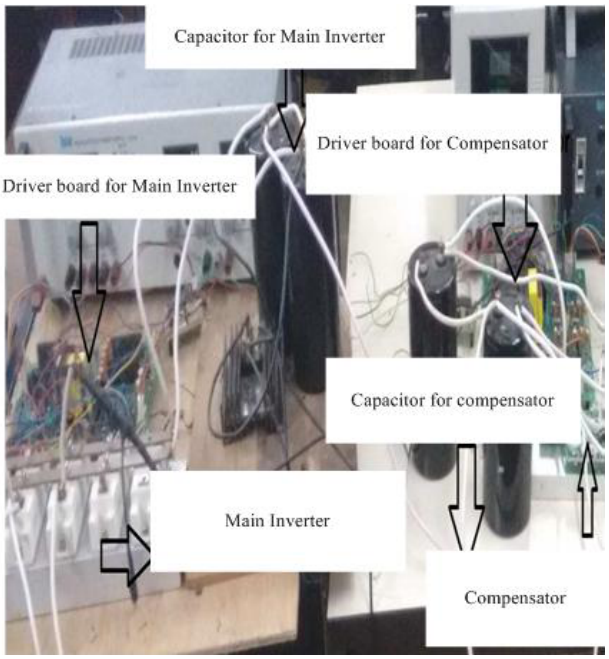
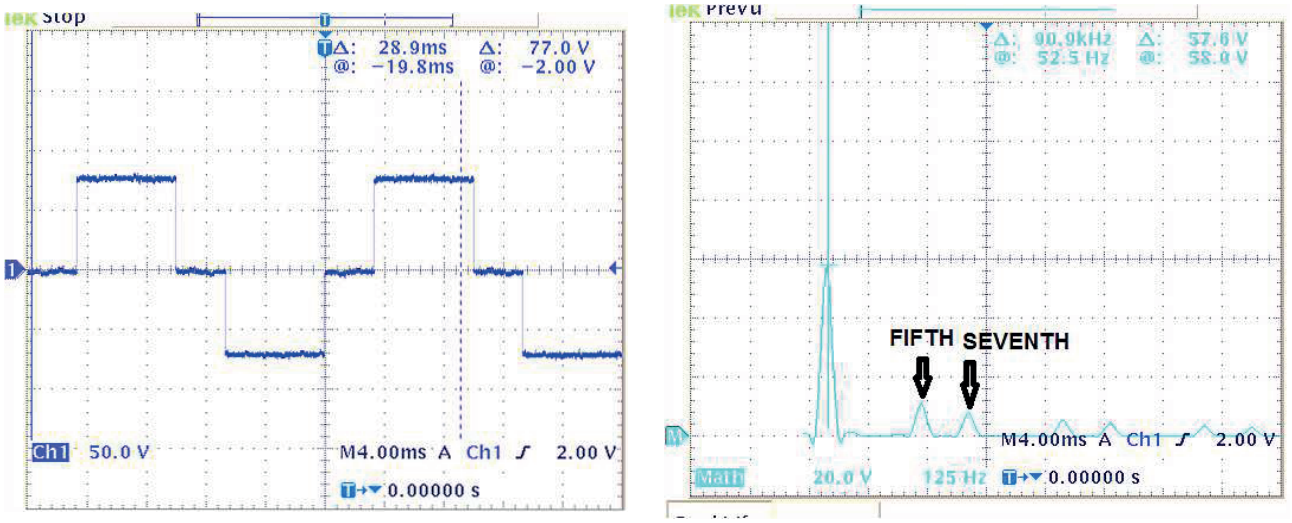


Figure 9. Experimental setup of the proposed topology.

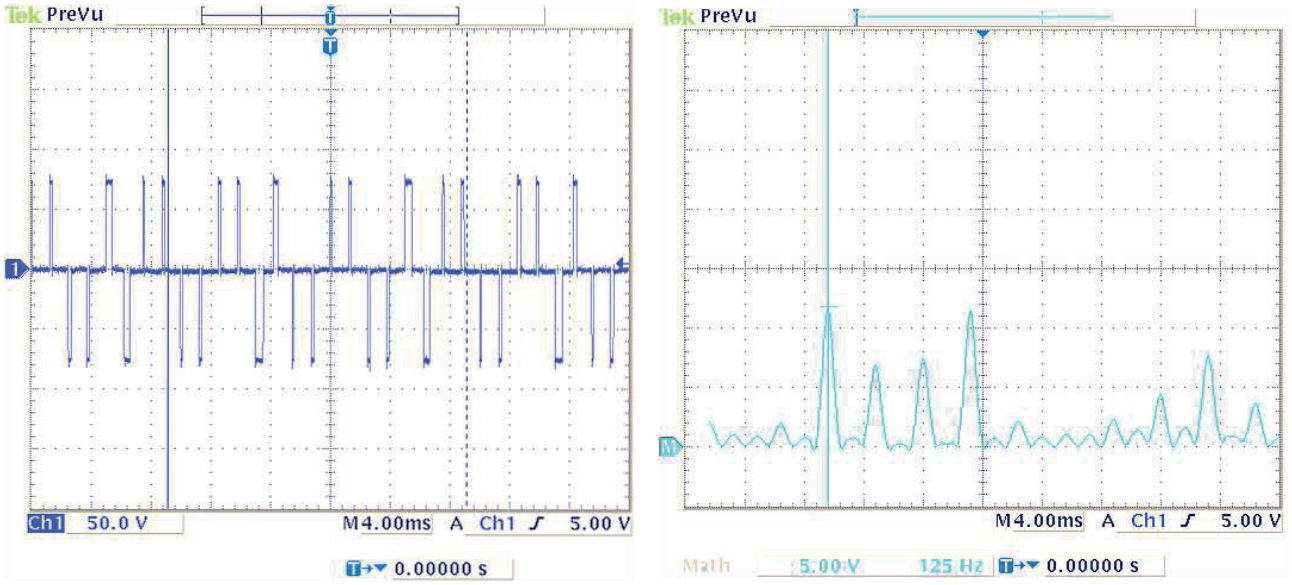


(a) (b)

Figure 10. Experimental results: (a) main inverter waveform, (b) FFT spectrum of main inverter.

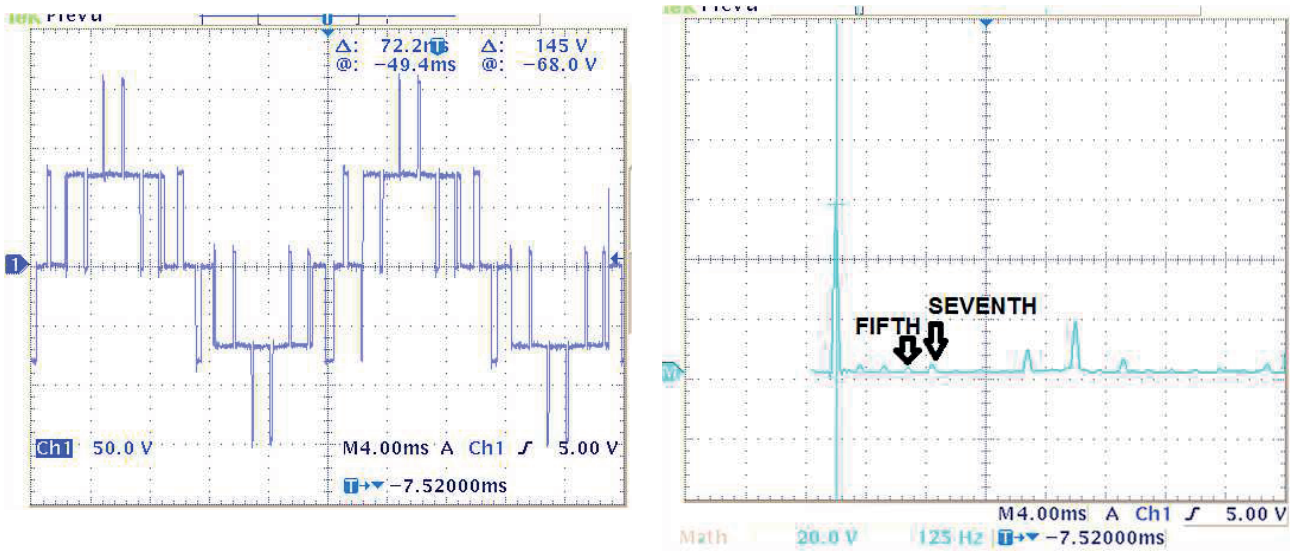
$$V_{THD} = \frac{\sqrt{V_3^2 + V_5^2 + V_7^2 + ...V_n^2}}{V_1} * 100. \tag{13}$$

The result indicates the percentage of harmonic components considered in the percentage of the signal. The higher the percentage of THD, the more distortion is present in the signal. The THD present in the voltage signal before compensation is 28.6% and after compensation with the proposed scheme it is 13.05%. Performance of the proposed scheme is comparable with that of the work in [21] with respect to dominant harmonics reduction. However, the proposed scheme outperforms [21] in reducing V_{THD}, as shown in Table 3. The proposed scheme



(a) (b)

Figure 11. Experimental results: (a) compensating inverter waveform, (b) FFT spectrum of compensating inverter.



(a) (b)

Figure 12. Experimental results: (a) main inverter waveform after adding compensating inverter, (b) FFT spectrum of main inverter with addition of compensating inverter.

performs the computation online while computation is carried out offline in [21]. Table 4 shows the advantages of the proposed method compared to earlier existing approaches.

6.1. Observations on the performance of the proposed method

The following conclusions are made with respect to the proposed method. The maximum reduction in harmonic value occurs at the same DC bus voltage values of the main inverter and compensating inverter. The normalized harmonic reduction value is identical for all ranges of loads and voltage levels.

Table 2. Harmonic reduction computed.

Harmonic value	Main inverter (M_N)	Main inverter after compensation (C_N)	% Harmonic reduction (H_R)
Fifth harmonic	11.2 V	1.2 V	90
Seventh harmonic	8 V	0.8 V	90

Table 3. Comparison with existing 120 degrees comparison methods.

	5th (% of fundamental)	7th (% of fundamental)	9th (% of fundamental)	11th (% of fundamental)	13th (% of fundamental)	THD
Without compensation	20.2	14.4	-	9.1	1.3	28.6%
Proposed online compensation	3.8	1.4	2.4	10.2	1.35	13.05%
Offline compensation [21]	1.59	3.66	-	10.7	7.7	15%

Table 4. Comparison with existing methods.

Features	Microprocessor implementation	Microcomputer implementation	Proposed method
Storage	Offline	Direct look-up table implementation	Implementation without look-up table
Execution	Medium	Medium	Fast
Storage	More memory requirement	More memory requirement	Less storage space requirement
Controller requirement	16-bit	16-bit	8-bit
Computation	Offline	Online	Online

7. Conclusion

In this paper, a synchronized microcontroller architecture is presented for eliminating lower order harmonics from a quasi square wave output. The multitasking functionality of the method comprises FFT computation of a quasi square wave and synchronized PWM pulse generation. Theoretical analysis is described for the computation of magnitude and phase of the quasi square wave. The phase and magnitude of the components are obtained from FFT computation. The synchronized PWM pulses are generated to eliminate the harmonics. The functionality of the proposed method has been demonstrated for a single-phase three-level NPC inverter. The FFT spectra from the experimental results illustrate 90% magnitude reduction of the fifth and seventh harmonic components with respect to 120 degree conduction without harmonic compensation.

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