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An improved space charge distribution analytical model to assess field-effect transistor's intrinsic capacitors

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Abstract: In this paper, an analytical model has been developed for improved assessment of Miller capacitors for high-frequency metal–semiconductor field-effect transistors. Depletion layer underneath the Schottky barrier gate has been divided into four distinct regions, and by evaluating the charges associated with each region, gate-to-source (C_{GS}) and gate-to-drain (C_{GD}) capacitors, commonly known as Miller capacitors, have been defined accordingly. Mathematical expressions have been developed both for the linear as well as for the saturation region. Miller capacitors and their variation as a function of applied bias have been assessed. It has been shown that the proposed technique offers better accuracy in determining the Miller capacitors, especially C_{GD} of the device relative to other reported analytical capacitor models. This improved accuracy has been achieved by involving the entire Schottky barrier depletion layer piecewise for the assessment of charges defining the Miller capacitors. Thus, the developed technique could be a useful tool in assessing the AC response of the device with more precision.

Key words: Metal–semiconductor field-effect transistor, analytical capacitor model, Miller capacitors, Schottky barrier gate

1. Introduction

Silicon carbide (SiC) field-effect transistors (FETs) are potential candidates for high-temperature and high-frequency applications, because they offer higher breakdown voltage and higher carrier mobility [1]. From the design point of view, high frequency capability of a SiC FET is primarily controlled by the device Miller capacitors determined by the depletion layer underneath the Schottky barrier gate. For accurate assessment of gate-to-source (C_{GS}) and gate-to-drain (C_{GD}) capacitors, it is imperative that the charge distribution underneath the Schottky barrier gate be known to a good degree of accuracy. In high-frequency FETs, the gate length of the device is of submicron dimension and for such devices, the extension of charges on the edges of the gate cannot be ignored for accurate Miller capacitors assessment.

In 1976, Yamaguchi et al. [2] derived expressions for Miller capacitors of a FET. They calculated total charge by integrating the channel underneath the Schottky barrier gate. After estimating the total charge, C_{GS} and C_{GD} were calculated. Hartgring et al. [3] derived expressions for C_{GS} and C_{GD} using Shockley's approximation, but their derived capacitance equations were too complex and difficult to be handled by a design engineer.

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In 1982, Takada et al. [4] derived analytical expressions for C_{GS} and C_{GD} by dividing the channel into three operational conditions, namely, a) before the pinch-off, b) after the pinch-off, and c) the intermediary status of the depletion. Statz et al. [5] showed that at zero or reverse bias, there is a large capacitance present between source and gate of the device that could cause large error if not taken into account. Considering this concept, they calculated total charge under the gate and derived expressions for C_{GS} and C_{GD}.

Scheinberg et al. [6] presented Miller capacitors model in 1991 by using bias-dependent nonlinear empirical equations. Hallgren et al. [7] also presented gate capacitor model of GaAs metal–semiconductor field-effect transistors (MESFETs) and demonstrated a good agreement in the modeled and the experimental data, but the developed model was inefficient in time and required 50% more time than its competitors.

Rizk et al. [8] derived gate capacitor equations using normal Schottky junction expressions and claimed improvement in predicting values of Miller capacitors at a given bias. In 1993, Rodriguez et al. [9] presented an improved junction capacitor model for FETs and exhibited by using experimental data that, in addition to the improved accuracy, their developed model has savings in CPU execution speed up to 72% compared to its counterparts. Agostino et al. [10], continuing Statz et al. [5] work, also presented a nonlinear capacitor model for FETs. They derived physics-based expressions for nonlinear parameters of the device. In their model, they evaluated total charge underneath the gate by dividing the depletion into three regions. Characteristics thus achieved were found in good agreement with the experimental data.

Bose et al. [11] derived Miller capacitors of FETs by using expressions presented by Takada and Rodriguez et al. [4, 9]. They showed that Miller capacitors are a function of gate length, as charge underneath the gate is proportional to the gate length of the device. They also extracted high frequency parameters of the device using assessed Miller capacitors and exhibited a reasonable compliance with the experimental data [11].

Murray et al. [12] derived expressions for C_{GS} and C_{GD} for both the linear and the saturation region of MESFETs output characteristics. They partitioned the charges underneath the gate into two regions; depletion region before the saturation, and after the saturation, which was further divided into two parts. The first part was underneath the Schottky metal and the second part was extension of the depletion towards the drain side. Murrey et al., however, did not compare their model experimentally, so no conclusion can be made about the accuracy of the model. In 2003, Ahmed [13] presented a method to calculate Miller capacitors of the device by using DC characteristics. Incorporating quarter circle assumption of potential at the source and at the drain side, C_{GS} and C_{GD} were found. In 2005, Aggarwal et al. [14] presented a capacitor model for SiC MESFETs. By calculating total charge under the gate as a sum of both linear and saturation regions, they showed that C_{GS} decreases as gate bias increases and doping concentration has a very small effect on the gate capacitance.

In this paper, we have extended the work of Murray et al. in which they have calculated analytical expressions for C_{GS} and C_{GD} by taking into account only three regions underneath the Schottky barrier gate. In their calculation, they ignored the extension of the depletion towards the drain side of the gate, which could have a significant contribution in charge accumulation, especially in submicron devices. This discrepancy of Murray expressions has been addressed by dividing the Schottky barrier depletion layer into four distinct regions as illustrated in Figure 1. In the figure, Region-IV describes the extension of the depletion layer towards ungated drain side of the device, and it holds charges Q_{IV} as shown in the figure. Capacitors C_{GS} and C_{GD} are evaluated and compared with Region-III model and tangible improvement, especially in the magnitude of C_{GD} is noted.

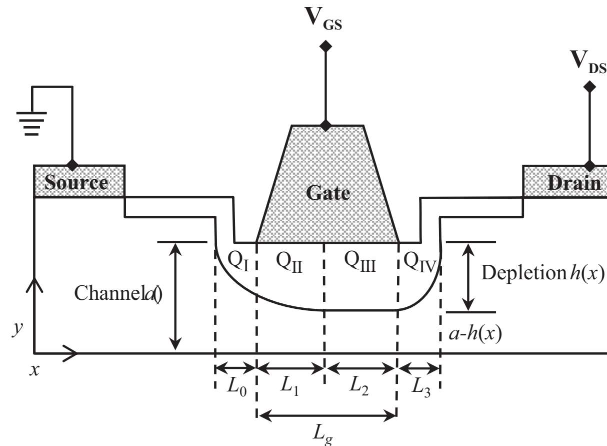

Figure 1. An operating MESFET with four distinct charge regions of the depletion layer: Region-I is defined by L_0, Region-II is defined by L_1, Region-III is defined by L_2 and finally, Region-IV is defined by the length L_3.

The remaining composition of the paper is that Section 2 deals with charge evaluation in different regions of the Schottky barrier depletion layer and its variation as a function of applied bias. Section 3 describes Miller capacitors assessment and Section 4 compares the assessed values of Miller capacitors with the experimental data. Finally, Section 5 summarizes the conclusions drawn from this research.

2. Charge evaluation

To calculate charge underneath the Schottky barrier gate of a FET, one needs basic $I-V$ expression, which governs the current flow of the device. Under the applied field (E), drain current (I_D) can be written as [15]:

$$I_D = qWN\mu(E)E(x)\left[a - h(x)\right] \tag{1}$$

where $h(x)$ is the depletion layer height, a represents epi-layer thickness of the device as shown in Figure 1, q is the electronic charge, W is the device width, N is the doping density of epi-layer, and $\mu(E)$ represents mobility of carriers, which can be defined as [16, 17].

$$\mu(E) = \frac{\mu_0}{\left[1 + \left(\dfrac{\mu_0 E}{v_s}\right)^{\beta}\right]^{1/\beta}} \tag{2}$$

In the above expression, μ_0 represents low field mobility, v_s is the saturation velocity of carriers, and $\beta \approx 1$ is a fitting parameter. Eq. (2) shows that μ is a function of applied field and typically it follows a bell-shaped profile when plotted against the increasing values of E. Reduction in the magnitude of μ at relatively increased E is predominantly associated with increased scattering caused by the high amplitude lattice phonon.

Figure 1 shows a cross-sectional view of an operating FET, where $L_g = L_1 + L_2$ represents metallic part of the Schottky barrier gate, whilst L_0 and L_3 show extension in depletion region towards source and drain sides of the Schottky barrier gate, respectively. This constitutes a four regions depletion of the Schottky barrier and the charges in each region are represented by Q_{I} to Q_{IV}, respectively. At a given bias, $I_{D(\mathrm{lin})}$ and $I_{D(\mathrm{sat})}$

for linear and saturation region, respectively, is given as [12, 18].

$$I_{D(\text{lin})} = I_P \left[\frac{3(u_d^2 - u_0^2) - 2(u_d^3 - u_0^3)}{1 + Z(u_d^2 - u_0^2)} \right] \tag{3}$$

$$I_{D(\text{sat})} = qWN\gamma v_s a\,(1 - u_1) \tag{4}$$

In Eq. (4), $\gamma \approx 1$ is a velocity saturation parameter that defines a smooth transition from the linear to the saturation region of operation. u_d and u_0 are normalized depletion layer heights towards drain and source side of the device, respectively. Variable u_1 also defines normalized depletion layer height but for location underneath the Schottky barrier gate where the carriers' velocity gets saturated. Normalized values of depletion layers as a function of applied bias are given as

$$u_d(V_G, V_D) = \sqrt{\frac{V_D + V_G + V_B}{V_P}}, \quad u_0(V_G) = \sqrt{\frac{V_G + V_B}{V_P}}, \quad u_1(V_G, V_D) = \sqrt{\frac{V(L_1) + V_G + V_B}{V_P}} \tag{5}$$

where V_D and V_G are the drain and gate potentials, respectively, V_B represents built-in potential, V_P pinch-off voltage and $V(L_1)$ is the potential under the gate, across the length L_1. Other variables of Eqs. (3) and (4) are given as

$$I_P = \frac{q^2 N^2 \mu_0 W a^3}{6\epsilon_s L_g}, \quad V_P = \frac{qNa^2}{2\epsilon_s}, \quad Z = \frac{qNa^2\mu_0}{2\epsilon_s L_g v_s} \tag{6}$$

where ϵ_s is the relative permittivity. Channel length, L_1 can be evaluated by using Eqs. (3) and (4), and is given as [19]:

$$L_1 = L_g Z \left[\frac{(u_1^2 - u_0^2) - (2/3)(u_1^3 - u_0^3)}{\gamma(1 - u_1)} - (u_1^2 - u_0^2) \right] \tag{7}$$

Potential drop at location L_1 can be assessed by applying Poisson's equation on two dimensional distribution of charges underneath the Schottky barrier depletion as shown in Figure 1. By involving device physical variables and appropriate boundary conditions, it can be shown that [19]

$$V\left(L_g, u_1 a\right) = V_P\left(u_1^2 - u_0^2\right) + \frac{2E_s a u_1}{\pi} \sinh\left[\frac{\pi\left(L_g - L_1\right)}{2au_1}\right] \tag{8}$$

where E_s represents saturation field. The first part of Eq. (8) represents potential drop in the region defined by L_1, whereas the second part of this expression represents potential drop in the region L_2. Moreover, from Figure 1, it is obvious that $L_2 = L_g - L_1$, so

$$V\left(L_1\right) = V_P\left(u_1^2 - u_0^2\right) \quad \text{and} \quad V\left(L_2\right) = \frac{2E_s a u_1}{\pi} \sinh\left[\frac{\pi L_2}{2au_1}\right] \tag{9}$$

It is obvious from Figure 1 that $V(L_0) = V_P u_0^2$ is the potential, which is caused by $V_G + V_B$. Using quarter circle approximation, L_3 can be approximated as $L_3 \approx L_g/4$ [19] resulting in

$$V(L_3) \approx \frac{2E_s a u_1}{\pi} \sinh\left[\frac{\pi L_3}{2au_1}\right] \approx \frac{2E_s a u_1}{\pi} \sinh\left[\frac{\pi L_g}{8au_1}\right] \tag{10}$$

Thus, the potential distribution across the Schottky barrier gate caused by V_D will be $V(L_0)+V(L_1)+V(L_2)+V(L_3)=V_D$, which can be written as:

$$V_P u_0^2 + V_P\left(u_1^2 - u_0^2\right) + \frac{2E_s a u_1}{\pi}\sinh\left[\frac{\pi\left(L_g - L_1\right)}{2au_1}\right] + \frac{2E_s a u_1}{\pi}\sinh\left[\frac{\pi L_g}{8au_1}\right] = V_D \tag{11}$$

2.1. For Region-I

As shown in Figure 1, the length of Region-I, which is represented by L_0, has the corresponding accumulation of charges shown as Q_{I}. For this region using quarter circle approximation [11], the magnitude of Q_{I} can be expressed as

$$Q_{\mathrm{I}} \approx \frac{\pi}{4}\epsilon_s W u_0^2 V_P \tag{12}$$

2.2. For Region-II

By considering the region represented by L_1 of Figure 1, one can see that the charge accumulation in this region is represented by Q_{II}, which can be evaluated as

$$Q_{\mathrm{II}} \approx qNW\int_0^{L_1} h(x)dx \tag{13}$$

For given values of V_D and V_G, the magnitude of Q_{II} can be known by rearranging Eqs. (1) and (2)

$$I_D\left(dx + \frac{qN\mu_0}{v_s\varepsilon_s}h(x)dx\right) = qN\mu_0 W\frac{qN}{\varepsilon_s}h(x)\left[a - h(x)\right]dx$$

After simplification and comparison with Eq. (13)

$$Q_{\mathrm{II}} = \frac{I_P V_P}{I_D}\times\frac{4\varepsilon_s W L_g}{a}\left[\left(1 - \frac{ZI_D}{3I_P}\right)(u_1^3 - u_0^3) - \frac{3}{4}(u_1^4 - u_0^4)\right] \tag{14}$$

Eq. (14) shows that the charge accumulation in Region-II is dependent upon the device physical parameters such as (WL_g/a) as well as on the device bias potentials, which control u_0 and u_1.

2.3. For Region-III

By looking at Figure 1, one can judge that the length of Region-III is defined by $L_2 = L_{\mathrm{g}} - L_1$, where it is assumed that the depletion remains constant to define the constant cross-sectional area for the saturation current. Thus, under such conditions, charge accumulated in Region-III can be represented as

$$Q_{\mathrm{III}} = qNWh_1(L_g - L_1) = qNWau_1(L_g - L_1) \tag{15}$$

2.4. For Region-IV

Again on the basis of quarter circle approximation [19], the charge accumulation in Region-IV can be approximated as

$$Q_{\mathrm{IV}} \approx \frac{\pi}{4}\epsilon_s W u_1^2 V_P \tag{16}$$

Eq. (16) represents the magnitude of charges accumulated in Region-IV, which are dependent upon the physical parameters W and a of the device. The variable a is indirectly there because of V_P as evident from Eq. (6). This shows that for devices meant for high-power and high-frequency applications, where W and V_P both are usually high, Q_{IV} will have a significant contribution and cannot be overlooked. Furthermore, when L_g of the device is small, Region-II and Region-III are bound to shrink as one can see from Figure 1 and for such devices, Region-IV shall have a pronounced effect in the evaluation of C_{GD} capacitor of the device.

Now, the total charge under the Schottky barrier gate can be attained by combining charges given in Eqs. (12), (14)–(16), i.e.

$$Q_{\mathrm{T}} = Q_{\mathrm{I}} + Q_{\mathrm{II}} + Q_{\mathrm{III}} + Q_{\mathrm{IV}}$$

$$Q_{\mathrm{T}} = \frac{\pi}{4}\epsilon_s W u_0^2 V_P + \frac{4 I_P V_P \varepsilon_s W L_g}{a I_D}\left[\left(1 - \frac{Z I_D}{3 I_P}\right)(u_1^3 - u_0^3) - \frac{3}{4}(u_1^4 - u_0^4)\right] + qNWau_1(L_g - L_1) + \frac{\pi}{4}\epsilon_s W u_1^2 V_P \tag{17}$$

Knowing the charge distribution as given by Eq. (17), one can find Miller capacitors both for the linear as well as for the saturation region of operation of a FET. Since it involves the entire depletion layer underneath the gate, it is assumed that the respective capacitor evaluation thus achieved will have better accuracy compared to Region-II or -III depletion models.

3. Gate-to-drain capacitor, C_{GD}

3.1. Linear region

To evaluate gate-to-drain capacitor (C_{GD}), one can differentiate Eq. (17) w.r.t V_D keeping V_G constant.

$$C_{GD}^L = \left.\frac{\partial Q_{\mathrm{T}}}{\partial V_D}\right|_{V_G=\mathrm{C}} = \left.\frac{\partial Q_{\mathrm{I}}}{\partial V_D}\right|_{V_G=\mathrm{C}} + \left.\frac{\partial Q_{\mathrm{II}}}{\partial V_D}\right|_{V_G=\mathrm{C}} + \left.\frac{\partial Q_{\mathrm{III}}}{\partial V_D}\right|_{V_G=\mathrm{C}} + \left.\frac{\partial Q_{\mathrm{IV}}}{\partial V_D}\right|_{V_G=\mathrm{C}} \tag{18}$$

In the linear region near the drain side, carriers are moving below the saturation velocity. Therefore, we can assume that there would be negligible tapering of the depletion to define Region-III and Region-IV. The entire depletion can be treated as a uniformly distributed layer underneath the Schottky barrier gate. Thus, L_1 in such a case would be defined by the entire gate length, i.e. $L_1 = L_g$ and the contribution of V_D in changing the depletion layer defining Q_{III} and Q_{IV} would be negligible; therefore,

$$Q_{\mathrm{III}} \approx Q_{\mathrm{IV}} \approx 0$$

In such a scenario, depletion layer underneath the Schottky barrier gate will have contribution made by the charges Q_{I} and Q_{II} alone, which are defined by Eqs. (12) and (14), respectively.

$$C_{GD}^{L} = \left.\frac{\partial Q_{\mathrm{I}}}{\partial V_D}\right|_{V_{G=\mathrm{C}}} + \left.\frac{\partial Q_{\mathrm{II}}}{\partial V_D}\right|_{V_{G=\mathrm{C}}}$$

Differentiating Eqs. (12) and (14) w.r.t V_D, and using $u_1 = u_d$ and $L_1 = L_g$ yields $\left.\frac{\partial Q_{\mathrm{I}}}{\partial V_D}\right|_{V_{G=\mathrm{C}}} = 0$, and

$$\frac{\partial Q_{\mathrm{II}}}{\partial V_D} = \frac{4\varepsilon_s W L_g V_P}{a}\frac{I_P}{I_D}\left[\frac{-G_{DL}}{I_D}\left\{(u_d^3 - u_0^3) - \frac{3}{4}(u_d^4 - u_0^4)\right\} + \frac{3u_d}{2V_P}\left(1 - u_d - \frac{Z}{3}\frac{I_D}{I_P}\right)\right]$$

where $\partial I_{D(\mathrm{lin})}/\partial V_D = G_{DL}$, which is the output conductance for the linear region. Thus, C_{GD}^{L} for the linear region can be expressed as

$$C_{GD}^{L} = \frac{4\varepsilon_s W L_g V_P}{a}\frac{I_P}{I_D}\left[\frac{-G_{DL}}{I_D}\left\{(u_d^3 - u_0^3) - \frac{3}{4}(u_d^4 - u_0^4)\right\} + \frac{3u_d}{2V_P}\left(1 - u_d - \frac{Z}{3}\frac{I_D}{I_P}\right)\right] \tag{19}$$

This expression gives variation in C_{GD}^{L} as a function of device and bias parameters. It shows that the magnitude of C_{GD}^{L} is directly proportional to (WL_g/a), which is the cross-sectional area defining the flow of current. This implies that by decreasing the available cross-sectional area, there is a decrease in the C_{GD}^{L}. A decrease in the cross-sectional area would mean that there is an extension in the height of depletion region caused by the applied potential. This explains the dependence of C_{GD}^{L} on the device bias potential.

3.2. Saturation region

In the saturation region of operation, the Miller capacitor is denoted by C_{GD}^{S}, which can be defined as

$$C_{GD}^{S} = \left.\frac{\partial Q_{\mathrm{II}}}{\partial V_D}\right|_{V_{G=\mathrm{C}}} + \left.\frac{\partial Q_{\mathrm{III}}}{\partial V_D}\right|_{V_{G=\mathrm{C}}} + \left.\frac{\partial Q_{\mathrm{IV}}}{\partial V_D}\right|_{V_{G=\mathrm{C}}} \tag{20}$$

It is worth mentioning that the charge Q_{I}, as discussed before, is primarily caused by V_G, which, therefore, will not contribute in defining C_{GD}^{S}. Eq. (20) has three parts and the first part of this expression can be evaluated by involving Eq. (14), which gives

$$\frac{\partial Q_{\mathrm{II}}}{\partial V_D} = \frac{4\varepsilon_s W L_g V_P}{a}\frac{I_P}{I_D}\left\{\frac{-G_{DS}}{I_D}\left((u_1^3 - u_0^3) - \frac{3}{4}(u_1^4 - u_0^4)\right) + \frac{3u_1}{2V_P}\left(1 - u_1 - \frac{Z}{3}\frac{I_D}{I_P}\right)\mathit{\Gamma}(V_G, V_D)\right\} \tag{21}$$

where $\partial I_{D(\mathrm{sat})}/\partial V_D = G_{DS}$, which represents output conductance for the saturation region. Now starting from Eq. (4) and by differentiating Eq. (11) w.r.t V_D keeping V_G constant and by involving Eqs. (5) and (7), the

function $\Gamma(V_G, V_D)$ of Eq. (21) can be derived as

$$\Gamma(V_G,V_D) = \Bigg[1+\frac{E_s a}{\pi u_1 V_P}\Bigg\{\sinh\left(\frac{\pi(L_g-L_1)}{2au_1}\right)-\frac{\pi}{2a}\cosh\left(\frac{\pi(L_g-L_1)}{2au_1}\right) \Bigg\{L_g Z\left(\frac{(u_1^2-u_0^2)-\frac{2}{3}(u_1^3-u_0^3)}{\gamma(1-u_1)^2}+2u_1\frac{1-\gamma}{\gamma}\right)+\frac{L_g-L_1}{u_1}\Bigg\} +\sinh\left(\frac{\pi L_g}{8au_1}\right)-\frac{\pi L_g}{8au_1}\cosh\left(\frac{\pi L_g}{8au_1}\right)\Bigg\}\Bigg]^{-1} \tag{22}$$

The second part of Eq. (20) can be assessed using Eq. (15)

$$\frac{\partial Q_{\mathrm{III}}}{\partial V_D} = qNWau_1\left(-\frac{\partial L_1}{\partial V_D}\right)+qNWa\left(L_g-L_1\right)\frac{1}{2u_1V_P}\Gamma(V_G,V_D) \tag{23}$$

and by using Eq. (7), one can write

$$\frac{\partial L_1}{\partial V_D} = \frac{L_g Z\Gamma(V_G,V_D)}{V_P}\left[\left(\frac{(u_1^2-u_0^2)-\frac{2}{3}(u_1^3-u_0^3)}{2\gamma u_1(1-u_1)^2}\right)+\frac{1-\gamma}{\gamma}\right] \tag{24}$$

Combining Eqs. (23) and (24), we get

$$\frac{\partial Q_{\mathrm{III}}}{\partial V_D} = \frac{\varepsilon_s W L_g}{au_1}\Gamma(V_G,V_D)\chi(V_G,V_D) \tag{25}$$

where the function $\chi(V_G, V_D)$ is defined as

$$\chi(V_G,V_D) = \left[1-\frac{L_1}{L_g}-Zu_1\left\{\frac{(u_1^2-u_0^2)-\frac{2}{3}(u_1^3-u_0^3)}{\gamma(1-u_1)^2}+2u_1\left(\frac{1-\gamma}{\gamma}\right)\right\}\right] \tag{26}$$

Finally, to find the contribution of Q_{IV} towards C_{GD}^S, Eq. (16) is employed, where

$$\frac{\partial Q_{\mathrm{IV}}}{\partial V_D} = \frac{\pi}{4}\epsilon_s W\frac{\partial V(L_1)}{\partial V_D} = \frac{\pi}{4}\epsilon_s W\Gamma(V_G,V_D) \tag{27}$$

Now by combining Eqs. (20), (21), (25) and (27), final expression for C_{GD}^S is obtained as

$$C_{GD}^S = \Gamma(V_G,V_D)\Bigg[\frac{4\varepsilon_s W L_g V_P}{a}\frac{I_P}{I_D}\Bigg\{\frac{-G_{DS}}{\Gamma(V_G,V_D)I_D}\left((u_1^3-u_0^3)-\frac{3}{4}(u_1^4-u_0^4)\right) +\frac{3u_1}{2V_P}\left(1-u_1-\frac{Z}{3}\frac{I_D}{I_P}\right)\Bigg\}+\frac{\varepsilon_s W L_g}{au_1}\chi(V_G,V_D)+\frac{\pi}{4}\epsilon_s W\Bigg] \tag{28}$$

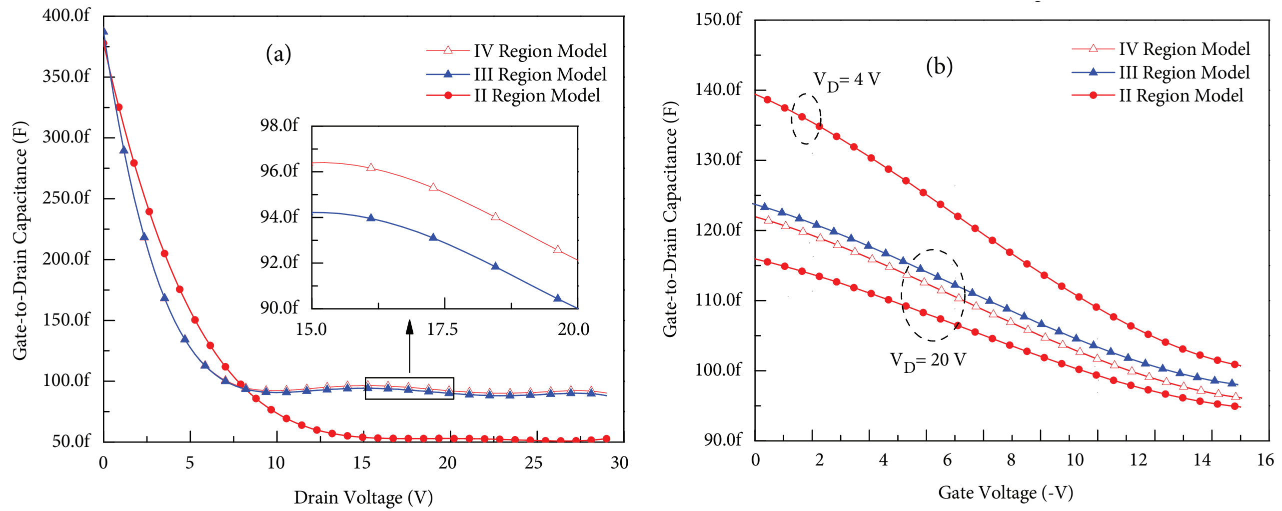

Figure 2. Variation in gate-to-drain capacitor (C_{GD}) for both linear and saturation regions of operation of a MESFET having $W = 500$ μm, $L_g = 0.5$ μm, $a = 0.3$ μm, and $N = 2.79 \times 10^{23}$ m^{-3}; (a) as a function of drain bias (b) as a function of gate bias.

Eq. (28) represents C^S_{GD} as a function of device physical as well as bias parameters. Usually, microwave devices are operated in the saturation region of operation therefore, Eq. (28) will play a crucial role in determining the device high frequency response. It is also pertinent to mention here that Eq. (28) has been evaluated comprehensively by involving all possible regions underneath the Schottky barrier gate. It is, therefore, assumed that it should provide a better accuracy in assessing C^S_{GD} of a finished device as a function of applied bias. It is pertinent to mention here that for Region-II model, $Q_{\text{II}} + Q_{\text{III}}$ are considered, for Region-III model, $Q_{\text{I}} + Q_{\text{II}} + Q_{\text{III}}$ are used, whereas for Region-IV model, $Q_{\text{I}} + Q_{\text{II}} + Q_{\text{III}} + Q_{\text{IV}}$ are used to assess the respective Miller capacitors.

Figure 2 shows variation in C_{GD} as a function of V_D and V_G for a submicron MESFET. Figure 2a represents C_{GD} for both linear and saturation region of operation of a microwave MESFET. Moreover, the figure represents Region-II, -III, and -IV depletion layer models discussed in the preceding paragraphs. The figure exhibits a sharp decline in the magnitude of C_{GD} with increasing values of V_D for various models under discussion. This decline is primarily associated with increased depletion layer width as a function of V_D, which causes an increased separation between the charges defining the depletion layer capacitor. Examination of the figure also shows that there is a significant difference in the magnitude of C_{GD} for Region-II depletion layer model relative to Region-III and -IV models. This is so, because the Region-II depletion layer model to assess C_{GD} is a simplified model and it ignores the extension of depletion towards the drain and source side of the device. Apparently, Region-III and -IV models provide almost a similar C_{GD} vs. V_D profile; however, a zoomed view of Figure 2a, shown in the inset of the figure, revealed that there is a difference in the assessed values of C_{GD} for Region-III and -IV models. In some cases, this could meaningfully contribute in assessing the correct high frequency response of a microwave FET.

Figure 2b is plotted to represent once again variation in C_{GD} capacitor but in this case as a function of V_G. This figure is plotted using Eqs. (19) and (28), where a relatively lower drain voltage value, i.e. $V_D = 4$ V is taken as a constant potential to represent linear region of operation, whilst $V_D = 20$ V represents saturation region of operation. In the linear region of operation, all the models under discussion have the same response.

Therefore, only one curve is shown at $V_D = 4$ V, whereas at $V_D = 20$ V, the plot shows an independent response of each model. Lowest values are observed for Region-II model, whilst highest values are observed for Region-III model. However, the profile of the plot at $V_D = 20$ V is identical for all the three models under evaluation.

4. Gate-to-source capacitor, C_{GS}

4.1. Linear region

Keeping in view the cross-sectional view of the depletion layer shown in Figure 1, it is obvious that linear region capacitor, C_{GS}^L is defined by those regions of the depletion layer, which are identified as Q_{I} and Q_{II}. Therefore, one can write C_{GS}^L as

$$C_{GS}^L = \left.\frac{\partial Q_{\mathrm{I}}}{\partial V_G}\right|_{V_{D=\mathrm{C}}} + \left.\frac{\partial Q_{\mathrm{II}}}{\partial V_G}\right|_{V_{D=\mathrm{C}}} \tag{29}$$

Differentiating Eq. (12) w.r.t V_G while keeping V_D constant, we can write the value of the capacitor associated with Region-I as

$$\left.\frac{\partial Q_{\mathrm{I}}}{\partial V_G}\right|_{V_{D=\mathrm{C}}} = \frac{\pi}{4}\epsilon_s W \tag{30}$$

In writing Eq. (30), quarter circle approximation is assumed. Now using the definition of Q_{II} as given by Eq. (14) and combining it with Eq. (5) and by replacing $u_1 = u_d$, we can have

$$\frac{\partial Q_{\mathrm{II}}}{\partial V_G} = \frac{4\varepsilon_s W L_g V_P}{a}\frac{I_P}{I_D}\left\{\frac{-G_{ML}}{I_D}\left((u_d^3 - u_0^3) - \frac{3}{4}(u_d^4 - u_0^4)\right)\right.$$
$$\left.+3u_d^2\left(1 - u_d - \frac{Z}{3}\frac{I_D}{I_P}\right)\frac{\partial u_d}{\partial V_G} - 3u_0^2\left(1 - u_0 - \frac{Z}{3}\frac{I_D}{I_P}\right)\frac{\partial u_0}{\partial V_G}\right\}$$

where $\partial u_d/\partial V_G = 1/2u_d V_P$, $\partial u_0/\partial V_G = 1/2u_0 V_P$ and $\partial I_{D(\mathrm{lin})}/\partial V_G = G_{ML}$, so combining the above expression with Eqs. (29) and (30)

$$C_{GS}^L = \frac{\pi}{4}\epsilon_s W + \frac{4\varepsilon_s W L_g V_P}{a}\frac{I_P}{I_D}\left\{\frac{-G_{ML}}{I_D}\left((u_d^3 - u_0^3) - \frac{3}{4}(u_d^4 - u_0^4)\right)\right.$$
$$\left.+\frac{3}{2V_P}(u_d - u_0)\left(1 - \frac{Z}{3}\frac{I_D}{I_P}\right) - \frac{3}{2V_P}(u_d^2 - u_0^2)\right\} \tag{31}$$

where G_{ML} is the transconductance in the linear region of operation. Eq. (31) represents variation in C_{GS}^L as a function of device applied bias. It clearly shows a significant contribution of Region-I in defining the magnitude of C_{GS}^L.

4.2. Saturation region

In the saturation region of operation, gate-to-source capacitor (C_{GS}^S) will be defined by the sum of charges marked as Q_{I}, Q_{II}, Q_{III} and Q_{IV} in Figure 1, and is given by

$$C_{GS}^S = \left.\frac{\partial Q_{\text{I}}}{\partial V_G}\right|_{V_{D=\text{C}}} + \left.\frac{\partial Q_{\text{II}}}{\partial V_G}\right|_{V_{D=\text{C}}} + \left.\frac{\partial Q_{\text{III}}}{\partial V_G}\right|_{V_{D=\text{C}}} + \left.\frac{\partial Q_{\text{IV}}}{\partial V_G}\right|_{V_{D=\text{C}}} \tag{32}$$

Eq. (32) is comprised of four terms. The first term has the same definition as that of Eq. (30), whereas the 2nd term of Eq. (32) can be evaluated by differentiating Eq. (14) w.r.t V_G keeping V_D constant

$$\begin{aligned} \frac{\partial Q_{\text{II}}}{\partial V_G} = \frac{4\varepsilon_s W L_g V_P}{a}\frac{I_P}{I_D}\left\{\frac{-G_{MS}}{I_D}\left((u_1^3-u_0^3)-\frac{3}{4}(u_1^4-u_0^4)\right)\right. \\ \left. +3u_1^2\left(1-u_1-\frac{Z}{3}\frac{I_D}{I_P}\right)\frac{\partial u_1}{\partial V_G} - 3u_0^2\left(1-u_0-\frac{Z}{3}\frac{I_D}{I_P}\right)\frac{\partial u_0}{\partial V_G}\right\} \end{aligned} \tag{33}$$

where

$$\frac{\partial u_1}{\partial V_G} = \frac{1}{2u_1V_P}\left(\frac{\partial V(L_1)}{\partial V_G}+1\right)$$

For writing Eq. (33), we also used $\partial u_0/\partial V_G = 1/(2u_0V_P)$ and $\partial I_{D(\text{sat})}/\partial V_G = G_{MS}$, which represents transconductance in the saturation region of operation. To evaluate potential $V(L_1)$ at the location where carriers are attaining the saturation velocity, we can differentiate Eq. (11) w.r.t V_G while keeping V_D constant

$$\begin{aligned} \frac{\partial V(L_1)}{\partial V_G} = -\left[\frac{1}{2u_0} + \frac{E_s a}{\pi u_1 V_P}\left\{\sinh\left(\frac{\pi(L_g-L_1)}{2au_1}\right) - \cosh\left(\frac{\pi(L_g-L_1)}{2au_1}\right)\right.\right. \\ \frac{\pi}{2a}\left\{L_g Z\left(\frac{(u_1^2-u_0^2)-\frac{2}{3}(u_1^3-u_0^3)}{\gamma(1-u_1)^2} - \frac{2u_1(u_1-u_0)}{\gamma(1-u_1)}\right) + \frac{1}{u_1}(L_g-L_1)\right\} \\ \left.\left. +\sinh\left(\frac{\pi L_g}{8au_1}\right) - \frac{\pi L_g}{8au_1}\cosh\left(\frac{\pi L_g}{8au_1}\right)\right\}\right] \Gamma(V_{GS},V_{DS}) = \Psi(V_{GS},V_{DS}) \end{aligned} \tag{34}$$

Combining Eqs. (33) and (34), we have

$$\begin{aligned} \frac{\partial Q_{\text{II}}}{\partial V_G} = \frac{4\varepsilon_s W L_g V_P}{a}\frac{I_P}{I_D}\left[\frac{-G_{MS}}{I_D}\left((u_1^3-u_0^3)-\frac{3}{4}(u_1^4-u_0^4)\right) + \frac{3u_1}{2V_P}\right. \\ \left.\left(1-u_1-\frac{Z}{3}\frac{I_D}{I_P}\right)\left(\Psi(V_{GS},V_{DS})+1\right) - \frac{3u_0}{2V_P}\left(1-u_0-\frac{Z}{3}\frac{I_D}{I_P}\right)\right] \end{aligned} \tag{35}$$

Now to have the contribution in C_{GS}^{S} by the third part of charges referred to as Q_{III} in Eq. (32), we can differentiate Eq. (15) w.r.t V_G keeping V_D constant, which generates

$$\left.\frac{\partial Q_{\mathrm{III}}}{\partial V_G}\right|_{V_D} = qNWa\left\{\frac{L_g - L_1}{2u_1 V_P}\Big(\Psi(V_{GS},V_{DS})+1\Big) - u_1\left(\frac{\partial L_1}{\partial V_G}\right)\right\} \tag{36}$$

In writing the above expression, use of Eq. (34) is made. By combining Eqs. (7), (26), and (34) we have

$$\frac{\partial L_1}{\partial V_G} = \frac{L_g Z}{V_P}\left\{\frac{\chi(V_{GS},V_{DS}) - 1 + \dfrac{L_1}{L_g}}{2Zu_1^2}\Big(\Psi(V_{GS},V_{DS})+1\Big) - \frac{1-\gamma}{\gamma} - \frac{(u_1-u_0)}{\gamma(1-u_1)}\right\} \tag{37}$$

This gives a final version of Eq. (36) as

$$\left.\frac{\partial Q_{\mathrm{III}}}{\partial V_G}\right|_{V_D} = \frac{2\varepsilon_s W L_g Z u_1}{a}\left[\left(\frac{1 - \dfrac{\chi(V_{GS},V_{DS})}{2} - \dfrac{L_1}{L_g}}{Zu_1^2}\right)\Big(\Psi(V_{GS},V_{DS})+1\Big) + \frac{1-\gamma}{\gamma} + \frac{(u_1-u_0)}{\gamma(1-u_1)}\right] \tag{38}$$

Fourth and the final part of the depletion layer, which contributes in the definition of C_{GS}^{S}, can be assessed by differentiating Eq. (16) w.r.t V_G keeping V_D constant

$$\left.\frac{\partial Q_{\mathrm{IV}}}{\partial V_G}\right|_{V_D} = \frac{\pi\epsilon_s W}{4}\left(\frac{\partial V(L_1)}{\partial V_G}+1\right) \tag{39}$$

Substituting the value of $\left(\dfrac{\partial V(L_1)}{\partial V_G}\right)$ from Eq. (34) into Eq. (39), we have

$$\left.\frac{\partial Q_{\mathrm{IV}}}{\partial V_G}\right|_{V_D} = \frac{\pi\epsilon_s W}{4}\Big[1+\Psi(V_{GS},V_{DS})\Big] \tag{40}$$

Combining Eqs. (30), (35), (38), and (40), we arrived at Eq. (41).

$$\begin{aligned} C_{GS}^{S} = \frac{\pi}{4}\epsilon_s W + \frac{\pi\epsilon_s W}{4}\Big[1+\Psi(V_{GS},V_{DS})\Big] + \frac{4\varepsilon_s W L_g V_P}{a}\frac{I_P}{I_D}\Bigg[\frac{-G_{MS}}{I_D}\left((u_1^3-u_0^3) - \frac{3}{4}(u_1^4-u_0^4)\right) \\ + \frac{3u_1}{2V_P}\left(1-u_1-\frac{Z}{3}\frac{I_D}{I_P}\right)\Big(\Psi(V_{GS},V_{DS})+1\Big) - \frac{3u_0}{2V_P}\left(1-u_0-\frac{Z}{3}\frac{I_D}{I_P}\right)\Bigg] \\ + \frac{2\varepsilon_s W L_g Z u_1}{a}\left[\left(\frac{1 - \dfrac{\chi(V_{GS},V_{DS})}{2} - \dfrac{L_1}{L_g}}{Zu_1^2}\right)\Big(\Psi(V_{GS},V_{DS})+1\Big) + \frac{1-\gamma}{\gamma} + \frac{(u_1-u_0)}{\gamma(1-u_1)}\right] \end{aligned} \tag{41}$$

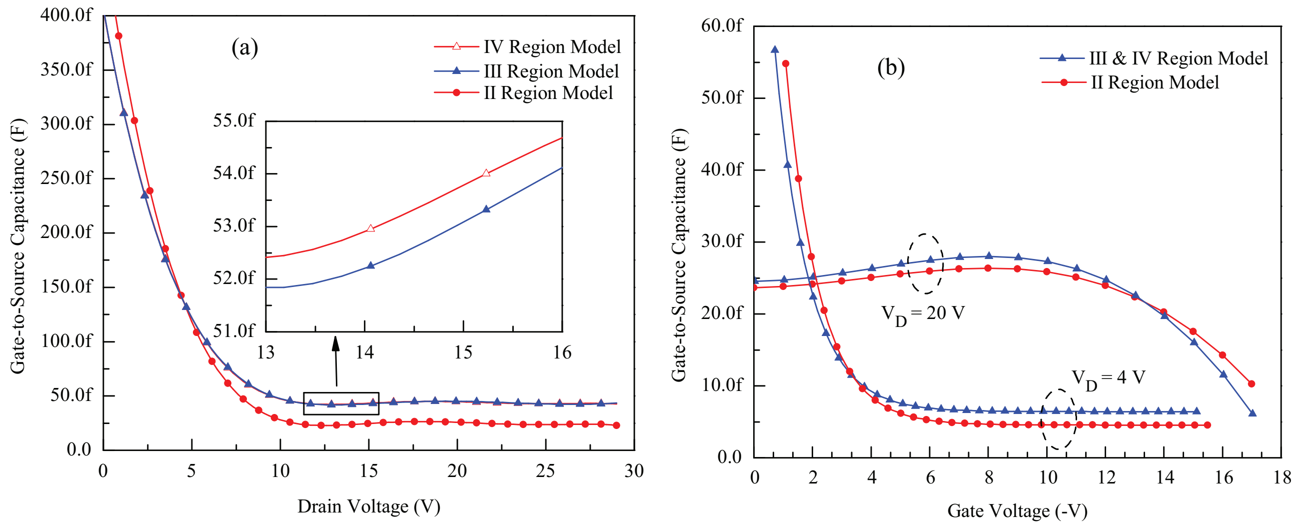

Figure 3. Variation in gate-to-source capacitor (C_{GS}) for both linear and saturation regions of operation of a MESFET having $W = 500$ μm, $L_g = 0.5$ μm, $a = 0.3$ μm and $N = 2.79 \times 10^{23}$ m^{-3}; (a) as a function of drain bias (b) as a function of gate bias.

This equation represents C_{GS}^{S} of the proposed four region model and its variation as a function of V_D and V_G as shown in Figures 3a and 3b, respectively. Careful examination of Figure 3a reveals that Region-II model, after the onset of current saturation, gives lower values of C_{GS}^{S} compared to Region-III and -IV models, whilst the difference between Region-III and -IV models in estimating C_{GS}^{S} is nominal, which is shown in the inset of Figure 3a. On the other hand, Figure 3b represents C_{GS} for linear, that is $V_D = 4$ V plots, as well as for saturation region of operation, that is $V_D = 20$ V plots. It is pertinent to mention here that at $V_D = 20$ V, plots maintain almost a straight profile for a reasonable variation in V_G and then they exhibit a decline with increasing magnitude of V_G. A decline in the values of C_{GS}^{S} after $V_G = -8$ V, as evident from Figure 3b, could be associated with an increased depletion width caused by the applied V_G.

5. Discussion

To check the accuracy of the proposed Region-IV Miller capacitors model in contrast to other models, Figures 4 and 5 have been plotted, where experimental data of a submicron SiC MESFET is compared for C_{GD} and C_{GS} capacitors, respectively. It can be seen from Figure 4 that the proposed Region-IV model gives better fit to experimental data compared to other two models. As expected, Region-III model is better than Region-II model, whereas Region-IV model maps the experimental data with reasonable accuracy both as a function of V_{DS} and V_{GS}.

Figure 5 gives experimental and evaluated values of C_{GS} as a function of drain and gate bias. One can see from the figure that the behavior of Region-III and -IV models are identical and close to the experimental data, whilst Region-II model shows a significant deviation. Identical response of Region-III and -IV models in assessing C_{GS} is understandable because Region-IV, shown in Figure 1, contributes only in C_{GD} resulting into an identical response of Region-III and -IV models in evaluating C_{GS} as evident from Figures 5a and 5b. Furthermore, improvement observed in assessing Miller capacitors using Region-IV depletion layer model has been summarized in Table 1, where it is shown that there is 69% and 93% improvement in RMSE while assessing C_{GD} as a function of V_{DS} and V_{GS}, respectively, relative to Region-III model.

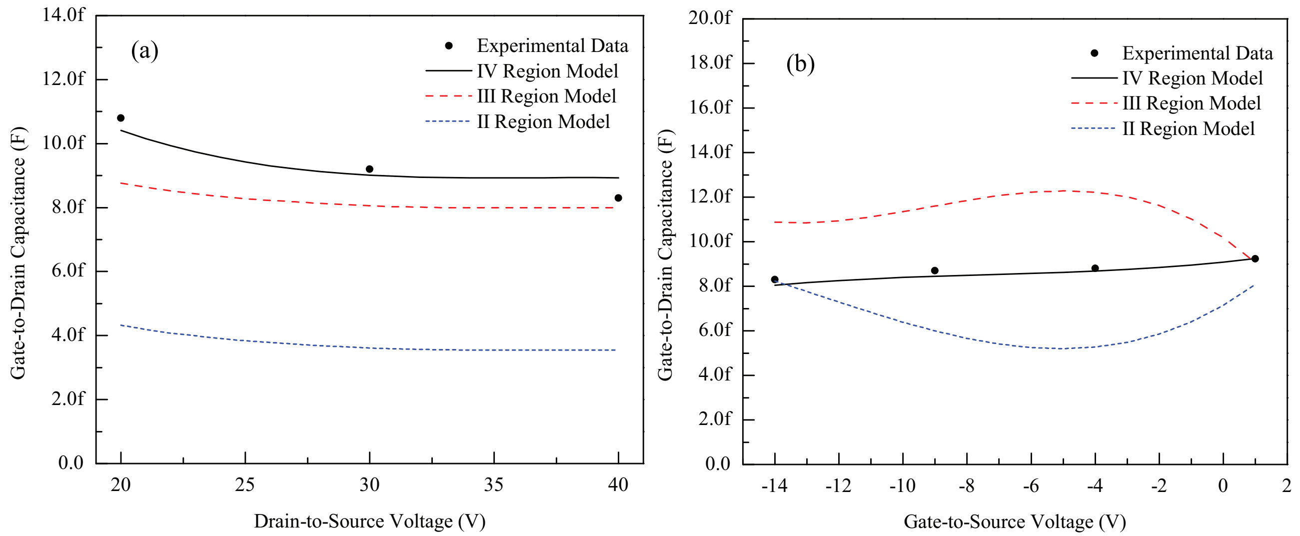

Figure 4. Gate-to-drain capacitor (C_{GD}) of a MESFET having $W = 500$ μm, $L_g = 0.5$ μm, $a = 0.3$ μm, and $N = 2.79 \times 10^{23}$ m^{-3}; (a) as a function of drain bias (b) as a function of gate bias. Experimental data from Ref. [20].

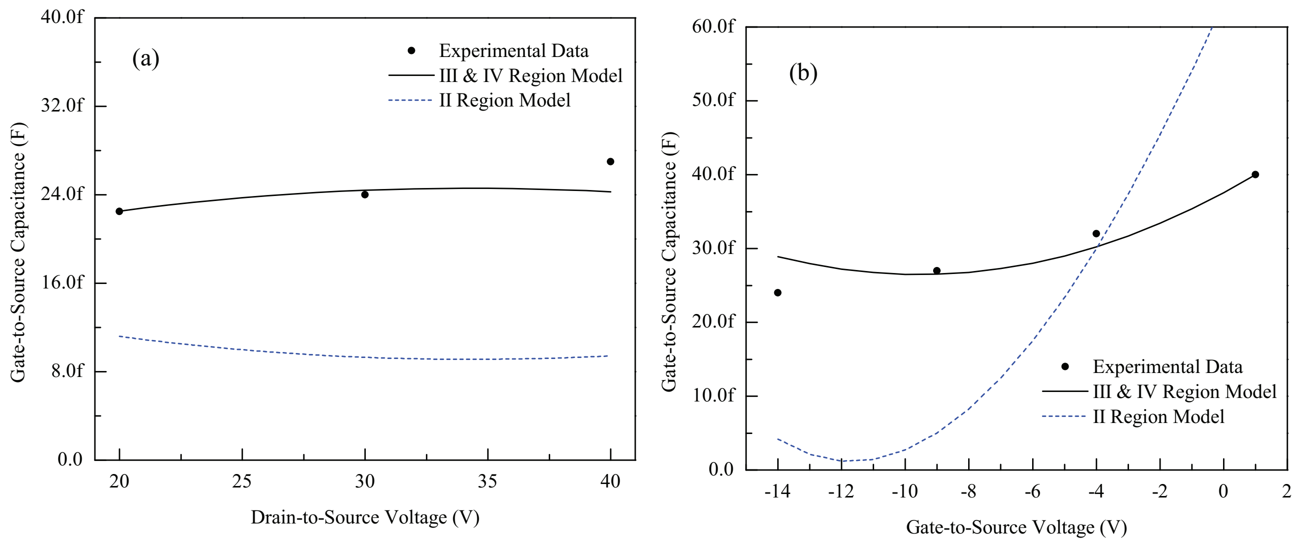

Figure 5. Gate-to-source capacitor (C_{GS}) of a MESFET having $W = 500$ μm, $L_g = 0.5$ μm, $a = 0.3$ μm and $N = 2.79 \times 10^{23}$ m^{-3}; (a) as a function of drain bias, (b) as a function of gate bias. Experimental data from [20].

6. Conclusion

In this article, an analytical model has been developed to assess Miller capacitors of a FET by distributing the depletion layer underneath the Schottky barrier gate of the device into four distinct regions. Region-I of the depletion is its extension towards the source side of the gate other than the Schottky barrier metal, whereas Region-II starts from the Schottky metal to the point where the carriers' velocity gets saturated, and from this point to the end of the Schottky metal gate, the depletion layer is represented by Region-III. Finally, Region-IV is defined by the extension of the depletion towards the drain side of the device. Analytical expressions have been developed to assess the linear as well as the saturation region gate-to-source (C_{GS}) and gate-to-drain

Table 1. Root mean square error (RMSE) in SiC MESFET C_{GS} and C_{GD} capacitors values evaluated using different depletion regions as illustrated in Figure 1. The least RMSE for each case is shown in bold face.

Model	RMSE ($\times 10^{-8}$) w.r.t V_{DS}		RMSE ($\times 10^{-8}$) w.r.t V_{GS}	
	C_{GS}	C_{GD}	C_{GS}	C_{GD}
II Region	9.51	5.86	12.9	2.45
III Region	1.06	1.45	1.31	2.74
IV Region	1.06	0.44	1.31	0.19

(C_{GD}) capacitors. It has been shown that three region analytical model to assess Miller capacitors, especially C_{GD} of the device reduces its accuracy because it does not take into account accurately Region-IV of the device, which plays a crucial role in defining the Miller capacitors. The proposed technique exhibited 69% and 93% improvement in RMSE while assessing C_{GD} as a function of V_{DS} and V_{GS}, respectively, relative to Region-III model when compared with the experimental data.

References

[1] Alexandru M, Banu V, Godignon P, Vellvehi M, Millan J. 4H-SiC MESFET specially designed and fabricated for high temperature integrated circuits. In: 2013 Proceedings of the European Solid-State Device Research Conference (ESSDERC), New York, NY, USA: IEEE; 2013. pp. 103-106.

[2] Yamaguchi K, Kodera H. Drain conductance of junction gate FET's in the hot electron range. IEEE T Electron Devices 1976; 23: 545-553.

[3] Hartgring CD, Oldham W, Chiu TY. A MESFET model for circuit analysis. Solid-State Electron 1980; 198: 121-126.

[4] Takada T, Yokoyama, Kiyoyuki, Ida M, Sudo T. A MESFET variable-capacitance model for GaAs integrated circuit simulation. IEEE T Micro Theory Tech 1982; 30: 719-724.

[5] Statz H, Newman P, Smith IW, Pucel RA, Haus HA. GaAs FET device and circuit simulation in SPICE. IEEE T Electron Devices 1987; 34: 160-169.

[6] Scheinberg N, Chisholm E. A capacitance model for GaAs MESFETs. IEEE J. Solid-State Circuits 1991; 26: 1467-1470.

[7] Hallgren RB, Litzenberg PH. TOM3 capacitance model: Linking large-and small-signal MESFET models 206 in SPICE. IEEE T Micro Theory Tech 1999; 47: 556-561.

[8] Rizk M, Saleh M, Aboulsoud A, El-Sherif A. A new analytical model of GaAs MESFET's: DC and sensitivity analysis. In: Proceedings of the 35th Midwest Symposium on Circuits and Systems, Washington, DC, USA. New York, NY, USA: IEEE; 1992. pp. 404-407.

[9] Rodriguez-Tellez J, Mezher K, Al-Daas M. Improved junction capacitance model for the GaAs MESFET. IEEE T Electron Devices 1993; 40: 2083-2085.

[10] D'Agostino S, Berutto AB. Physics based expressions for the nonlinear capacitances of the MESFET equivalent circuit. IEEE T Micro Theory Tech 1994; 42: 403-406.

[11] Bose S, Kumar A, Simrata, Gupta M, Gupta RS. A complete analytical model of GaN MESFET for microwave frequency applications. Microelectron J 2001; 32: 983-990.

[12] Murray S, Roenker K. An analytical model for SiC MESFETs. Solid-State Electron 2002; 46: 1495-1505.

[13] Ahmed MM. An improved method to estimate intrinsic small signal parameters of a GaAs MESFET from measured DC characteristics. IEEE T Electron Devices 2003; 50: 2196-2201.

[14] Aggarwal SK, Gupta R, Haldar S, Gupta M, Gupta RS. A physics based analytical model for buried p-layer non-self aligned SiC MESFET for the saturation region. Solid-State Electron 2005; 49: 1206-1212.

[15] Neamen DA. Semiconductor Physics and Devices. New York, NY, USA: McGraw-Hill; 1997.

[16] Lv H, Zhang Y, Zhang Y, Yang LA. Analytic model of $I-V$ characteristics of 4H-SiC MESFETs based on multiparameter mobility model. IEEE T Electron Devices 2004; 51: 1065-1068.

[17] Roschke M, Schwierz F. Electron mobility models for 4H, 6H, and 3C SiC MESFETs. IEEE T Electron Devices 2001; 48: 1442-1447.

[18] Ladbrooke PH. MMIC Design: GaAs FETs and HEMTs. Boston, MA, USA: Artech House; 1989.

[19] Ahmed MM, Riaz M, Ahmed UF. An improved model for the $I-V$ characteristics of submicron SiC MESFETs by evaluating the potential distribution inside the channel. J Comput Elect 2017; 16: 514-525.

[20] Na HJ, Moon JH, Yim JH, Lee JB, Kim HJ. Fabrication and characterization of 4H-SiC planar MESFETs. Microelectron Eng 2006; 83: 160-164.