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Energy efficiency in CMOS power amplifier designs for ultralow power mobile wireless communication systems

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Abstract: Wireless communication standards keep evolving so that the requirement for high data rate operation can be fulfilled. This leads to the efforts in designing high linearity and low power consumption radio frequency power amplifier (RFPA) to support high data rate signal transmission and preserving battery life. The percentage of the DC power of the transceiver utilized by the power amplifier (PA) depends on the efficiency of the PA, user data rate, propagation conditions, signal modulations, and communication protocols. For example, the PA of a WLAN transceiver consumes 49% of the overall efficiency from the transmitter. Hence, operating the PA with minimum power consumption without trading-off the linearity is vital in order to achieve the goal of fully integrated system-on-chip (SoC) solution for 4G and 5G transceivers. In this paper, the efficiency in CMOS PA is discussed through the review of multifarious efficiency enhancement techniques in CMOS PA design. This is categorized into the review of efficiency in fundamental classes of PA in which Class E achieves the highest efficiency of 67%, followed by complex architectures utilized to enhance the efficiency level of the PA in which the outphasing architecture achieved the highest efficiency of 60.7%.

Key words: Efficiency, radio frequency, power amplifier, CMOS, wireless, 4G, 5G, system-on-chip

1. Introduction

Radio frequency (RF) wireless communication is broadly utilized in a myriad of devices such as cell phones, computers, and satellites. An RF communication system consists of transmitters and receivers (transceivers). The toughest part in transceiver design is designing the power amplifiers due to their inherited high-power consumption as compared to other blocks. For practical IEEE 802.11a WLAN transceivers, the power amplifier (PA) dominates 49% of the total power consumed by the transmitter as compared to other blocks [1]. The transmit-power of 8% is included in the power consumption of the PA while other blocks such as digital-to-analog converter and digital signal processor consumes up to 6% and 25%, respectively.

Currently, for mobile handset applications the PAs are designed by utilizing costly III-V compound semiconductors because they tend to deliver higher linear output power as compared with silicon due to reduced inherent parasitic effects [2]. All other blocks in the mobile transceiver are designed in CMOS which results in dual chip implementation solution. Dual chip implementation is costly and time-consuming when it comes

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to mass production. Hence, studies on mobile handset transceivers are exploring the possibility to implement the mobile wireless transceivers as CMOS system-on chip (SoC). In addition, as the era of communication has evolved from 3G-WCDMA to 4G-LTE, the requirement for PAs with high efficiency for mobile communication has been growing. Due to the need for optimizing the battery life, mobile communication demands PAs that are more efficient with maximum linear output power. In the primary attempt, several studies reported watt-level CMOS PAs with power combining techniques, assisted by distributed elements [3].

Despite these achievements, the efficiency remains low; thus, the goal to achieve a fully integrated SoC remains an arduous challenge. The oftentimes utilized PAs can be categorized as current mode PAs and switch mode PAs. The typical current mode PAs are Class A, B, AB, and C. Other than that, Class D, E, and F serve to be switch mode PAs. The efficiency for PA is defined as the ratio between RF output power transmitted to the DC power used by the PA. Drain efficiency and power added efficiency (PAE) are the parameters utilized to evaluate its efficiency. Drain efficiency and PAE is as given in (1) and (2), respectively.

$$\eta(\%) = \frac{P_{out}}{P_{dc}}(100) \tag{1}$$

$$PAE(\%) = \frac{P_{out} - P_{in}}{P_{dc}}(100) \tag{2}$$

where P_{out} represents the RF power transmitted, P_{in} is the RF input power supplied, and P_{dc} is the DC power consumed by the PA.

Several efficiency enhancement techniques have been implemented recently as a method to further ameliorate the efficiency performance of the CMOS PA for the given classes. This review is organized as follows. Section 2 reviews the efficiency in various fundamental classes of CMOS PAs frequently implemented in wireless communication. Section 3 presents the current research output in enhancing efficiency of the CMOS PA. Further continued by a conclusion in Section 4.

2. Efficiency in fundamental CMOS PA classes

2.1. Class AB PA

The time period that a Class AB PA operates in saturation region is in between Class A and Class B where the drain current conduction angle is between 180° and 360°. Therefore, class AB has characteristics of hybrid Class A and Class B. During weak input signal, Class AB PA works in Class A mode, alternately, significant increment in the input signal shall drive the PA to operate in Class B mode. Figure 1 depicts the common structure of CMOS Class AB PA. L2 and C3 are the parallel resonant circuit that resonates at operating frequency.

When Class AB PA is in operation, the drain current IDD is given as:

$$I_{DD} = \frac{I_o}{\pi}(sin\theta - \theta cos\theta) \tag{3}$$

where I_o is the amplitude of the output AC current and θ is the half conduction angle.
The I_{DD} amplitude at fundamental frequency is:

$$I_f = \frac{I_o}{2\pi}(2\theta - sin(2\theta)) \tag{4}$$

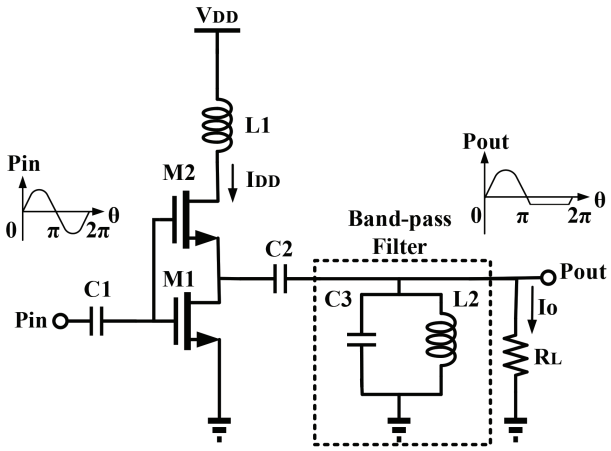

Figure 1. CMOS Class AB PA structure.

The transmitted output power for Class AB PA is given by:

$$P_{out} = \frac{R_L I_o I_f}{4\pi}[2\theta - sin(2\theta)] \tag{5}$$

The DC power consumed for Class AB PA is defined as:

$$P_{dc} = I_{DD} V_{DD} = \frac{V_{DD} I_o}{\pi}(sin\theta - \theta cos\theta) \tag{6}$$

Therefore, the efficiency of this PA can be derived as:

$$\eta(\%) = \frac{P_{out}}{P_{dc}}(100) = \frac{I_f R_L[2\theta - sin(2\theta)]}{4V_{DD}(sin\theta - \theta cos\theta)}(100) \tag{7}$$

The theoretical efficiency of the Class AB PA is about the efficiency of Class A (50%) and Class B (78.5%). The practical efficiency of CMOS Class AB PA achieved is about 55% [4].

2.2. Class E PA

Class E PA is also known as the switch mode PA which are classified into zero-voltage switching (ZVS) and Zero-current switching (ZCS) scheme. Ideally, the drain current and voltage of Class E PA would not emerge at the same time. This gives the Class E PA 100% DC power conversion efficiency. However, the practical efficiency achieved in CMOS Class E PA is only 67% due to conduction and switching losses [5]. The configuration of the CMOS Class E PA is depicted in Figure 2. L2 and C4 are the series resonant circuit while C2 is the shunt capacitor. The shunt capacitor, C2 charges and discharges during the ON/OFF transition of the transistors. Since C2 does not allow instant changes in drain voltage, it generates smooth transition between the ON/OFF transitions of the transistor.

Class E PA efficiency is given by:

$$\eta(\%) = \frac{1}{1 + \frac{1.4 r_{on}}{R_L}}(100) \tag{8}$$

where r_{on} is the on-resistance of the switching transistor.

Class E PA is widely utilized in Bluetooth system [6], WCDMA and WiMAX applications [7], surface-to-orbit proximity link microtransceiver [8], long-term evolution (LTE) applications [9], and wireless sensor network (WSN) [10].

2.3. Class F PA

For Class F PA, the output circuit controls the harmonic components of the voltage or current. If all harmonic components are considered, the theoretical DC power conversion efficiency would be 100%. In practical approach, the designs are restricted to 3rd harmonic termination which restrains the theoretical maximum efficiency of the PA up to 75%. However, the practical efficiency achieved in CMOS Class F PA is 56% [11]. Figure 3 delineates the typical structure of a CMOS Class F PA with 3rd harmonic termination provided by L2 and C3. C4 and L3 are the parallel resonant circuits. By considering only the 3rd component, the power transmitted to the load is given by:

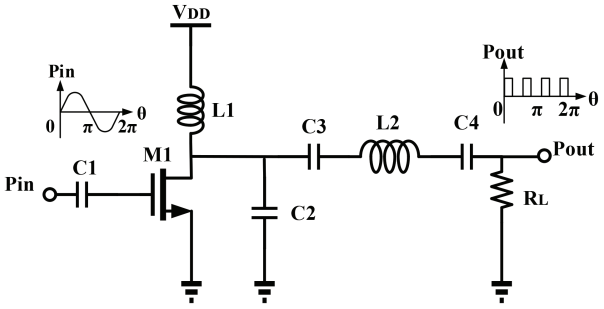

Figure 2. CMOS Class E PA structure.

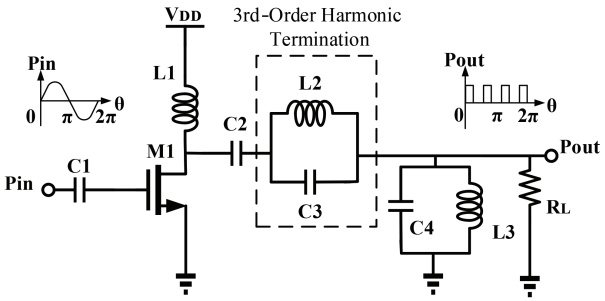

Figure 3. CMOS Class F PA structure.

$$P_{out} = \frac{81V_{DD}^2}{128R_L}(100) \tag{9}$$

The DC power consumed is given by:

$$P_{dc} = \frac{9V_{DD}^2}{4\pi R_L}(100) \tag{10}$$

The efficiency of the PA is given by:

$$\eta(\%) = \frac{P_{out}}{P_{dc}}(100) = \frac{9\pi}{32}(100) \tag{11}$$

Table 1 delineates the ideal and practical efficiency between various PA classes.

Table 1. Performance comparison of various classes of CMOS PA.

Class	Modes	Ideal Efficiency	CMOS PA Efficiency	Ref.
AB	Current source	50%–78.5%	55%	[4]
E	Switch	100%	67%	[5]
F		100%	56%	[11]

3. Efficiency enhancement techniques in CMOS PA

3.1. On-chip transformer PA

Several exertions have been made to utilize the structures and layout of on-chip transformers to integrate it with the PAs. A transformer has multiple features which are impedance matching, differential to single-ended balun, and it provides DC isolation along with ESD protection. Transformer combination structures can be categorized according to the ways they are combined at the load. Some of the transformer structures include series-combining transformers (voltage mode) and parallel-combining transformers (current mode) [12]. Parallel-combined transformer shows 50% improvement in efficiency with increasing primary windings as compared to series-combined transformer. Figures 4 and 5 depict the transformer combination structures.

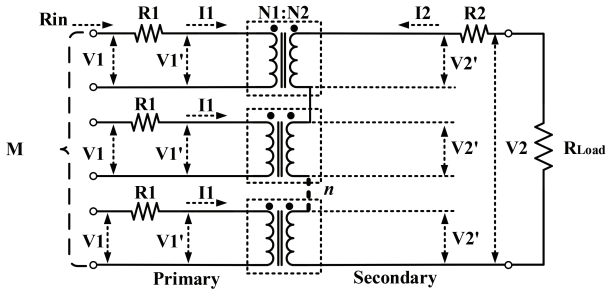

Figure 4. Series transformer combination structure.

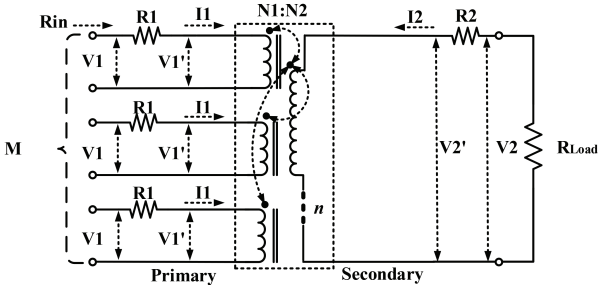

Figure 5. Parallel transformer combination structure.

In series combination, the secondary coils of n transformers are connected in series configuration, which results in voltage addition at the secondary side and thus produces more output power. At each amplifier, the impedance seen is n times higher than that of directly connected to the load. This benefits the driver design and reduces the layout parasitics from the primary side. A symmetrical physical layout must be obtained to alleviate maximum output power and efficiency [13].

The first implementation of an integrated CMOS PA with on-chip input and output matching was achieved by Aoki et al. (2001) by using a series combination transformer [14]. The series-combining distributed active transformer (DAT) architecture functions as a matching network and a power combiner which produces a solution with high efficiency [15]. However, it occupies a large on-chip active area. A power combining method using monolithic voltage-boosting parallel-primary transformer was suggested by AN et al. [16] for a fully integrated CMOS PA. This design gives voltage-boosting effect when the primary to secondary loop turn ratio is increased. Moreover, the current in the secondary loop can be increased by parallely interweaving the multiple primary loops. An efficient power combining method has been produced monolithically by increasing the voltage and current of the secondary loop.

To combine the output of several amplifiers, 1:1 transformers were utilized in series combination [17]. It can also be used for power control since each transformer can be switched off independently. As presented by Afsahi et al. [18], the signal can also be combined in parallel which gives improved signal symmetry and minimizes loss on the secondary side. However, the number of turns in the secondary side increases, which lowers the self-resonance frequency and increases the area as compared to series combining technique. Javidan et al. [19] achieved an implementation with a 40% smaller fingerprint as compared to Afsahi et al. [18] and still attained good performance by using a transformer with different sizes.

Furthermore, the interleaved transformer structure produces better performance in terms of efficiency as compared to 1:1 planar transformers as reported by Belabad et al. [20]. The interleaved structure reduces the self-inductance and the quality factor while it increases the coupling coefficient of the transformer which is suitable for transferring current. An enhanced efficiency is contributed by the high coupling coefficient and low parasitic impedance characteristics of the interleaved structure. As shown in the schematic in Figure 6, the interleaved transformer consists of 2 input ports (P1, P2) and 1 output port (P3). The output port of the transformer is connected to the load and the input ports of the transformer are connected to the drain of the PA. The transformer efficiency was ameliorated by interleaved method compared to 1:1 transformer method. Figure 7 depicts the layout structure of the interleaved transformer.

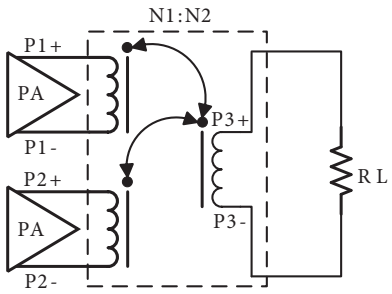

Figure 6. Configuration of $2 \times 1{:}2$ interleaved transformer.

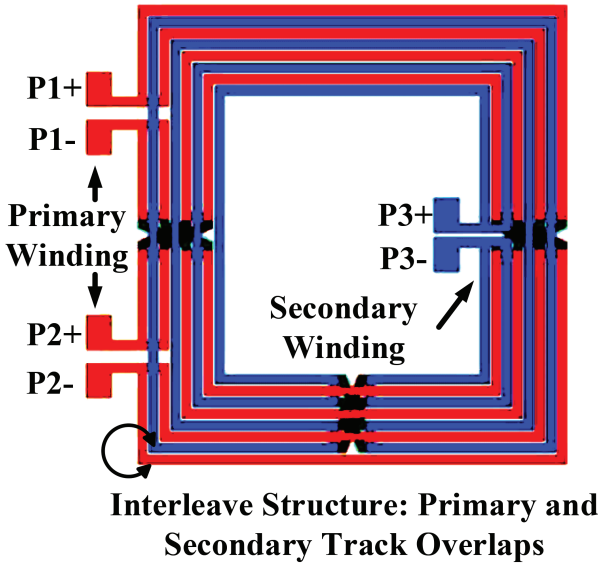

Figure 7. Top view of $2 \times 1{:}2$ interleaved transformer.

In addition, CMOS PAs with autotransformers were proposed in order to enhance the efficiency in a compact die area [21, 22]. Ahn et al. [23] recently proposed a dual mode autotransformer based parallel combining transformer (ABPCT) which offers high-efficiency performance. The ABPCT PA consists of a single PA, PA_A, that is connected on the secondary winding. In the primary windings, multiple PAs such as PA_B and PA_C are connected independently. For high power mode, all the PAs are enabled while in low power mode, one or two PAs are selectively enabled. The PA achieves PAE of 34.4% and 38.1% in LP mode and HP mode respectively.

Figure 8 depicts the schematic structure of the designed ABPCT PA. In Figure 8, X3 represents PA_A, PA_B, and PA_C. Each amplifier has a transformer that serves as the input matching. At the output, the ABPCT also functions as the matching network. The gate bias of each PA is tuned to select the LP and HP operation modes. For LP mode, the PA_A biasing is reduced from Class AB biasing to deep Class AB biasing, which results in reduction of DC power consumption.

On-chip transformers are suitable for high-power applications since they are advantageous in generating high output power by integrating multiple number of PAs in a single chip and reduces the need of multiple matching networks for impedance transformation. The disadvantage of an on-chip transformer is that it consumes a large chip area for a single passive component and it is affected by the passive losses in silicon substrate. Thus, it is advisable to implement it with reduced gate length process technology (130 nm and below) to have beneficial performance particularly at high frequency.

PA designers shall be mindful when selecting the passive components such as the transformers, inductors, and capacitors for their circuit. For inductors and transformers, metal thickness contributes to passive Q factor that reduces power loss in the PA. For example, in 130 nm CMOS process, the 23 kA metal is preferred to be used for the inductor or transformer. Further improvement in Q factor can be obtained by selecting inductors or transformers with patterned ground shield. For transformers, interleaved configuration have better coupling and Q factor on the secondary side since both primary and secondary winding uses thick top metal as compared to stacked configured transformers where the secondary winding uses lower metals with lower thickness. For capacitors, metal-insulator-metal (MIM) capacitors can be utilized when high capacitance value is required and metal finger capacitors can be used when low capacitance value is required. To increase the capacitance per area, 4 layers MIM capacitors are suggested to be used.

3.2. Doherty PA (DPA)

The Doherty power amplifier (DPA) consists of a carrier and a peaking amplifier. The backed-off efficiency of the amplifier is enhanced by varying the load impedance. This can be achieved by utilizing a current source at the output terminal. The concept of Doherty PA is illustrated in Figure 9 [24].

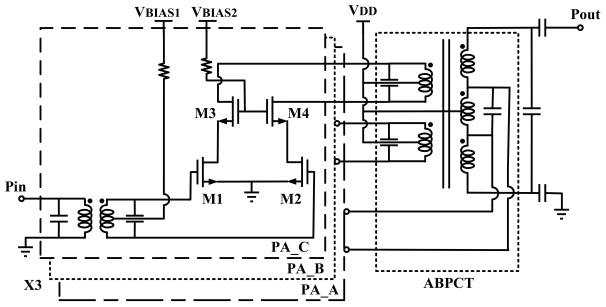

Figure 8. The schematic of ABPCT CMOS PA.

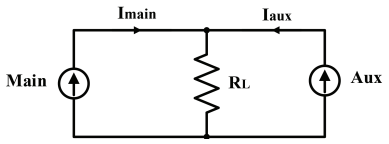

Figure 9. The concept of Doherty PA.

Referring to Figure 9, "Aux" is the auxiliary amplifier while "Main" denotes the main amplifier. When the auxiliary amplifier is idle, the main amplifier will see a load resistance of R_L. Meanwhile, when the auxiliary amplifier is on and produces current I_{aux}, the main amplifier sees load impedance as given in (12). From (12), it can be comprehended that the source current (I_{aux}) of the auxiliary amplifier can be changed to vary the load impedance of the main amplifier to enhance the backed-off efficiency.

$$Z_{MAIN} = R_L \left(1 + \frac{I_{aux}}{I_{main}}\right) \tag{12}$$

By utilizing the Doherty structure in CMOS, a constant efficiency across output power can be achieved as demonstrated by N. Deltimple et al. [25]. Another method proposed was by Hu et al. [26]; it adopted a hybrid Class G Doherty PA configuration in CMOS to increase the efficiency at deep backed-off power. The Class G and Doherty combination operation improves the deep backed-off efficiency without additional complexity at the input and output RF passive networks. The series Doherty power amplifier (SDPA), as presented by Levy et al. [27], achieves more output power than that of the conventional Doherty PA. In SDPA, the load voltage can be twice as high as the voltage of either amplifiers separately due to the parallel load impedance with the peaking amplifier. In order to obtain a backed-off efficiency performance close to Class B operation, the main amplifier is biased in deep Class AB operation.

Additionally, a highly efficient fully integrated CMOS Doherty PA was designed by Traiche et al. [28]. The designed Doherty PA has 2 parallel amplifiers in which the main amplifier and auxiliary amplifier had been designed in Class AB and B, respectively. The 2 structures adopt cascode configuration for its high supply voltage characteristic and high input-output isolation. Figure 10 depicts the schematic of the aforementioned DPA design. As shown in the schematic, a Wilkinson divider is utilized in the design which consists of lumped elements R0, C1, C2, C3, L1, and L2. For the transmission line design, a PI network consisting of (C5, C6, L4) and (C11, C12, L13) integrates the dephasing circuit and impedance inverter respectively. The branches of (C9, L9) and (C10, L10) are the resonant circuits used to eliminate the harmonics.

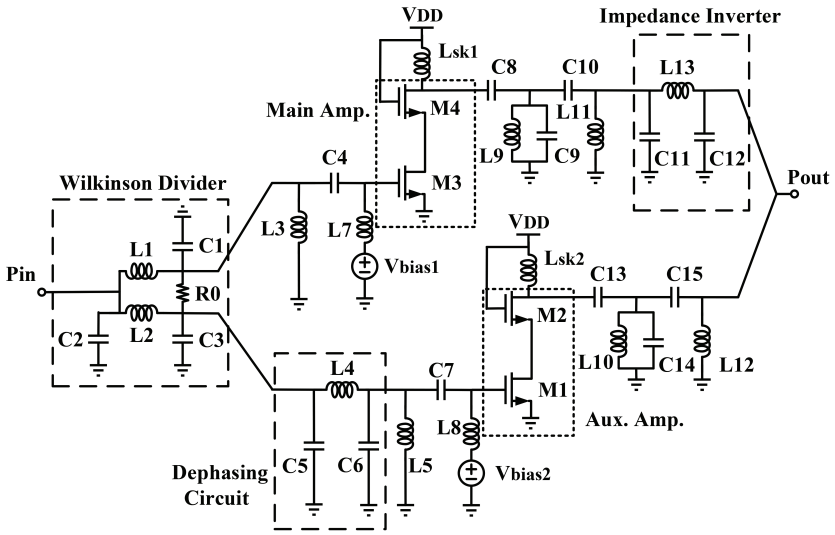

Figure 10. The schematic of the designed Doherty PA.

The Doherty PA has its simplicity since no complex circuitry is reacting to the input signal as compared to envelope tracking method. Moreover, lumped and distributed impedance inverters are possible to be implemented. Both the impedance inverter and the power splitter as well as the delay compensation can be implemented by utilizing the lumped and distributed approaches. However, the presence of the power splitter and combiner contributes to the increased losses in RF path. Moreover, the RF paths required to be synchronized with high precision where the main and auxiliary RF path delays must be equivalent for high efficiency. It also consumes large chip area since the architecture uses a power splitter at the input and a power combiner at the output. The DPA is only suitable for narrowband applications due to the nature of the $\lambda/4$ microstrip impedance inverter which has limited bandwidth.

3.3. Envelope tracking PA

The envelope-tracking (ET) design is originated based on the envelope elimination and restoration (EER) technique introduced by Kahn [29]. In EER, the amplitude modulation to phase modulation (AM-PM) distortion was eliminated by preserving the phase modulation of the input signal. Meanwhile, the amplitude modulation of the input signal was utilized to modulate the voltage supply of the PA in order to enhance the efficiency at backed-off output power. Figure 11 shows the envelope tracking (ET) topology [30].

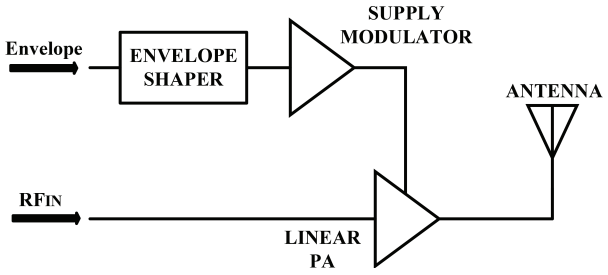

Figure 11. ET PA topology.

Initially, for ETPA the maximum linear output power is achieved by matching the load resistance of the PA. When the output power is gradually decreased, the supply voltage also reduces with respect to the drive voltage. As a result, the back-off efficiency is improved. A dynamic stacked CMOS PA is designed by Woo et al. [31] to improve the efficiency of the ETPA for low-voltage operation. The efficiency of the ETPA with maximum voltage of 3.4 V is comparable with works utilizing GaAs HBT with 5 V headroom, which made it favorable. Subsequently, Park et al. [32] reported a CMOS PA with enhanced envelope tracking supply modulator. By implementing this modulator, higher efficiency at all power levels has been achieved. This CMOS PA also utilizes 2nd harmonic control circuits at the input and the output of the PA to enhance efficiency. Ham et al. [33] proposed a CMOS PA with dual-mode supply modulator which is utilized for envelope tracking (ET) and average power tracking. The dual-mode supply modulator is based on hybrid buck converter that consists of a switching amplifier and a wideband linear amplifier. In ET mode, PA is capable to achieve an efficiency of 45.4%. The schematic of the CMOS ETPA is depicted in Figure 12.

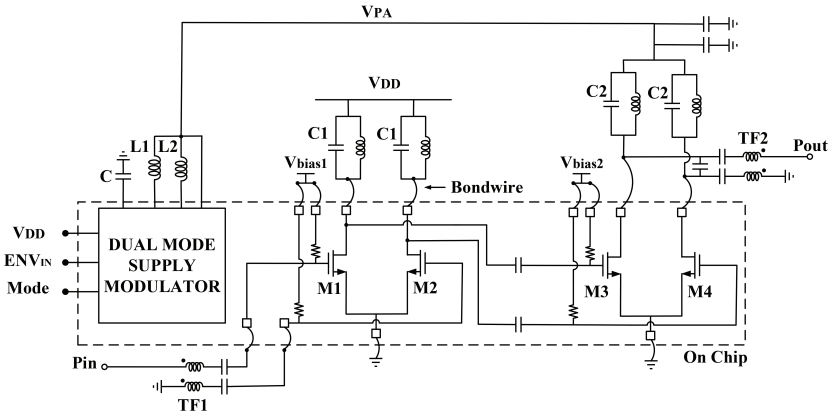

Figure 12. Circuit schematic of the designed CMOS ET transmitter.

Referring to Figure 12, the PA has a differential common source structure and a deep Class AB operation biasing in order to achieve high efficiency. External passive components and a 1:1 transformer is utilized to achieve proper load match as well as to realize a differential to single-ended conversion. For both PA stages, the second harmonics are terminated using series resonance between the bond wire and a capacitor (C1, C2) at the drain terminal to improve the efficiency.

For ETPA, various envelope detection methods using analog domain and digital signal processor can be implemented. Different architecture variations such as linear, switching, and adaptive biasing techniques can be chosen by the designers for the ETPA regulator. Albeit, highly precised synchronization between the PA and the regulator is required. The RF path and the regulator must be in-phase, as the supply voltage must follow the envelope in order to attain maximum efficiency. In addition, utilization of switching regulators generates noise in the supply rail of the PA and at the same time limits its operating bandwidth. Thus, ETPA is suitable for narrow-band applications such as the LTE Band 1 which has 60 MHz bandwidth.

3.4. Outphasing PA

In outphasing PA, the signal with amplitude modulation is represented as the vector sum of two constant envelope phase-modulated signals. By modulating differential phase with the input signal amplitude held constant, an enhanced efficiency is achieved. In outphasing technique using nonlinear components, the amplitude modulation is achieved by combining the outputs of two PAs which are supplied with constant envelope phase modulated signals [34–38]. The structure of the outphasing and its principle of operation are depicted in Figure 13. The amplitude and phase modulated signal in (13) can be separated into 2 constant amplitude phase modulated signals ($S_1(t)$ and $S_2(t)$) as defined in (14) and (15):

$$S_{out}(t) = A(t)cos(\omega_c t + \phi(t)) \tag{13}$$

$$S_1(t) = \frac{A_{max}}{2} cos(\omega_c t + \phi(t) + \theta(t)) \tag{14}$$

$$S_2(t) = \frac{A_{max}}{2} cos(\omega_c t + \phi(t) - \theta(t)) \tag{15}$$

where $S_{out}(t) = S_1(t) + S_2(t)$, $A(t)$ is the time-dependent amplitude and $\phi(t)$ is the time-dependent phase of the original signal $S(t)$, ω_c is angular frequency of the carrier, A_{max} is the maximum value of $A(t)$, and the outphasing angle $\theta(t)$ is defined as:

$$\theta(t) = cos^{-1} \frac{A(t)}{A_{max}} \tag{16}$$

As $S_1(t)$ and $S_2(t)$ are constant envelope phase modulated signals, the amplification can be done by using nonlinear switch mode PA that has high efficiency. A combiner circuit is utilized to combine the outputs of the PA in order to obtain $S_{out}(t)$, which is the amplified original signal $S(t)$. The block diagram of the outphasing PA architecture is presented in Figure 14. A RFDAC-based outphasing PA with an integrated combiner was presented by Hu et al. [39]. The high-efficiency operation was obtained by using a dynamic amplitude control in quasiload insensitive Class E performance. The amplitude control is achieved by a digitally divided approach for the branch amplifier. By utilizing this method, the power losses can be minimized by avoiding the highly reactive and extreme loading modulation conditions as in the conventional outphasing operation.

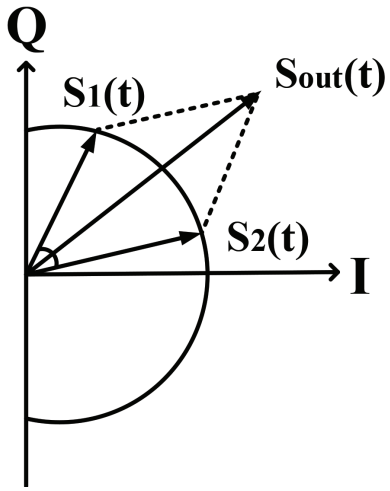

Figure 13. Operation principle.

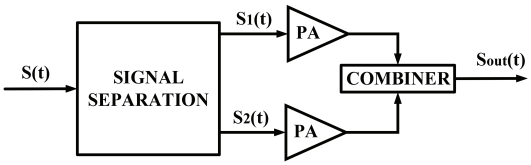

Figure 14. Outphasing architecture.

Moreover, a CMOS Class D PA with on/off control logic method for multilevel outphasing transmitter was proposed by Martelius et al. [40]. There are 8 PAs with cascoded output stages utilized in this design. The PAs are turned on and off in pairs for different amplitude levels as a method of enhancing the back-off efficiency. Banerjee et al. [41] proposed a CMOS Class E outphasing PA with a new passive combining circuit that achieved high output power and efficiency. The combiner consists of a power enhancement circuit and efficiency enhancement circuit as a part of it. This is utilized to enhance the efficiency at back-off power and increases the output power respectively.

Ghahramani et al. [42] proposed a Class E outphasing PA by utilizing load-pull analyses which is utilized to rotate and shift power contours and also to rotate the efficiency contours. This method enhances the efficiency of the outphasing PA at deep back-off output power. The resonance frequency of the LC tank and duty cycle scaling factor are tuned accordingly to realize the rotation of efficiency contours and power contours. Figures 15 and 16 depict the schematics of the designed Class E PA and its combiner, respectively.

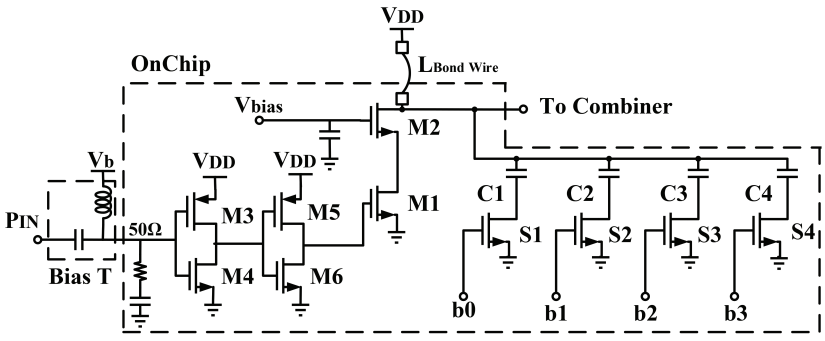

Figure 15. Schematic of the outphasing PA.

Referring to Figure 15, the Class E PA comprising transistors M1 and M2 act as a square-wave input signal driven switch, P_{IN} with angular frequency ω_0 and duty cycle of 50%. A high Q-factor parallel bond-wire, $L_{Bond\ Wire}$ is used as the dc-feed inductor for each PA (PA_1 and PA_2). Two cascaded inverters made up of

transistors M3 to M6, were utilized as the driver for the switch. The off-chip control voltage, V_b is used to control the duty cycle of the switch. The switched capacitor banks with 4 control bits (b0, b1, b2, b3) are utilized at the switching nodes to tune the relative resonance frequency of the LC tank of the branch PAs independently. The LC tank is realized by LBondWire and capacitors C1 to C4. Another LC tank (L0, C0) is a band-pass filter which filters out load current harmonics which further improves the efficiency.

The advantage of the outphasing PA is that it has an area-efficient architecture consisting of a signal component separator, two parallel amplifiers, and a power combiner. Furthermore, its efficiency can be enhanced by improving only the DSP algorithms without conducting any hardware changes. The drawback of the outphasing PA is that it requires a strict margin phase compensated power combiner in order to split and combine the RF signals accurately. This disqualifies common power combiners such as the Wilkinson. Plus, high precision synchronization is required between the parallel RF paths to achieve high efficiency. The power combiner restricts the bandwidth of the outphasing PA, makes it applicable for narrow-band applications only.

The efficiency performance of each techniques in recent studies is shown in Figure 17. It can be observed that all the techniques was able to achieve efficiency performance of more than 30%, with outphasing technique achieving the highest efficiency of 60.7%. The summarized performance of the assorted energy efficiency enhancement techniques is tabulated in Table 2. It can be observed that the output power of CMOS-based PAs is quite close in achieving a maximum output power of 1 W, with reduced power consumption. Doherty and outphasing PA are capable to be utilized for 5G New Radio applications which requires operating frequency of sub-6 GHz. Meanwhile, Doherty PA is also applicable for 5G millimeter wave applications since an operating frequency of 14 GHz has been achieved.

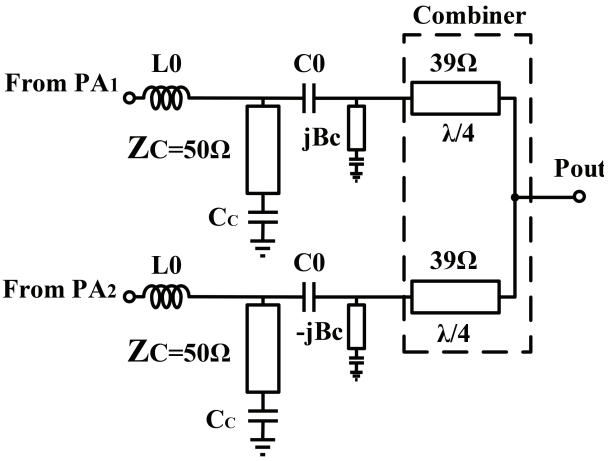

Figure 16. Schematic of the combiner.

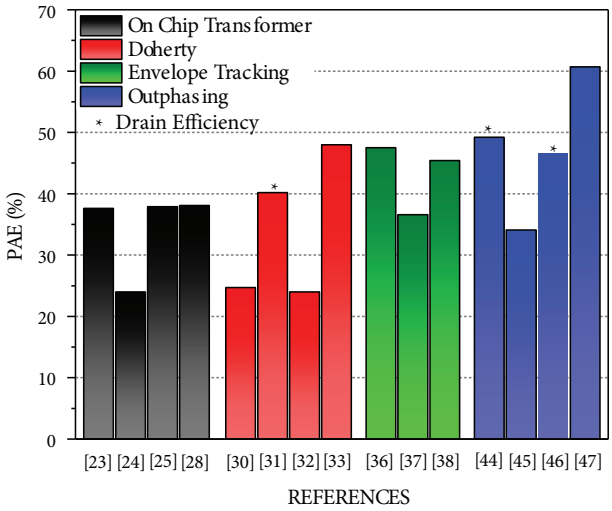

Figure 17. Summarized efficiency performances of various PA techniques.

4. Conclusion

In this review, the multifarious design methodology for CMOS PA has been discussed, starting from the fundamental configuration of the PA classes. The performance of the different classes of PA and topologies is analogized and tabulated. Each of the different topologies has its own advantages and disadvantages. As

Table 2. Comparison of PA topologies.

PA Configuration	Year	Technology	V_{DD} (V)	Freq. (GHz)	Max. P_{out} (dBm)	Peak PAE (%)	Gain (dB)	Ref.
On-chip Transformer	2010	65 nm CMOS	3.3	2.4	33.5	37.6	40.0	[18]
	2010	180 nm CMOS	3.3	0.9	29.5	24.0	-	[19]
	2013	180 nm CMOS	3.3	2.4	32.5	37.9	32.4	[20]
	2017	40 nm CMOS	2.8	1.75	24.7	38.1	5.9	[23]
Doherty	2015	65 nm CMOS	-	2.5	23.4	24.7	15.0	[25]
	2016	65 nm CMOS	3.0	3.71	26.7	40.2*	16.0	[26]
	2016	45 nm CMOS SOI	2.4	14.0	22.0	24.0	8.0	[27]
	2017	130 nm CMOS	2.6	3.0	26.0	48.0	17.0	[28]
Envelope Tracking	2014	320 nm CMOS SOI	3.4	0.837	25.9	47.5	26.6	[31]
	2016	180 nm CMOS	4.7	1.7	28.5	36.6	12.0	[32]
	2016	180 nm CMOS	3.3	0.78	24.0	45.4	24.1	[33]
Outphasing	2016	40 nm CMOS	1.2	5.9	22.2	49.2*	-	[39]
	2016	28 nm CMOS	3.6	1.8	32.4	34.1	-	[40]
	2017	45 nm CMOS	2.4	2.4	29.5	46.8*	-	[41]
	2018	65 nm CMOS	1.25	1.8	20.1	60.7	-	[42]

* Drain Efficiency

reviewed in this paper, lots of exertions have been done in the past decade towards enhancing the energy efficiency of CMOS-based PAs via circuit and architecture innovations. Further progress is still needed to be achieved as technology scaling tends to make the design of CMOS PAs even more exigent. Hence, it is expected that this field of study will assist to conserve energy for the betterment of future generation innovation of PAs.

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