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A low dropout voltage regulator with a transient voltage spikes reducer and improved figure of merit

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Abstract: An area efficient output capacitor-free low dropout [LDO] voltage regulator with an improved figure of merit is presented in this paper. The proposed LDO regulator consists of a novel, dynamically biased error amplifier that reduces overshoot and undershoot voltage spikes arising from abrupt load changes. Source bulk modulation is employed to enhance the current driving capability of the pass transistor. An adaptive biasing scheme is also used along with dynamic biasing to improve the current efficiency of the system. The on-chip capacitor required for proper working of the LDO regulator is only 35 pF. The proposed LDO regulator is designed and simulated in 180 nm standard CMOS technology. The LDO regulator exhibits a line regulation of 1.67 mV / V and a load regulation of 100 $\mu V/$mA. When load changes from 0 mA to 100 mA in 1 μs, an undershoot of 148 mV and an overshoot of 172 mV are observed. The measured power supply rejection ratio is 25 dB at 100 kHz. The working of the proposed LDO regulator has been tested under all process corners and Monte-Carlo statistical analysis reveals that it is robust against process variations and local mismatch.

Key words: Dynamic biasing, adaptive biasing, source bulk modulation, output capacitorless, figure of merit, low dropout voltage regulator

1. Introduction

Today's electronics market is dominated by battery operated devices. These devices need integrated power management circuits to meet the desired requirements. A typical power management system consists of switching regulators, linear regulators, voltage references, etc. Low dropout (LDO) regulators belong to the linear regulator category, which has better power efficiency, transient response, and noise immunity.

An LDO regulator is basically a negative feedback system in which the resistivity of the pass device is controlled by an error amplifier such that a constant voltage difference is maintained between input and output terminals even though there are fluctuations in supply voltage and load demand [1–3]. The vital performance indicators of LDO regulators are line and load regulation, maximum load current, transient response, on-chip capacitance value, stability, quiescent current magnitude, and power supply rejection ratio [PSRR] [4, 5]. It is practically impossible to improve all the parameters together. For example, if the quiescent current is reduced, transient response is hampered. Hence, a figure of merit [*FOM*] quantity is defined, which is a collective measure of the above-mentioned parameters. The objective of many recent LDO regulators has been to improve this *FOM*. Equation (1) defines the *FOM* used in [6, 7] and the smaller the *FOM* value, the better the performance.

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$$FOM = \frac{C_{out} \times \Delta V_{peak} \times I_Q}{I_{o,max}^2}, \tag{1}$$

where C_{out} is the output capacitance used in the design for stability and better transient response. ΔV_{peak} is the voltage spike observed when load current changes from minimum to maximum. I_Q is the quiescent current under no load condition. $I_{o,max}$ is the maximum load supplied by the LDO regulator.

Recently many have proposed different LDO regulator architectures and design techniques to improve *FOM* [7–11]. In [12] a local common mode feedback technique was used to increase the order of transfer characteristics, so that at low quiescent current better regulation could be achieved. However, while the line and load regulation were improved, the voltage spike during load transition was high. The author of [13] proposed an LDO regulator with small gain stages in which load was distributed between two pass transistors and on-chip capacitance was avoided. However, the observed line and load regulation were poor. A nested Miller capacitor-based LDO regulator was presented in [14]. Line and load regulation and transient responses were improved significantly but occupied a large area on the chip. A flipped voltage follower output stage was used in [15] to improve the response time and reduce the voltage spike during load transition. However, the LDO regulator was able to deliver only $10\,mA$ load. Another design technique to improve the transient response is to use multiple loops with different loop delays. Although this was adapted in [16], the achieved *FOM* value was very high. Better transient response can be achieved even with low quiescent current by having a dedicated voltage spike detection circuit that increases the quiescent current momentarily only when required. The author of [17] implemented this technique, and although the transient response was improved, the on-chip capacitor used was large and maximum driving load current was very low. The present work tries to improve *FOM* by adapting a novel dynamic biasing technique along with an adaptive biasing scheme and source bulk modulation. On-chip capacitance is kept very low so that area occupancy is significantly reduced. The rest of the article is arranged as follows. The structure and working principle of the proposed LDO regulator are explained in section 2. Stability analysis of the LDO regulator is outlined in section 3. The simulation results and discussion are elaborated in section 4. The conclusion is drawn in the last section.

2. Structure and operation of the proposed LDO regulator

The objective of the proposed LDO regulator is to improve the figure of merit and reduce the area occupancy. The area occupied by the LDO largely depends on the size of the on-chip capacitor. If the capacitance value is reduced to minimize the area, then transient response and stability are degraded. At the same time, to improve the *FOM*, quiescent current $[I_Q]$ and voltage spikes during abrupt load transition have to be reduced. Hence, the main focus is to improve transient response without using a large I_Q. Large I_Q is required only during abrupt load change and also the magnitude of I_Q should vary proportionately with respect to the magnitude of load current. Dynamic biasing addresses the former issue, whereas the adaptive biasing takes care of the latter. One more factor that affects the transient response is the large parasitic capacitance present at the gate of the pass transistor. This large size of parasitic capacitance is due to the large size of the pass transistor, which is required to accommodate minimum dropout voltage and maximum output current. The MOSFET source bulk modulation technique can reduce the threshold voltage so that the size of the pass transistor and associated parasitic capacitance can be reduced.

Figure 1 shows the schematic diagram of the proposed LDO regulator. Transistors from M_1 to M_9 form an error amplifier, which is basically an operational transconductance amplifier [OTA]. M_{5a}, M_{10}, R_3, C_3,

and I_{b1} constitute the undershoot voltage spike reducer block. M_{5b}, M_{11}, M_{12},M_{13}, R_4, C_4, and I_{b2} are part of the overshoot voltage spike reducer circuit. When output voltage suddenly drops due to a steep change in the load, C_3 and R_3 act as differentiator and $|V_{GS}|$ of M_{5a} momentarily increases, which provides large I_Q to charge parasitic capacitance; hence undershoot voltage is reduced. During this, the overshoot voltage spike reducer circuit will be in cut-off mode. Similarly, only the overshoot reducer is active during the overshoot of output voltage and reduces the voltage spike. The current mirror formed by M_{14} and M_{15} maintains the same drain voltage across the main pass transistor M_p and auxiliary pass transistor M_{pa}. The transistor pair M_{16} and M_{17} adaptively varies the bias point of the Schottky diode D_1 with respect to load current. In this way the magnitude of I_Q is controlled by the load current. The Schottky diode can be realized in standard CMOS technology [18]. Transistor M_{18} acts as a current buffer during instantaneous load transition. When load changes from minimum to maximum in a short period, voltages at the output and at the gate of M_{18} drop, forcing M_{18} to draw less current. In the meantime, the pass transistor steers this current to the output node. Hence, there is an improvement in transient response.

Table 1 shows the W/L ratio of all the MOSFETs and the values of passive components and bias currents used in the LDO regulator.

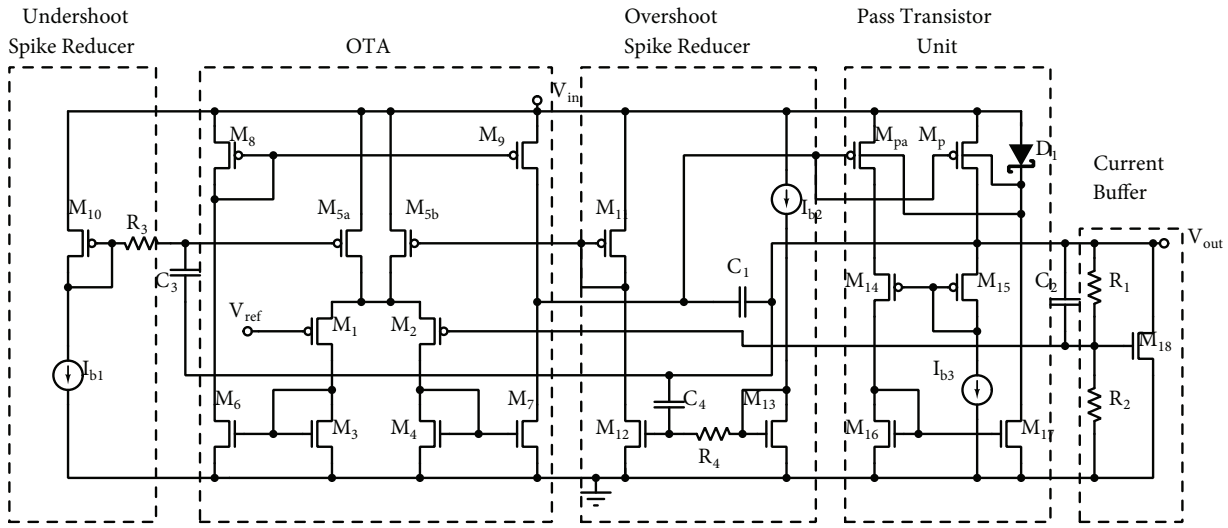

Figure 1. Schematic of the proposed LDO regulator.

3. Stability Analysis

Figure 2 shows the simplified small signal model of the proposed LDO regulator, where

$g_{m,ota}$, $g_{m,cb}$ $\rightarrow$ Transconductance of the OTA and current buffer transistor (M_{18}).

$g_{m,pass}$ $\rightarrow$ Total transconductance of the pass transistor.

$g_{m,usr}$, $g_{m,osr}$ $\rightarrow$ Transconductance of the undershoot spike reducer block and overshoot spike reducer block.

r_{ota}, r_{pass} and r_{cb} $\rightarrow$ Output resistance of the OTA, pass transistor, and M_{18}

C_{ota}, C_{pass} and C_{cb} $\rightarrow$ Parasitic capacitance of the OTA, pass transistor, and M_{18}

$R_o = r_{pass} \parallel r_{cb} \parallel (R_1 + R_2)$ $\rightarrow$ Total output resistance.

$C_{E1} = C_{ota} + C_1(1 + g_{m,pass}R_o)$ $\rightarrow$ Effective capacitance at output of OTA.

$C_{E2} = C_{pass}+C_1 + C_{cb}$ $\rightarrow$ Effective capacitance at the output of the pass transistor.

Table 1. Transistors' dimensions and passive components values.

Device	Parameter	Value
M_1, M_2, M_7, M_9	W/L	20/1
M_3, M_4, M_6, M_8	W/L	5/1
M_{5a}, M_{5b}, M_{10}, M_{11}	W/L	15/1
M_{12}, M_{13}	W/L	5/1
M_{14}, M_{15}, M_{16}, M_{17}	W/L	10/1
M_{18}, M_{pa}	W/L	1/0.2
M_p	W/L	7500/0.2
R_1	Resistance	40 $k\Omega$
R_2	Resistance	60 $k\Omega$
R_3, R_4	Resistance	100 $k\Omega$
C_1	Capacitance	5 pF
C_2, C_3, C_4	Capacitance	10 pF
I_{b1}, I_{b2}, I_{b3}	Current	5 μA

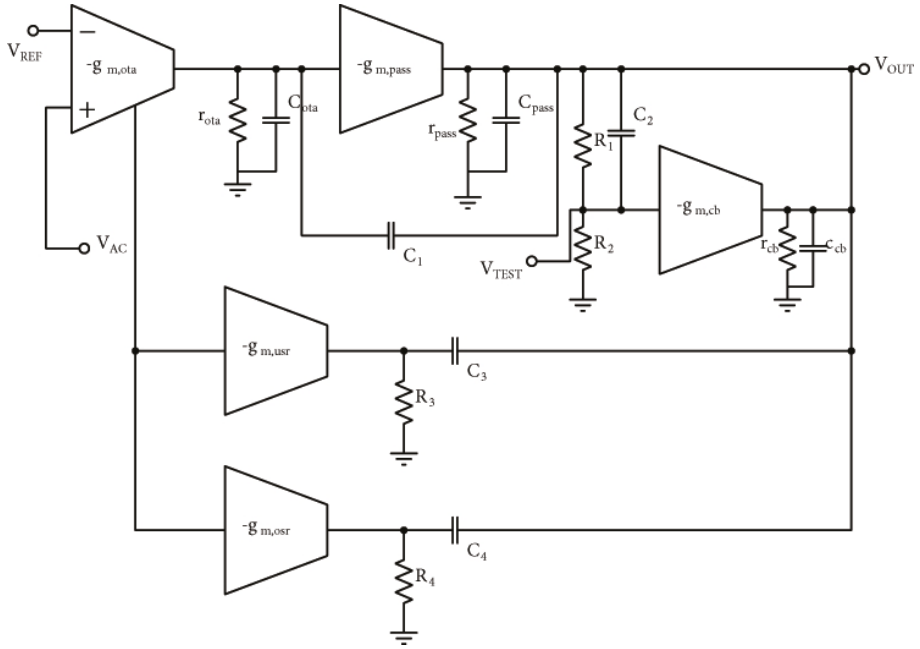

Figure 2. Small signal model of the proposed LDO regulator.

DC open loop gain can be derived from the small signal model as shown below:

$$V_1 = g_{m,ota} r_{ota} V_{AC}$$

$$V_{out} = \left(-g_{m,pass} V_1 - g_{m,cb} V_{TEST}\right) R_o$$

$$V_{out} = -g_{m,pass} g_{m,ota} R_o r_{ota} V_{AC} - g_{m,cb} R_o V_{TEST}$$

$$V_{TEST} = \frac{V_{out} R_2}{R_1 + R_2} = V_{out}\beta$$

$$= \beta(-g_{m,pass} g_{m,ota} R_o r_{ota} V_{AC}) - \beta(g_{m,cb} R_o V_{TEST})$$

$$\frac{V_{TEST}}{V_{AC}} = \frac{-\beta g_{m,pass} g_{m,ota} R_o r_{ota}}{1 + \beta g_{m,cb} R_o} \quad (2)$$

A 50-F capacitor is connected at the output node for simulation; it models the parasitic capacitance induced by bond wires and pads. The poles and zeros of concern when load current is 10 μA and 100 mA are shown in Figure 3 [a-d], respectively. All poles are located on the left half of the s-plane; hence the system is stable.

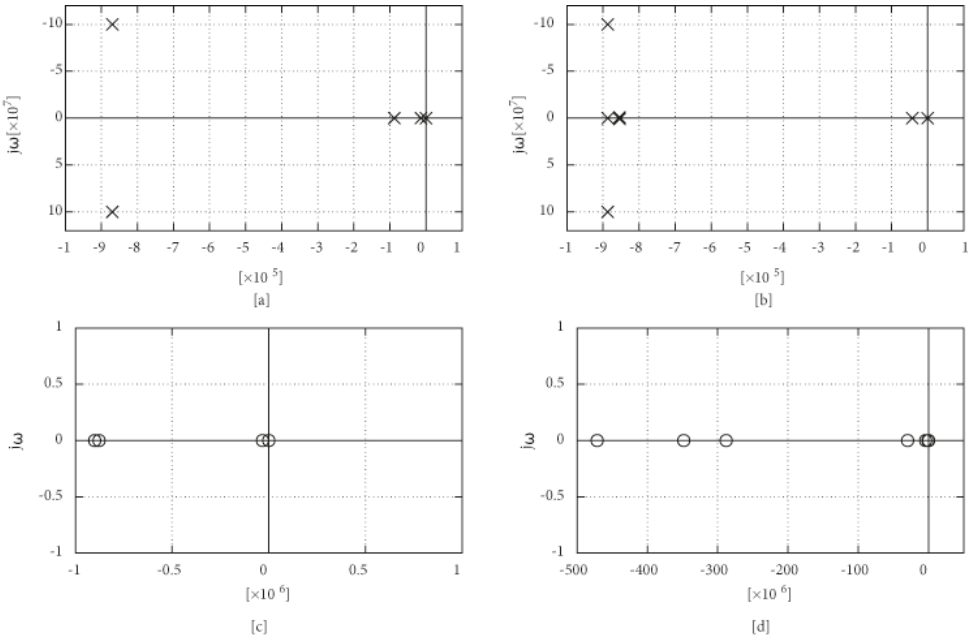

Figure 3. [a] Poles of the LDO regulator when I_L=10 μA, [b] poles of the LDO regulator when I_L=100 mA, [c] zeros of the LDO regulator when I_L=10 μA, [d] zeros of the LDO regulator when I_L=100 mA.

The loop gain response of the proposed LDO regulator was tested under different loads and process corners. Loop gain and phase responses in a typical corner are shown in Figures 4 [a,b]. Similarly, loop gain and phase responses of the LDO regulator in fast and slow process corners are shown in Figures 4 [c,d] and Figures 4 [e,f], respectively. It can be seen that phase margin is above 50° in all the cases, which in turn proves that the proposed LDO regulator is stable.

4. Results and Discussion

The proposed LDO regulator was laid out in 180 nm standard CMOS technology and postlayout simulation was carried out using BSIM v3.0 SPICE parameters. The obtained results for different performance parameters are explained in this section.

To measure the line regulation, input voltage was varied from 1.2 V to 2 V under different loads, 10 μA, 50 mA, and 100 mA. The average line regulation was 1.67 mV/V as shown in Figure 5 [a]. Load regulation of the LDO regulator under different process corners is shown in Figure 5 [b], where 'tt','ff, and 'ss' refer to the process corners, namely typical, fast, and slow corners. Fast and slow corners consider carrier mobilities that are higher and lower than the typical or nominal value specified in the model file, respectively. The observed load regulation was 100 $\mu V/$mA. To investigate the transient performance of the LDO regulator, a pulse of 100 mA load, of width 7 μs, and of rise and fall time of 1 μs was applied, considering the above-mentioned process corner cases. An undershoot of 148 mV and an overshoot of 172 mV were recorded; also output voltage was able to settle in 2 μs as shown in Figure 5 [c]. Similarly, keeping the load constant at 10 μA, 50 mA, and 100 mA, input voltage was changed from 1.2 V to 1.4 V for 6 μs with a rise and fall time of 1 μs. The LDO regulator

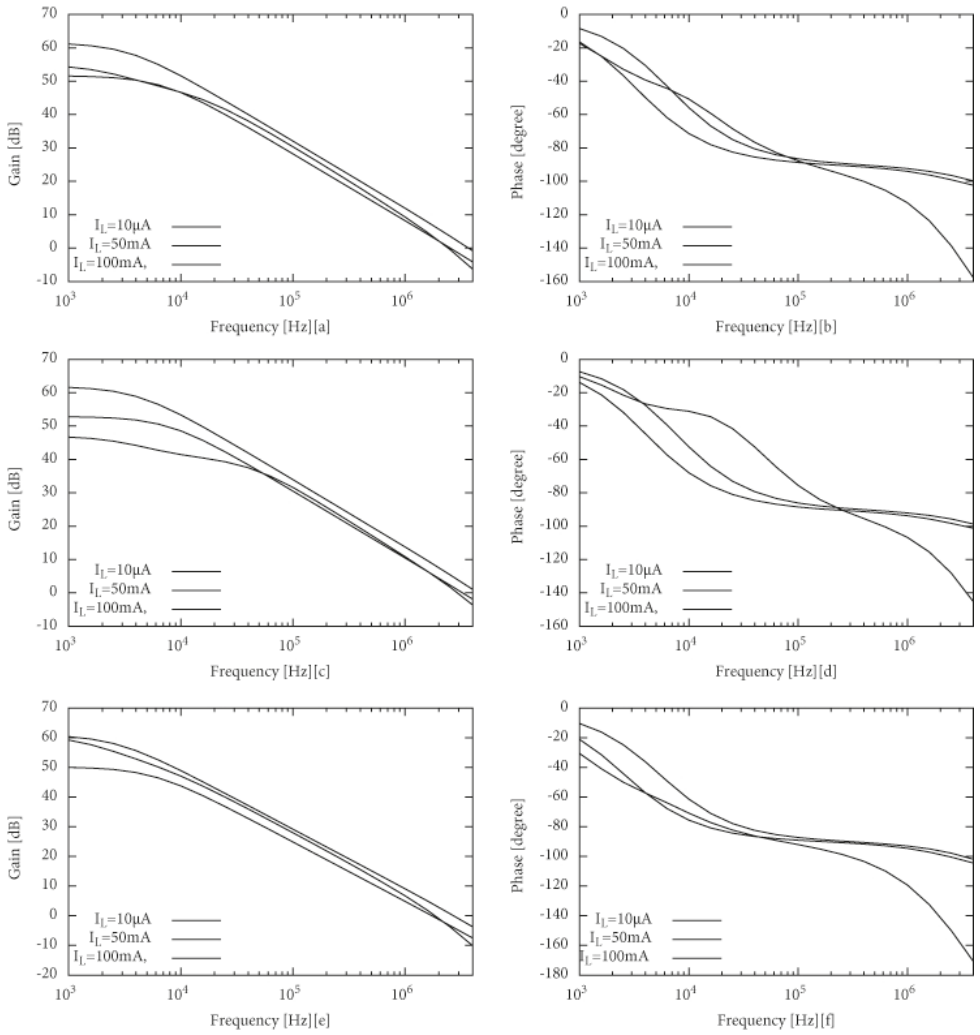

Figure 4. [a]&[b] Loop gain and phase response-typical corner, [c]&[d] loop gain and phase response-fast corner, [e]&[f] loop gain and phase response-slow corner.

response is shown in Figure 5 [d]. It can be seen that even under full load the voltage spike was within 80 mV.

To study the effect of temperature variation, the output voltage was measured for different temperatures ranging from 0° C to 100° C and typical (tt), fast (ff), and slow (ss) process corners. The LDO regulator output voltage was almost constant as shown in Figure 6 [a]. The PSRR of the LDO regulator is shown in Figure 6 [b]. When load was 100 mA, the PSRR was 25 dB at 100 kHz.

Monte-Carlo statistical analysis was carried out to find the effect of local and global parameter variations on the operation of the designed LDO regulator. Three key performance parameters, line regulation, load regulation, and undershoot voltage, during load transition were measured in the Monte-Carlo simulation. Threshold voltage and carrier mobility were considered for local mismatch and global variations. Totally 100 samples were taken and Gaussian distribution was assumed for varying the parameters. Figure 7 [a] shows the histogram plot of variation in line regulation for different samples. The mean value of line regulation was 1.51 mV/V. Histogram plots of variations in load regulation and undershoot spike voltage during load transition are shown in Figures 7 [b] and Figure 7 [c], respectively. The mean value of load regulation was 151.2 $\mu V/$mA

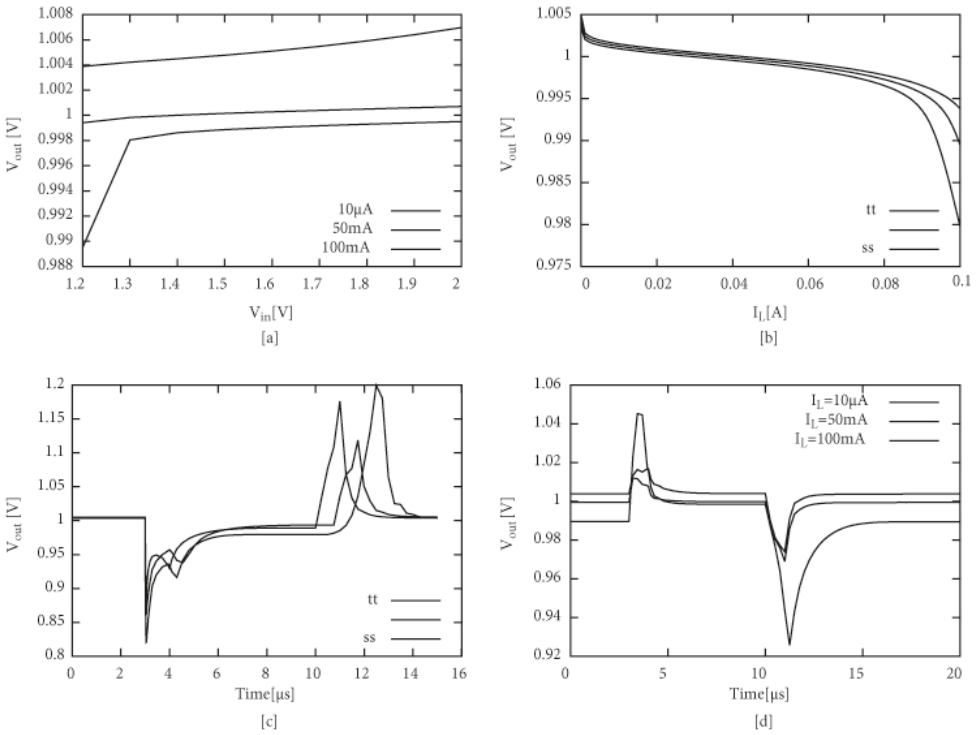

Figure 5. [a] Line regulation of the LDO regulator, [b] load regulation of the LDO regulator, [c] load transient response of the LDO regulator, [d] line transient response of the LDO regulator.

and undershoot voltage was 160.3 mV. In all three simulations the mean values of parameters match the typical values and also standard deviation was less. This shows that the proposed LDO regulator is robust against process variations and mismatch.The layout of the LDO regulator is depicted in Figure 8. The area occupied by the LDO regulator was 0.06253 mm^2.

The performance of the proposed LDO regulator has been compared with that of the recent state of the art LDO regulators as shown in Table 2. The table reveals that the proposed LDO regulator has a better current driving capability for the given quiescent current. The on-chip capacitance value of the LDO regulator is only 35 pF and hence the area occupied by it is very small. *FOM* is calculated using equation (1). From Table 2, it is evident that the proposed LDO regulator has the lowest *FOM* value.

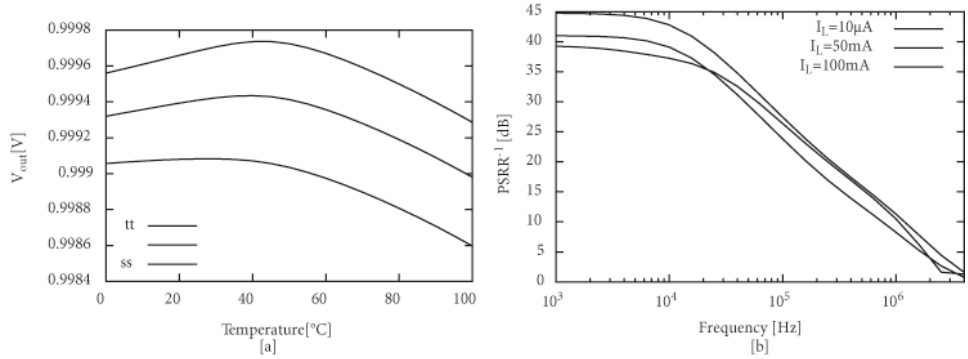

Figure 6. [a] Temperature response of the LDO regulator, [b] PSRR response of the LDO regulator.

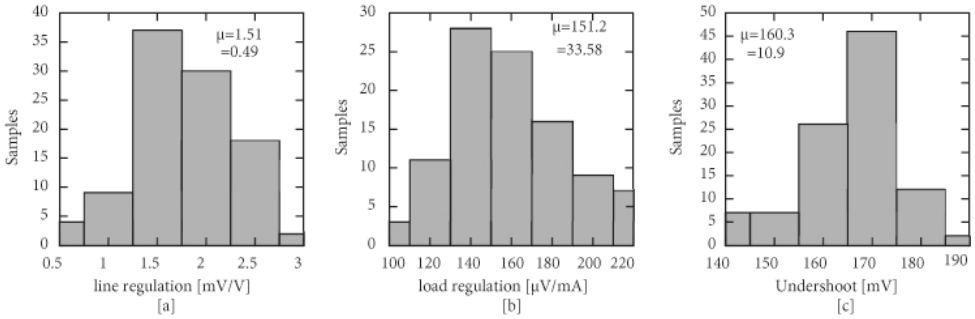

Figure 7. [a] Histogram plot of line regulation for different samples, [b] histogram plot of load regulation for different samples, [c] histogram plot of undershoot voltage for different samples when load changes from 0 mA to 100 mA.

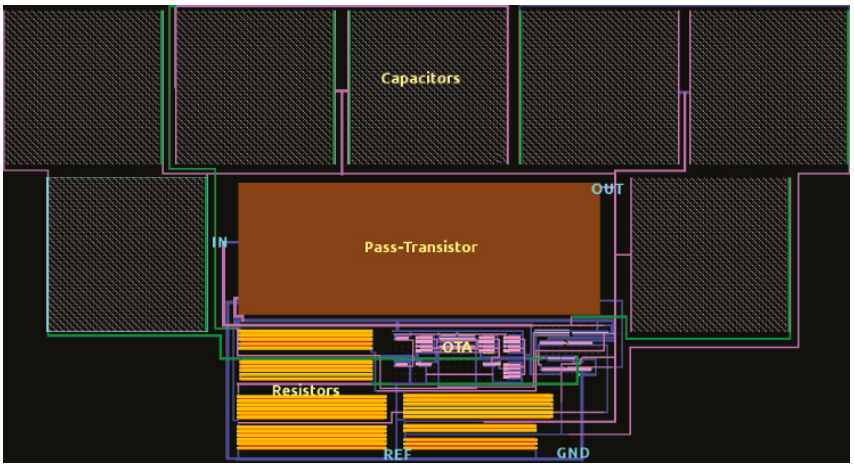

Figure 8. Layout of the LDO regulator.

Table 2. Performance comparison of the proposed LDO regulator with recent LDO regulators.

Parameters	[15]	[7]	[17]	[8]	[9]	[10]	[11]	[6]	**Present work**
Technology $[nm]$	65	90	180	350	65	350	350	500	**180**
V_{out}[V]	0.5	0.9	1.6	1	1	1.6	1	1.8	**1**
I_{max}[mA]	10	100	50	50	10	12	100	100	**100**
I_Q $[\mu A]$	49.4	6000	55	95	50	28.6	100	78	**65**
V_{drpout} $[mV]$	250	300	200	200	150	400	200	200	**200**
ΔV_{out}[mV]	41.6	600	120	180	82	40	50	135	**148**
$C_{on,chip}[pF]$	16	100	28	20	140	28	100	100	**35**
FOM $[fs]$	328.8	36000	73.92	136.8	5740	222.4	50	105.3	**33.15**

5. Conclusion

In this paper, an output off-chip capacitor-free, area efficient low dropout voltage regulator with improved *FOM* is presented. A novel dynamic biasing technique has been adapted, from which the LDO regulator is able to exhibit a better transient response without consuming a large quiescent current. With the help of source bulk modulation, the parasitic capacitance of the pass transistor has been reduced. For proper operation of the LDO regulator, only 35 pF on-chip capacitance is required; hence the area occupancy of the circuit is very low,

making it suitable for area constraint applications. Moreover, optimum performance can be achieved with the proposed LDO regulator because of its improved *FOM*.

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