Turkish Journal of Electrical Engineering & Computer Sciences

http://journals.tubitak.gov.tr/elektrik/

Research Article

Turk J Elec Eng & Comp Sci
(2020) 28: 509 – 524

doi:10.3906/elk-1905-26

Pulse width modulation control of fifteen-switch inverter for four AC loads

Gaurav GOYAL[1,*], **Mohan AWARE**[2]

[1]Department of Electrical Engineering, Shri Ramdeobaba College of Engineering and Management, Nagpur (M.S.), India

[2]Department of Electrical Engineering, Visvesvaraya National Institute of Technology, Nagpur (M.S.), India

Received: 06.05.2019 • **Accepted/Published Online:** 26.08.2019 • **Final Version:** 27.01.2020

Abstract: In many studies in the literature, various topologies with reduced switch count are proposed. With the use of these topologies, a lower number of semiconductor switches are required to produce a desired set of voltage. This in turn reduces the size and cost of the inverter. This paper proposes a new reduced switch count topology named "fifteen-switch inverter (FSI)", which is experimentally verified. The FSI has five switches in one leg and have three legs for three phases. It is capable of controlling four three-phase ac loads. In this proposed inverter topology, fifteen switches are used against the twenty four switches in conventional two-level inverter to control four ac loads. The proposed control is implemented using modified sinusoidal and space vector pulse width modulation techniques. A comparative performance of FSI with conventional sinusoidal pulse width modulation and space vector pulse width modulation are presented in linear operating region. The structure and the principle of operation of the proposed inverter are introduced and verified using simulation. The inverter prototype was built and the proposed inverter has been verified experimentally using digital signal controller. The experimental results verify the applicability of the proposed inverter and the employed pulse generation technique.

Key words: Common frequency mode, fifteen-switch inverter, sinusoidal pulse width modulation, space vector pulse width modulation

1. Introduction

The main area in today's research in the field of power electronics is to have converter which has less cost, minimum components, with high reliability and efficiency. Many topologies had been proposed for motor drive application for component minimization [1-6] , such as two level and three-level indirect matrix converters [7-10] in which the bulky electrolytic dc-link capacitors is eliminated with the added advantage of increased life time of converter and reduction in system size. Further advancement in area of reduced semiconductor topology is B4 inverter [11] and five-leg inverter [12-20]. The B4 inverter reconfigures the third phase to the middle point of split dc link capacitor. Whereas five leg inverter is designed to run two three-phase motors independently with the fifth phase leg as common phase leg to which one phase from each motor connects. There are many application which require independent control of two or more ac loads such as four wheel drive of an electric vehicle, robotics etc. The basic solution to the problem is to use independent inverters to control each ac load. With this solution the cost and volume of the system is increased. Recently a new topology was designed called as Nine Switch Inverter (NSI) [21-28] to control two three phase ac loads independently. This topology saves three switches in comparison to conventional method used for controlling two ac loads independently In this

*Correspondence: goyalg@rknec.edu

paper, fifteen switch inverter to drive four three phase ac loads is proposed. Comparing fifteen switch inverter with conventional two level three phase inverter, it is possible to reduce switch count by nine switches. This easily fulfills the practical concern of cost/space reduction along with thermal management. In this paper the basic structure of fifteen switch inverter is proposed with its control strategy. This inverter is controlled using sinusoidal pulse width modulation (SPWM) and sinusoidal pulse width modulation, space vector pulse width modulation (SVPWM) technique. The control proposed for this inverter under common frequency operating mode is evaluated by simulation and verified through prototype.

2. Structure of the fifteen-switch inverter

2.1. Proposed topology

The topology of the proposed fifteen-switch inverter is shown in Figure 1. The fifteen switch inverter generates four sets of the standard three-phase two-level output with only one dc link voltage source. In this figure, the fifteen-switch inverter consists of four three-phase inverters named as Inv1, Inv2, Inv3, and Inv4 with nine common semiconductor switches. The Inv1 comprises switches SR1, SY1, SB1,SR2, SY2, SB2; Inv2 comprises switches SR2, SY2, SB2, SR3, SY3, SB3; Inv3 comprises switches SR3, SY3, SB3, SR4, SY4, SB4; and Inv4 comprises switches SR4, SY4, SB4, SR5, SY5, SB5.

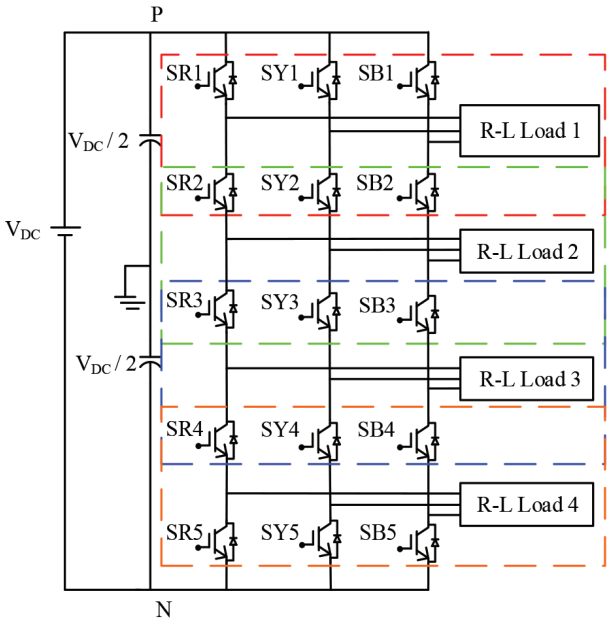

Figure 1. Main circuit of the proposed fifteen-switch inverter, where Inv1, Inv2, Inv3, and Inv4 are indicated by box with color red, green, blue, and orange respectively.

2.2. Carrier-based PWM method

The basic operation principle involved in generation of gating signal is that, the pulses generated should be able to turn ON only four semiconductor switches in a leg out of five at any instant of time. To satisfy this criterion a gating circuit to generate the pulses for fifteen-switch inverter is proposed as shown in Figure 2. There are four reference signals as indicated in (1)–(4) for each phase. The intermediate gate signal for Inv1, Inv2, Inv3, and Inv4 is generated by comparing Inv 1, Inv2, Inv3, and Inv4 reference signals of the related phase

(V_{xy}^{ref} $(x = R, Y \; or \; B \; \& \; y = 1, 2, 3 \; or 4)$) and the carrier signal. The final signal is generated by using a method as shown in Figure 2. By using this method four switches are ON at any instant of time in a particular leg. Let the voltage reference for Inv1, Inv2, Inv3, and Inv4 be $V_1{}^{ref}$, $V_2{}^{ref}$, $V_3{}^{ref}$, and $V_4{}^{ref}$ respectively and be represented by

$$V_1^{ref} = A_1 \sin(2\pi f_1 t + \varnothing_1) + offset_1, \tag{1}$$

$$V_2^{ref} = A_2 \sin(2\pi f_2 t + \varnothing_2) + offset_2, \tag{2}$$

$$V_3^{ref} = A_3 \sin(2\pi f_3 t + \varnothing_3) + offset_3, \tag{3}$$

$$V_4^{ref} = A_4 \sin(2\pi f_4 t + \varnothing_4) + offset_4, \tag{4}$$

where A_1, A_2, A_3, and A_4 are amplitudes, f_1, f_2, f_3, and f_4 are frequencies, and $\varnothing_1$, $\varnothing_2$, $\varnothing_3$, and $\varnothing_4$ are phases.

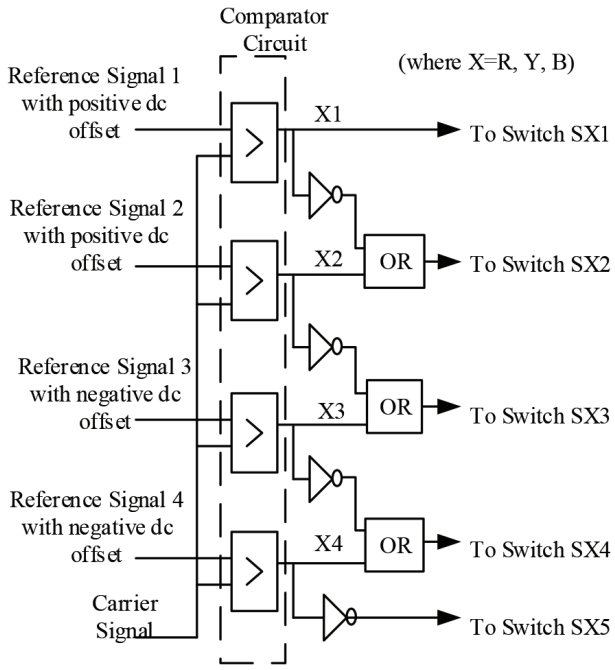

Figure 2. Method of generation gate signals.

The switching vectors of carrier-based PWM method are shown in Figure 3. Combining these switching vectors creates a specific sequence. This sequence is used to design the SVM method. One switching cycle consists of 24 vectors: two active vector for load 2 (VR2)—zero (VZ)—two active vector for load 1 (VR1)— zero (VZ)— two active vector for load 1 (VR1)—zero(VZ)— two active vector for load 2 (VR2)—zero (VZ) — two active vector for load 3 (VR3)—zero (VZ)—two active vector for load 4 (VR4)—zero (VZ)— two active vector for load 4 (VR4)—zero (VZ)— two active vector for load 3 (VR3)—zero (VZ).

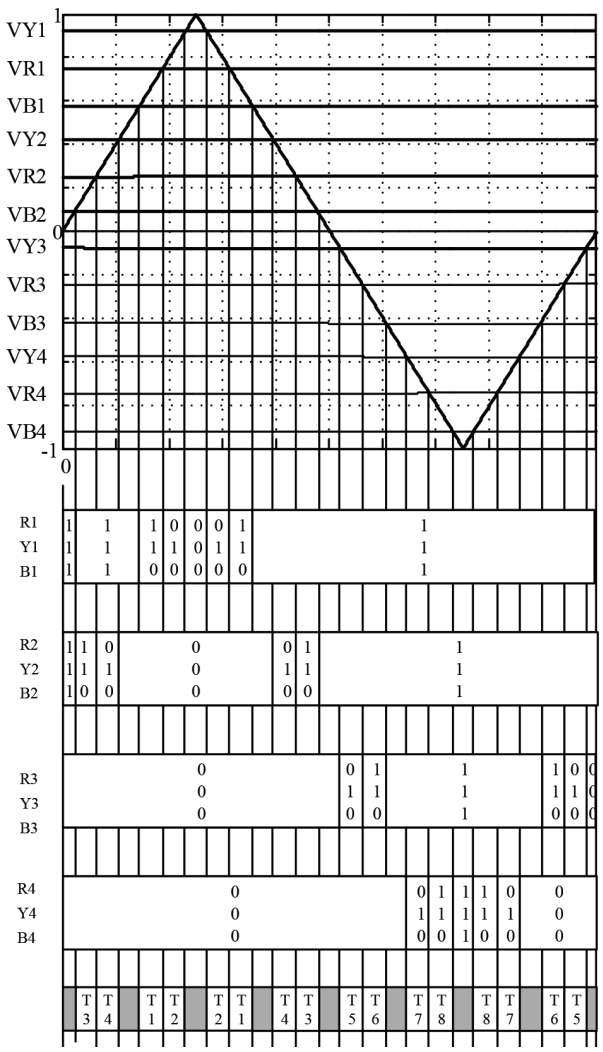

Figure 3. Carrier-based PWM method switching vector.

2.3. Space vector PWM method

Considering five switches in each leg of the FSI, the semiconductors of each leg can have thirty-two different ON–OFF positions. With the constraint that only four switches should be ON at any instant of time to avoid DC bus short circuit and also importantly floating of the connected loads, five states by each leg is permitted as indicated in Table 1.

Table 1. Semiconductor ON-OFF position of leg 1.

State	SR1	SR2	SR3	SR4	SR5	V_{R1N}	V_{R2N}	V_{R3N}	V_{R4N}
2	ON	ON	ON	ON	OFF	V_{DC}	V_{DC}	V_{DC}	V_{DC}
1	ON	ON	ON	OFF	ON	V_{DC}	V_{DC}	V_{DC}	0
0	ON	ON	OFF	ON	ON	V_{DC}	V_{DC}	0	0
–1	ON	OFF	ON	ON	ON	V_{DC}	0	0	0
–2	OFF	ON	ON	ON	ON	0	0	0	0

Therefore, having five possible states for each leg, there are 125 various switching mode configurations as shown in Figure 4.

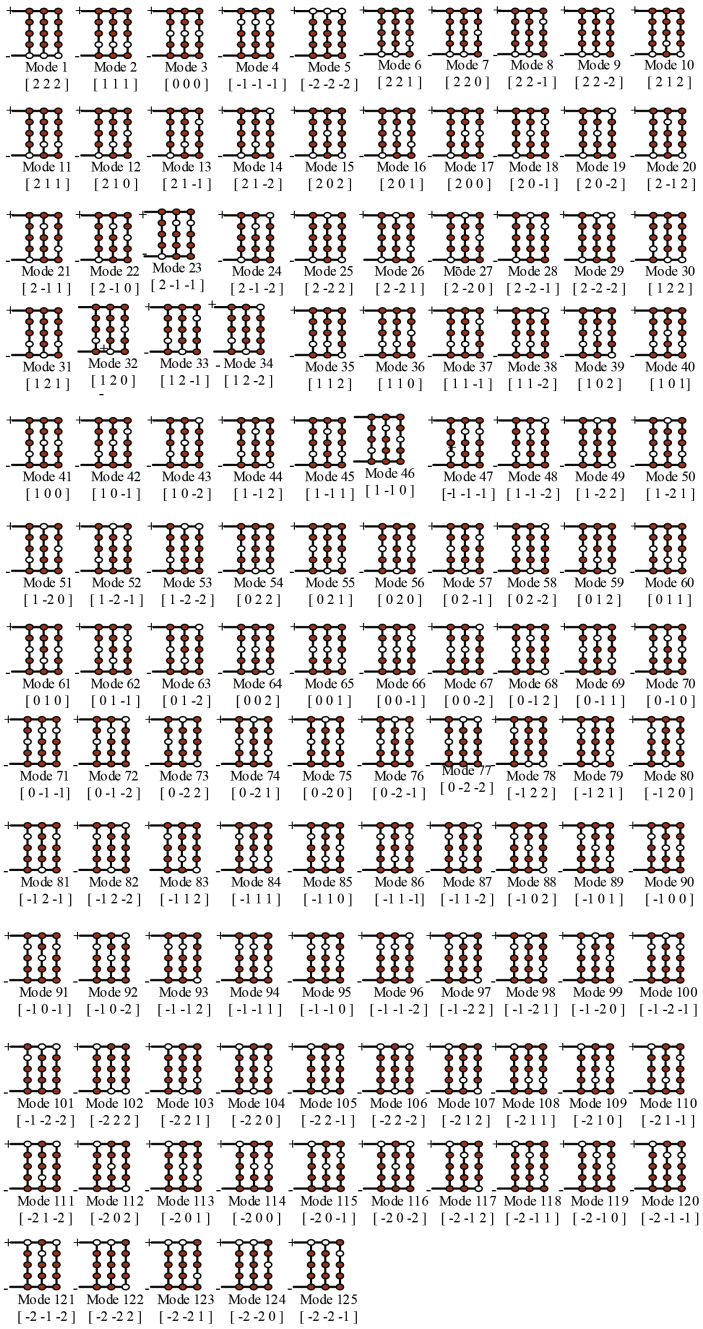

Figure 4. Arrangement of 125 switching modes of the fifteen-switch inverter.

Out of 125 switching modes; Mode 1, Mode 2, Mode 3, Mode 4, and Mode 5 are the zero modes (or vectors) wherein the line voltage is zero for all four inverters. The 125 vectors of FSI can be divided into eight groups' i.e.

(i) zero vector (05) (ii) only one active (24) (iii) upper two active (12)

(iv) lower two active (12) (v) middle two active (12) (vi) only three active (36)
(vii) all active: not identical (18) (viii) all active: identical (06)

All the possible variations of switching state {–2}, {–1}, {0}, {1}, and {2} are shown in Figure 4. However, a vector-including combination of {–2} and {–1} with {2} and {1} is undesirable because it disobeys the constraint that $V_1^{ref} > V_2^{ref} > V_3^{ref} > V_4^{ref}$.

For example, if it is desired to get 101 at the output of Inv1 and Inv2, it can be achieved through 9 different modes i.e. {0, –2, 0}, {1, –2, 0}, {2, –2, 0}, {0, –2, 1}, {0, –2, 2}, {1, –2, 1}, {2, –2, 1}, {1, –2, 2} and {2, –2, 2}. Only mode {0, –2, 0} follows the constraint and gives the desirable output of 101 at Inv1 and Inv2. With all the remaining modes the independency of loads is lost and they cannot have independent frequencies. Space presentation of the FSI switching modes is shown in Figure 5. With the above constraints only 53 vectors out of 125 vectors are desirable and expected to operate in FSI. The desired 53 vectors for independent control of load with fifteen-switch inverter are shown in Figure 6.

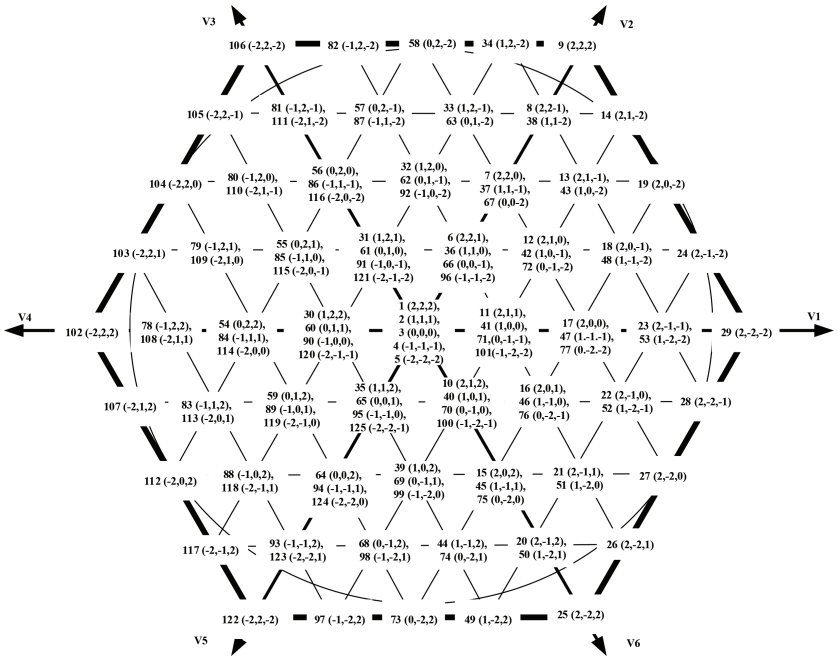

Figure 5. Switching vectors of FSI: space diagram presentation.

The reference signals for all four inverters are defined as

$$\bar{V}_1^{ref} = V_1^{ref} \angle \alpha_1, \tag{5}$$

$$\bar{V}_2^{ref} = V_2^{ref} \angle \alpha_2, \tag{6}$$

$$\bar{V}_3^{ref} = V_3^{ref} \angle \alpha_3, \tag{7}$$

$$\bar{V}_4^{ref} = V_4^{ref} \angle \alpha_4, \tag{8}$$

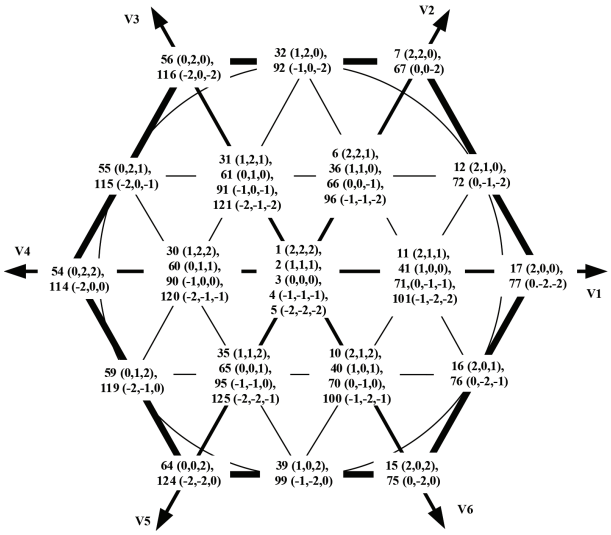

Figure 6. Desirable vectors of FSI for independent control of four loads.

where

$$\alpha_1 = 2\pi f_1 t + \varnothing_1, \tag{9}$$

$$\alpha_2 = 2\pi f_2 t + \varnothing_2, \tag{10}$$

$$\alpha_3 = 2\pi f_3 t + \varnothing_3, \tag{11}$$

$$\alpha_4 = 2\pi f_4 t + \varnothing_4, \tag{12}$$

where f_1, f_2, f_3 and f_4 are the frequencies, and $\varnothing_1$, $\varnothing_2$, $\varnothing_3$, and $\varnothing_4$ are the phases.

All five zero vectors can be used for placement of zero states based on minimum number of semiconductor switchings control goals and optimizations. The switching time intervals of vectors are calculated as

$$T_1 = \frac{\sqrt{3}}{2} m_1 T sin(\frac{\pi}{3} - \alpha_1), \tag{13}$$

$$T_2 = \frac{\sqrt{3}}{2} m_1 T sin(\alpha_1) \tag{14}$$

$$T_3 = \frac{\sqrt{3}}{2} m_2 T sin(\frac{\pi}{3} - \alpha_2), \tag{15}$$

$$T_4 = \frac{\sqrt{3}}{2} m_2 T sin(\alpha_2), \tag{16}$$

$$T_5 = \frac{\sqrt{3}}{2} m_3 T sin(\frac{\pi}{3} - \alpha_3), \tag{17}$$

$$T_6 = \frac{\sqrt{3}}{2} m_3 T sin(\alpha_3), \tag{18}$$

$$T_7 = \frac{\sqrt{3}}{2} m_4 T sin(\frac{\pi}{4} - \alpha_4), \tag{19}$$

$$T_8 = \frac{\sqrt{3}}{2} m_4 T sin(\alpha_4). \tag{20}$$

$$T_0 = T - T_1 - T_2 - T_3 - T_4 - T_5 - T_6 - T_7 T_8 \tag{21}$$

3. Inverter performance analysis and hardware implementation

To validate the topology of the fifteen-switch inverter operated by the proposed sinusoidal and space vector modulation technique the simulation is performed using MATLAB/Simulink and tested on a laboratory prototype. The load parameters of the simulation and the experiment are kept similar for an apparent comparison, as shown in Table 2. Similar R-L loads are connected to the outputs of all four inverters. The fifteen-switch inverter with input dc source of 50 V is simulated. To validate the proposed topology, the simulation of the fifteen-switch inverter is performed with different proposed modulation techniques. In this paper the fifteen-switch inverter is operated with a common reference frequency for each load. For performance analysis, fundamental RMS value and THD of output line voltage, phase voltage, and load current are analyzed.

Table 2. Inverter specification.

Parameters and operating modes	Values	
DC Link voltage source (V_{DC})	50	V
Switching frequency	2	kHz
Load resistance	5	Ω
Load inductance	2	mH
Fundamental frequency	50	Hz

To validate the topology of the fifteen-switch inverter a laboratory prototype is built. The four equal R-L loads are connected to the FSI with the same rating as used in simulation to compare the simulation and experimental results. The gating signal for fifteen semiconductor switches of the FSI is generated using programming Digital Signal Controller (DSC) dsPIC33EP512MU810. The pulses obtained from DSC are passed through buffer circuit, isolation circuit, and driver circuit before they are given to the gate of semiconductor switches. The MOSFET IRF 840 (8A, 500V) is used as switching device for the FSI. The DSC used is a 100 pin IC with 512 kb ram and speed of 70 MIPS. The schematic representation of hardware circuit is shown in Figure 7. An algorithm is prepared using output compare register of DSC to generate gating pulses with the constraint that only four switches should be ON at any instant of time.

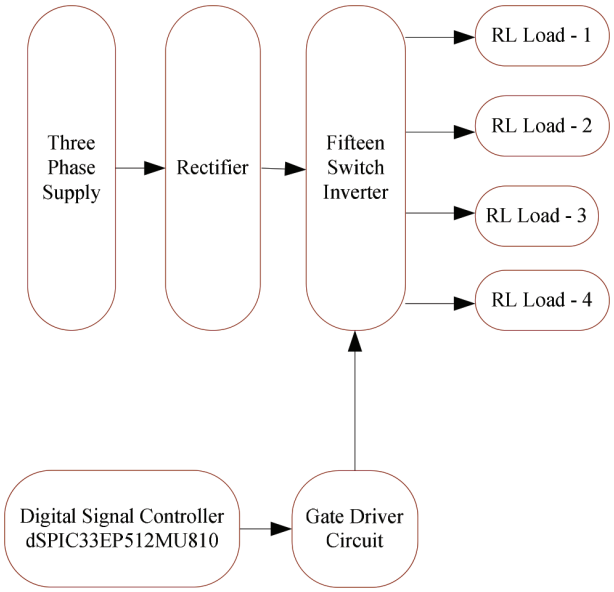

Figure 7. Block diagram representation of hardware circuit.

3.1. SPWM analysis of fifteen switch inverter

For analysis of FSI with SPWM modulation technique, the gating signal for fifteen switches is generated by the method as shown in Figure 2. The modulating references per phase are assigned the same frequency but ensuring $V_1^{ref} > V_2^{ref} > V_3^{ref} > V_4^{ref}$ with no crossover intersection.

A limited amount of phase shift can be introduced between the modulating reference waveform such that the total sum should not exceed the peak to peak vertical band of the carrier signal. Therefore, for a given phase shift; there is a limit on the maximum amplitude sum that can be divided among the two references and obviously the maximum sum of amplitude occurs when the waveform has zero phase shift. The modulation index sum for upper two references should be less than 1, i.e. $M_1 + M_2 \leq 1$ and similarly for lower references $M_3 + M_4 \leq 1$.

For example, if modulation index for reference-1 is 0.6 then modulation index for reference-2 can be maximum 0.4. Let the modulation index for Inv1 (=M1), Inv2 (=M2), Inv3 (=M3), and Inv4 (=M4) be the same and kept to the value of 0.4 for both simulation and hardware analysis. The simulated line voltages, phase voltages, and R phase current with their THD analysis of R phase are shown in Figure 8. With the same parameters as indicated in Table 2 the experimentation is performed with the SPWM modulation technique. The experimental line voltages, phase voltages, and R phase current with their THD analysis of R phase are shown in Figure 9. It can be clearly observed that output voltage has the desired frequency. The peak value of phase voltage of the two-level inverter is given by

$$V_{ph} = \frac{MV_{DC}}{2}. \tag{22}$$

The applied dc source voltage is 50 V and the modulation index in this case for all four inverters is 0.4. For these parameters the peak phase voltage calculated value is 10 V. It is observed from Figures 8 and 9 that the simulated and experimental value obtained for line voltage, phase voltage, and line current are satisfactory as compared to the calculated value. Similarly, the value of THD is also the same as the THD level of the

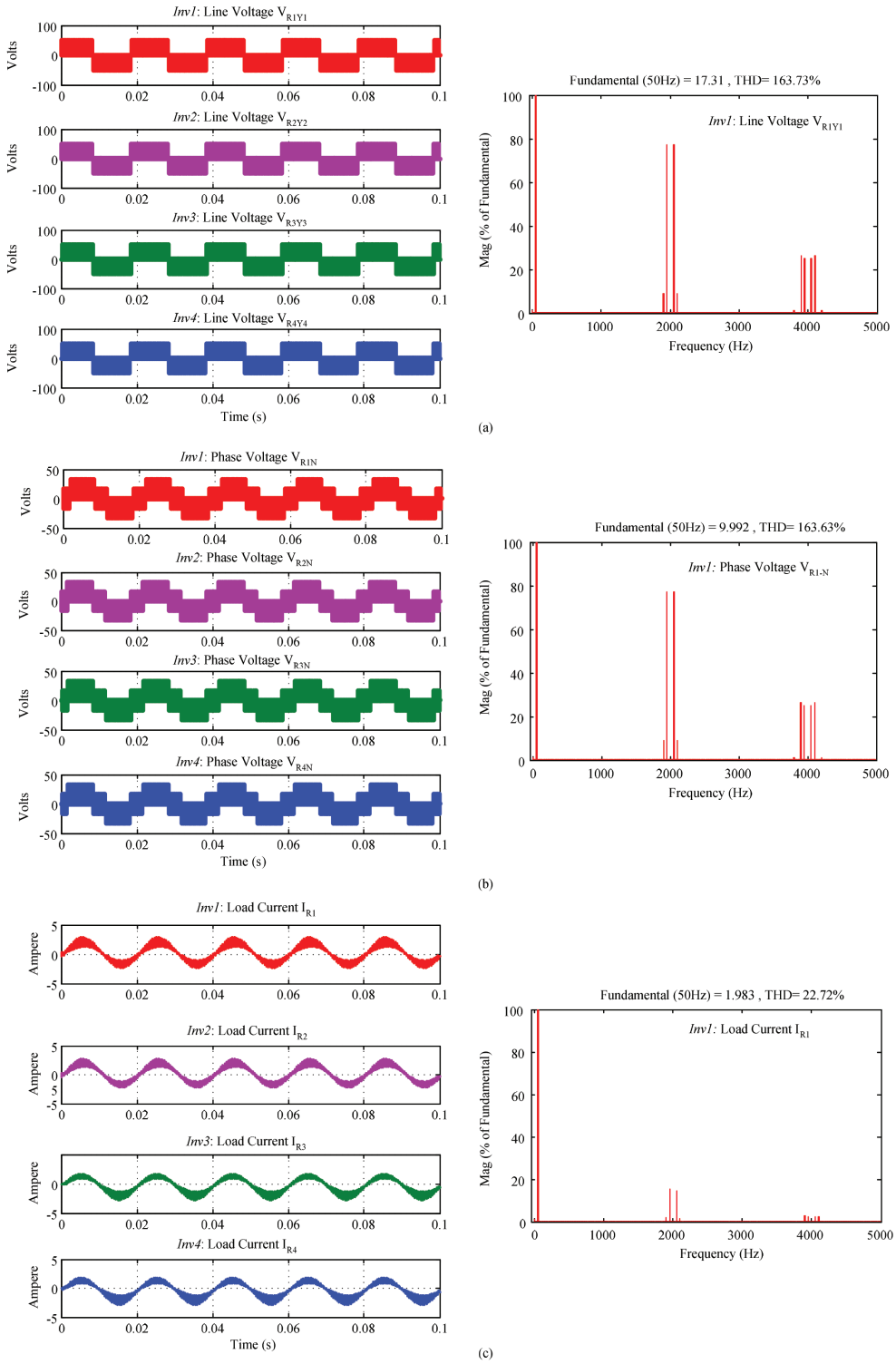

Figure 8. Simulated results of the fifteen-switch inverter with SPWM technique.

two-level inverter for modulation index of 0.4. Thus, this validates the fifteen-switch inverter topology with the SPWM modulation technique.

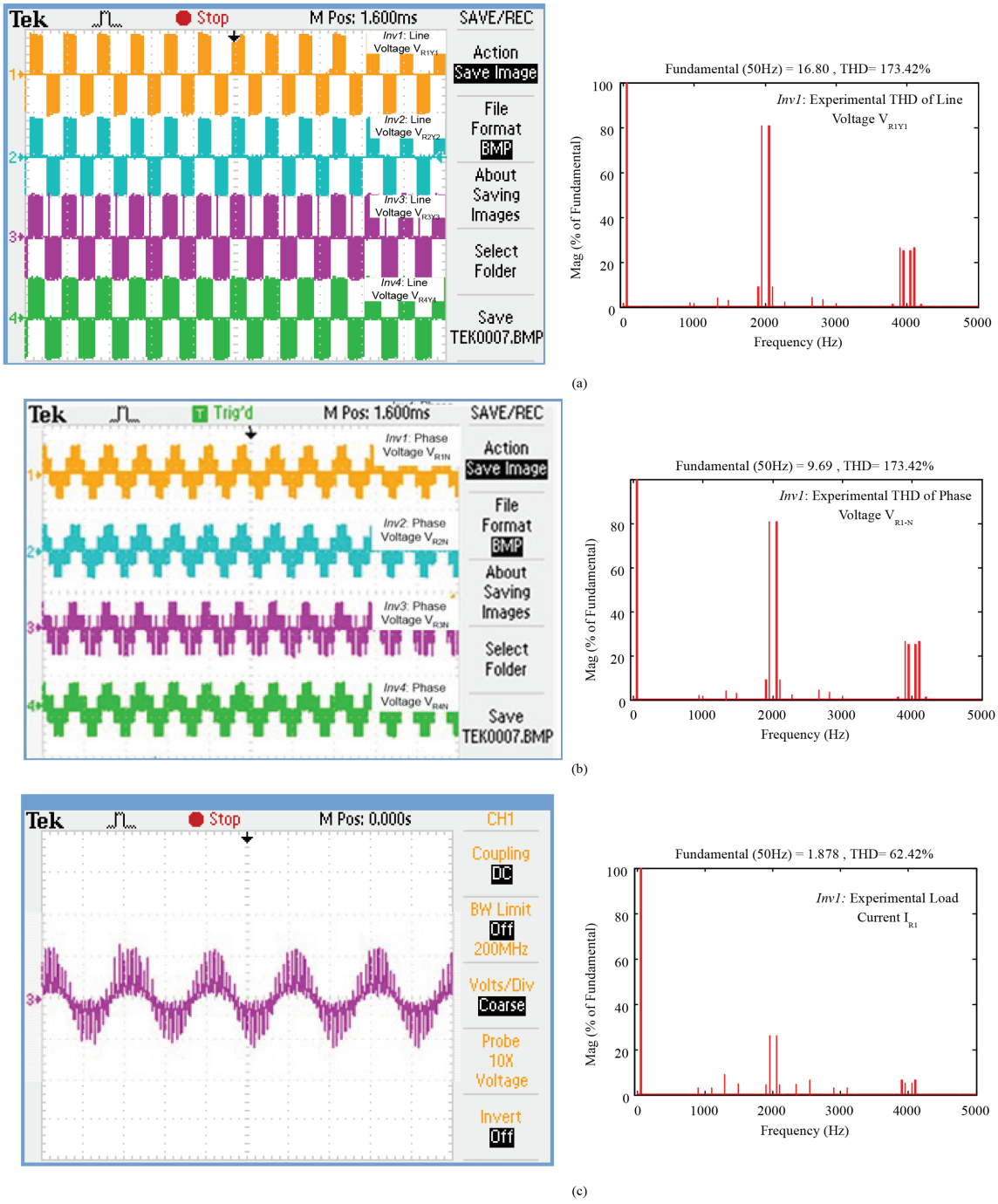

Figure 9. Experimental results of the fifteen-switch inverter with the SPWM technique (Scale Y axis (voltage):50 V/div, (current):5A/div and x axis: 10 ms/div).

3.2. SVPWM analysis of the fifteen-switch inverter

For better performance of fifteen switch inverter, space vector PWM modulation technique is employed. The switching vectors are as indicated in Figure 4. Space vector PWM modulation technique gives better fundamental output voltage and help in improving harmonic performance and reducing THD.

To validate the proposed space vector modulation as indicated in the previous section and to compare the experimental results with the simulation results, the analysis is done on hardware prototype of the FSI. The reference frequencies for all four inverters are the same and are set to 50 Hz. The modulation index is considered the same for Inv1, Inv2, Inv3, and Inv4 with the value of 0.4. The simulated line voltages, phase voltages, and R phase current with their THD analysis of R phase with the SVPWM technique are shown in Figure 10. With

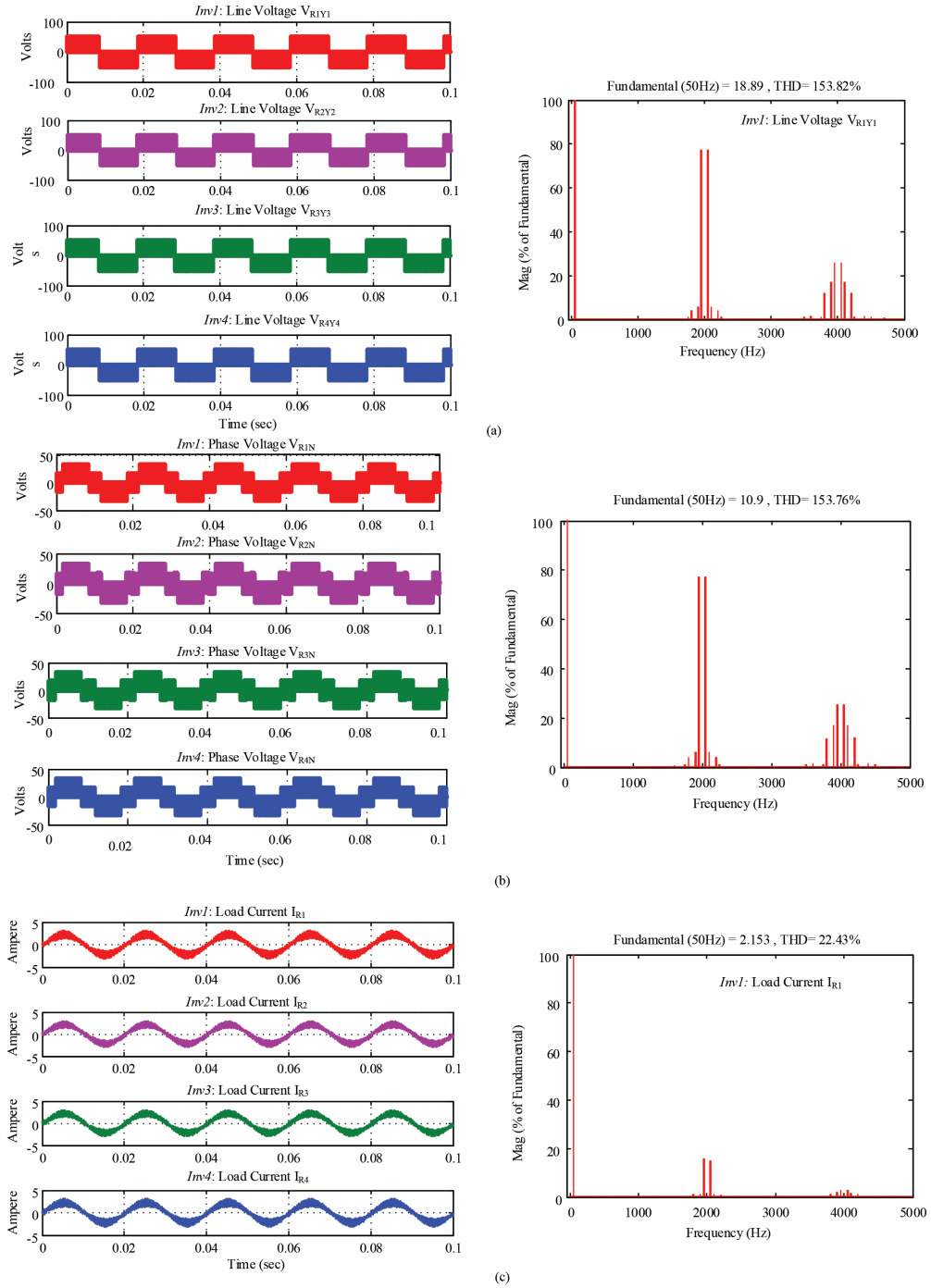

Figure 10. Simulation results of the fifteen-switch inverter with the SVPWM technique.

the same parameters as indicated in Table 2, the experimentation is performed with the SVPWM modulation technique. The experimental line voltages, phase voltages, and R phase current with their THD analysis of R phase are shown in Figure 11. With the applied dc source voltage of 50 V and the modulation index of 0.4, it is observed from Figures 10 and 11 that the simulated and experimental values obtained for line voltage, phase voltage, and line current are satisfactory compared to the calculated value.

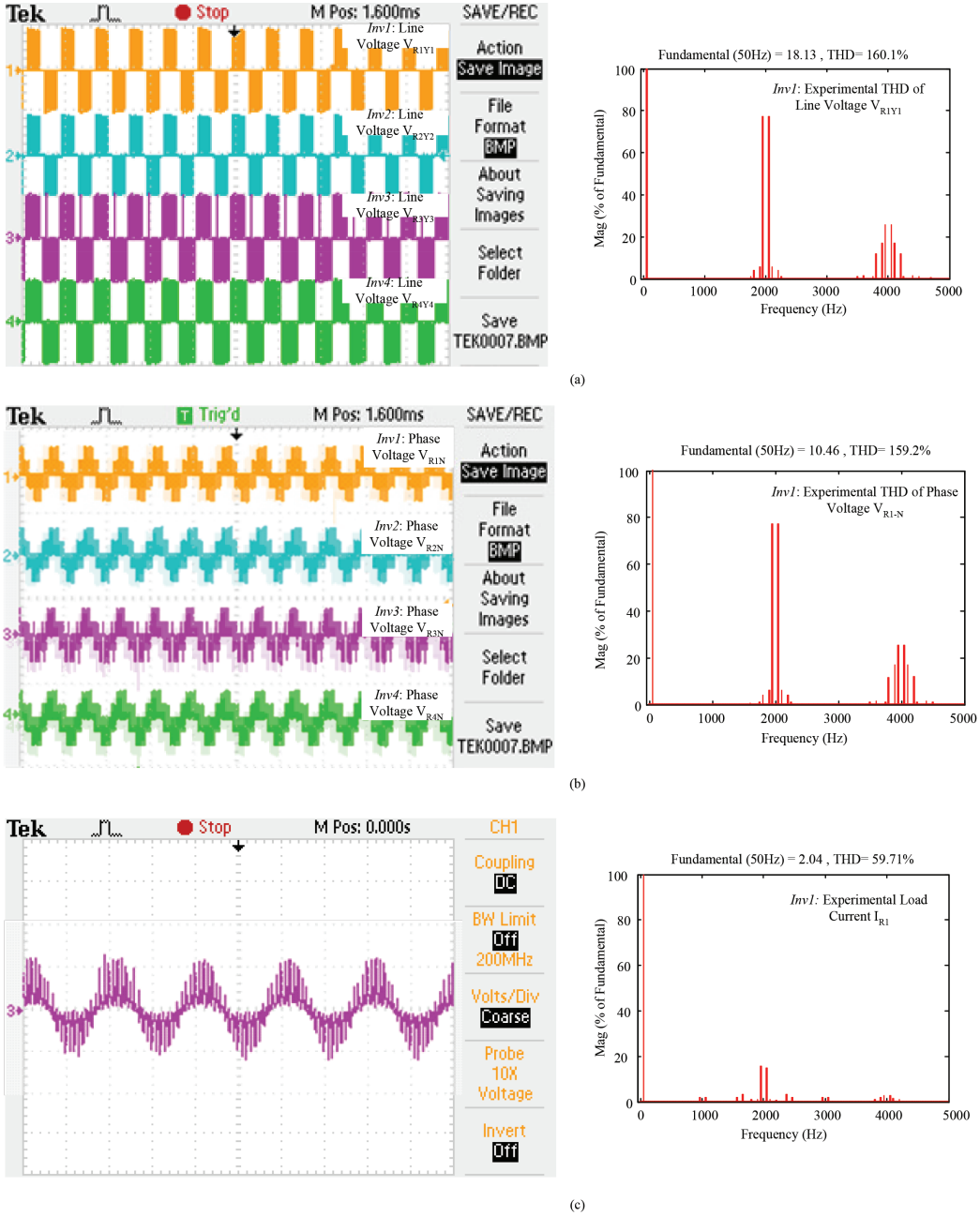

Figure 11. Experimental results of the fifteen-switch inverter with the SVPWM technique (Scale Y axis (voltage): 50 V/div, (current):5 A/div and x axis: 10 ms/div).

It is also observed that the fundamental RMS value is increased for the SVPWM technique compared to the SPWM modulation technique. Thus, this validates the fifteen-switch inverter topology with the SVPWM

modulation technique. The comparison of fundamental rms & THD values is shown in Table 3 for different modulation index with the SPWM & SVPWM techniques.

Table 3. Simulated and experimental values of fundamental rms and total harmonic distortion of line voltage & phase voltage at different modulation index for the SPWM & SVPWM techniques for load-1 R-phase (carriers frequency = 2 kHz, DC voltage = 50V).

MI	Line voltage								Phase voltage							
	SPWM				SVPWM				SPWM				SVPWM			
	Simulated		Experimented		Simulated		Experimented		Simulated		Experimented		Simulated		Experimented	
	RMS	THD	RMS	THD	RMS	THD	RMS	THD	RMS	THD	RMS	THD	RMS	THD	RMS	THD
0.1	3.07	370.4	2.89	402.2	3.33	359.2	3.20	364.1	1.77	370.4	1.67	402.2	1.92	359.1	1.85	363.2
0.2	6.13	252.0	5.83	272.1	6.69	241.9	6.40	248.1	3.54	252.0	3.37	272.1	3.86	242.1	3.69	247.8
0.3	9.18	197.1	8.91	212.2	10.10	187.2	9.70	194.3	5.30	197.1	5.14	212.2	5.83	187.3	5.60	194.2
0.4	12.2	163.4	11.88	173.4	13.36	153.8	12.82	160.1	7.07	163.4	6.85	173.4	7.71	153.7	7.40	159.2
0.5	15.3	145.4	15.01	156.4	16.84	135.2	16.17	141.2	8.84	145.4	8.67	156.3	9.72	135.5	9.34	140.8

4. Conclusion

In this paper, a new reduced switch topology of inverter which is capable of delivering three-phase power to four connected AC loads is proposed. The presented inverter is low-cost because the number of semiconductor switches is reduced compared to the traditional method of controlling four three-phase ac loads independently. In this paper, modified SPWM and SVPWM modulation techniques are proposed to control FSI. The inherent advantage of the SVPWM technique over the SPWM technique is that it increases the fundamental rms value by 15.5% and this can be clearly observed in Table 3. The FSI has a total of 125 switching vectors but to run four ac loads independently we require only 63 vectors. Thus, with the proposed control technique, the controlling of FSI becomes a bit simpler. As a proof of concept of the proposed inverter topology simulation analysis was presented. Finally, to validate the applicability of the proposed inverter in practical application, experimentation test using digital signal controller was conducted. The results are satisfactory as the inverter delivers the power to all four shared inverters at desired frequency and voltage. The application of the fifteen-switch inverter can be in industries like paper, textile etc. or in the area of robotics with multijoint robots and also in electric vehicles.

References

[1] Ebrahimi J, Babaei E, Gharehpetian GB. A new multilevel converter topology with reduced number of power electronic components. IEEE Transaction on Industrial Electronics 2012; 59(2): 655-667.

[2] Chu GML, Lu DDC, Agelidis VG. Flyback-based high step-up converter with reduced power processing stages. IET Power Electronics 2012; 5(3): 349-357.

[3] Itoh J, Noge Y, Adachi T. A novel five-level three-phase PWM rectifier with reduced switch count. IEEE Transaction on Power Electronics 2011; 26(8): 2221-2228.

[4] Santos dos EC, Jacobina CB, Almeida Carlos de GA, Freitas de IA. Component minimized AC–DC–AC single-phase to three-phase four-wire converters. IEEE Transaction on Industrial Electronics 2011; 58(10): 4624-4635.

[5] Lezana P, Rodriguez J, Oyarzun DA. Cascaded multilevel inverter with regeneration capability and reduced number of switches. IEEE Transaction on Industrial Electronics 2008; 55(3): 1059-1066.

[6] Figarado S, Bhattacharya T, Mondal G, Gopakumar K. Three-level inverter scheme with reduced power device count for an induction motor drive with common-mode voltage elimination. IET Power Electronics 2008; 1(1): 84-92.

[7] Young CM, Chen HL, Chen MH. A Cockcroft-Walton voltage multiplier fed by a three-phase-to-single phase matrix converter with PFC. IEEE Transaction on Industrial Application 2014; 50(3): 1994-2004.

[8] Vargas R, Ammann U, Rodriguez J. Predictive approach to increase efficiency and reduce switching losses on matrix converters. IEEE Transaction on Power Electronics 2009; 24(4): 894-902.

[9] Jussila M, Tuusa H. Comparison of simple control strategies of space-vector modulated indirect matrix converter under distorted supply voltage. IEEE Transaction on Power Electronics 2007; 22(1): 139-148.

[10] Idris SZ, Hamzah MK, Saidon MF. Implementation of single-phase matrix converter as a direct ac-ac converter with commutation strategies. Proceeding of 6th International Conference IEEE Power Electronics Drives System; Monterey, CA, USA; 2006. pp. 2240-2246.

[11] Masmoudi M, El Badsi B, Masmoudi A. DTC of B4-inverter-fed bldc motor drives with reduced torque ripple during sector-to-sector commutations. IEEE Transactions on Power Electronics 2014; 29(9): 4855-4865.

[12] Jacobina CB, Freitas ISD, Silva ERCD, Lima AMN, Riberio RLDA. Reduced switch count dc-link ac-ac five-leg converter. IEEE Transaction on Power Electronics 2006; 21(5): 1301-1310.

[13] Lim CS, Rahim NA, Hew WP, Levi E. Model predictive control of a two-motor drive with five-leg-inverter supply. IEEE Transaction on Industrial Electronics 2013; 60(1): 54-65.

[14] Jones M, Vukosavic SN, Dujic D, Levi E, Wright P. Five-leg inverter PWM technique for reduced switch count two-motor constant power applications. IET Electric Power Application 2008; 2(5): 275-287.

[15] Oka K, Nozawa Y, Matsuse K. Improved method of voltage utility factor for PWM control method of five-leg inverter. Proceeding of 37th IEEE Power Electronics Specialists Conference; Jeju, South Korea; 2006. pp. 1-5.

[16] Hizume M, Yokomizo S, Matsuse K. Independent vector control of parallel connected two induction motors by a five-leg inverter. Proceeding of European Conference on Power Electronics Application; 2003; pp. 1-7.

[17] Delarue P, Bouscayrol A, Semail E. Generic control method of multi-leg voltage-source-converters for fast practical implementation. IEEE Transaction on Power Electronics 2003; 18(2): 517-526.

[18] Jones M, Dujic D, Levi E. A performance comparison of PWM techniques for five-leg VSIs supplying two-motor drives. Proceeding of 34th Annual Conference of IEEE Industrial Electronics IECON; Orlando, FL, USA; 2008; pp.508-513.

[19] Jones M, Vukosavic SN, Dujic D, Levi E, Wright P. Five-leg inverter PWM technique for reduced switch count two-motor constant power applications. IET Electric Power Applications 2008; 2(5): 275-287.

[20] Lim CS, Rahim N, Hew WP, Levi E. Model predictive control of a two-motor drive with five-leg-inverter supply. IEEE Transaction on Industrial Electronics 2013; 60(1): 54–65.

[21] Liu C, Wu B, Zargari NR, Xu D, Wang J. A novel three-phase three-leg ac-ac converter using nine IGBTs. IEEE Transaction on Power Electronics 2009; 24(5): 1151-1160.

[22] Consoli A, Cacciato M, Gennaro F, Scarcella G, Testa A. Common mode current elimination in multi-drive industrial systems. Conference Record of the IEEE Industry Applications Conference; Phoenix, AZ, USA; 1999; pp. 1851-1857.

[23] Kshirsagar A, Kaarthik RS, Umanand L, Gopakumar K, Rajashekara K. Nine level inverter for open end induction motor with eight switches per phase. Proceeding of 41st Annual Conference of IEEE Industrial. Electronics Society; Yokohama, Japan; 2015; pp. 001097-001102.

[24] Edpuganti A, Rathore A. Fundamental switching frequency optimal pulsewidth modulation of medium-voltage nine-level inverter. IEEE Transaction on Industrial Electronics 2015; 62(7): pp. 4096-4104.

[25] Dehnavi SM, Mohamadian M, Yazdian A, Ashrafzadeh F. Space vectors modulation for nine-switch converters, IEEE Transaction on Power Electronics 2010; 25(6): 1488–1496.

[26] Dehghan SM, Amiri A, Mohamadian M, Andersom MAE. Modular space-vector pulse-width modulation for nine-switch converters. IET Power Electronics 2013; 6(3): 457–467.

[27] Tseng SK, Tseng CC, Liu TH, Chen JL. Wide-range adjustable speed control method for dual-motor drive systems. IET Electronics Power Application 2015; 9(2): 107–116.

[28] Goyal GN, Aware MV. A comparative performance of six-phase nine-switch inverter operation with SPWM and SVPWM. IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES); Bengaluru, India; 2012; pp. 1-6.