Design of a spurious-free RF frequency synthesizer for fast-settling receivers

Hilmi Kayhan YILMAZ[1,*] , **Serkan TOPALOGLU**[2]

[1]Department of Avionics Technologies, Advanced Technologies Directorate, Roketsan Missiles Inc., Ankara, Turkey
[2]Department of Electrical and Electronics Engineering, Faculty of Engineering, Yeditepe University,
İstanbul, Turkey

Abstract: A tunable reference clock frequency topology is presented as a spur reduction application for frequency synthesizers of fast frequency hopping spread spectrum systems. The method was verified by measurements on a designed hardware operating at L-band frequencies. This spur reduction method is based on optimizing the reference clock frequency of synthesizers to mitigate spurs. By using the spur reduction method, the power of spurious signals was reduced up to 57 dB. The performance of the spur reduction method was also analyzed at different loop-filter configurations. Smaller lock time was obtained by enlarging the bandwidth of the loop filter up to 150 kHz. The required power response of the spurious signals specified in telecommunication standards was achieved even though the loop filter bandwidth was enlarged.

Key words: Fast-frequency hopping spread spectrum, spurious-free, integer-boundary spur, synthesizer, fractional phase-lock loop, L-band, receiver, transmitter, RF phase-lock loop, spur mitigation

1. Introduction

A frequency synthesizer is a critical section of an intermediate frequency (IF)-based receiver design in terms of both local oscillator signal generation and the analog-to-digital conversion section. The receiver performance is directly affected by clock phase noise and accuracy properties because the reduction in signal-to-noise ratio and the effective number of bits in the analog-digital converter (ADC) section is caused by poor phase noise and signal frequency accuracy properties. On the other hand, local oscillator (LO) signal quality is critical in the RF downconversion section due to the spectrum efficiency. An adjacent channel or an interference can exist in the same span, which is very close to the desired signal and has a higher power response than the desired signal. Furthermore, both desired signals and other signals are downconverted by mixing with an LO signal. Reciprocal mixing is caused by these impairments of the LO signal. A reciprocal mixing example is shown in Figure 1.

Phase-locked loop (PLL)-based clock distribution devices and RF synthesizers can be a solution for both ADC clock and LO signal issues. In addition, high-efficiency spectrum applications can be achieved by smaller tuning step size properties of fractional type PLLs. However, the spurious response is caused by the PLL operation itself. Likewise, improper downconversion is caused by spurious products. The power response of spurious products of the signals is defined by communication standards, which are specific for applications. The spurious response of the PLL is caused by reference clock properties and fractional type PLL operation. This paper presents a fractional spur mitigation by taking lock time into consideration [1].

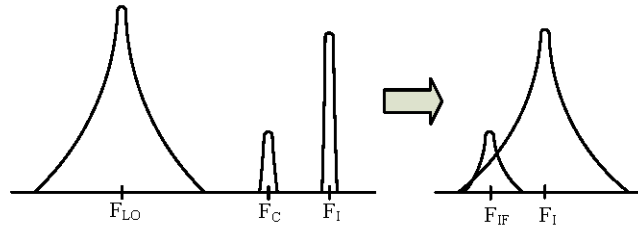*Correspondence: kayhan.yilmaz@roketsan.com.tr

Figure 1. Reciprocal mixing.

2. PLL architectures

Analog PLLs are commonly used for generating high-frequency signals, which are used as local oscillator signals for both downconverters and upconverters with a constant phase response and high accuracy.

2.1. Integer PLL architecture

Basic PLL topology contains a comparator, loop filter, VCO, and frequency dividers. The comparator is fed by a reference clock signal and the clock signal is obtained by dividing the VCO frequency by a feedback divider. These clock sources are compared in the comparator and a clock frequency error is obtained. To decrease the amount of the error level, a charge pump current is generated and the VCO tuning port is fed by the generated charge pump current. With the decreasing error, VCO is set to the desired frequency with a more constant phase. When these clock sources are in the same phase and frequency, lock condition is ensured. The integer PLL structure is given in Figure 2.
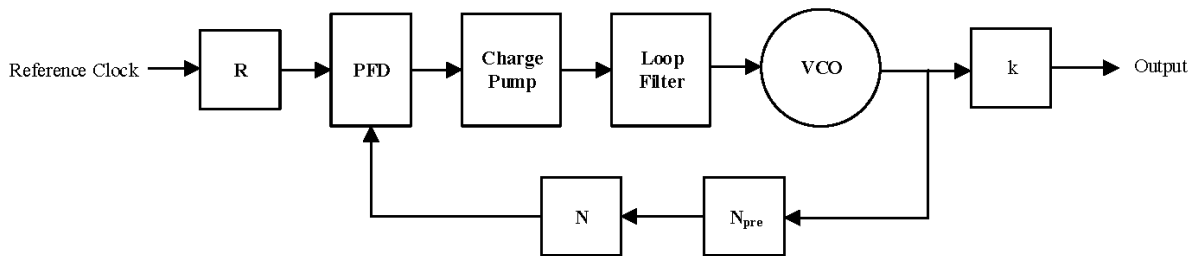

Figure 2. Block diagram of integer PLL.

The reference clock divider and VCO prescalar can be involved in the PLL structure. Through these dividers, smaller phase-frequency detector (PFD) frequencies can be obtained. In other words, the VCO tuning resolution is increased by decreasing the PFD frequency. On the other hand, tuning step sizes are limited by the smallest PFD frequency, which is supported by the PLL device. Moreover, the phase noise reduction problem is generated by the smaller PFD frequency. Output frequency of the PLL structure can be expressed as in (1),

where f_{output} is output frequency, f_{VCO} is VCO frequency, and k is output divider [1, 2].

$$f_{output} = \frac{f_{VCO}}{k} \tag{1}$$

The output VCO frequency is directly related to the divider ratios and reference frequency. Output VCO frequency can be expressed as in (2), where f_{Ref} is reference frequency, R is reference divider, N is feedback divider, and N_{pre} is predivider.

$$f_{VCO} = N \cdot N_{pre} \cdot \frac{f_{Ref}}{R} \tag{2}$$

2.2. Fractional PLL architecture

Very small step tuning sizes can be also achieved by fractional PLLs. The architecture of the fractional PLLs is similar to the integer PLLs. The modulator is the only major difference between fractional and integer type PLLs. PFD frequencies can be higher than the integer PLLs in order to get the same tuning step size. Step sizes lower than the PFD frequencies can be achieved by modulator operation. In that case, the feedback divider ratio includes the fractional part to obtain a smaller step size. The output frequency calculation of a fractional PLL topology can be expressed as in (3) and (4), where f_{int} is the integer part of VCO frequency, f_{frac} is the fractional part of VCO frequency, N_{int} is the integer division ratio, and N_{frac} is the fractional division ratio.

$$f_{VCO} = f_{int} + f_{frac} \tag{3}$$

$$f_{VCO} = f_{PFD} \cdot (N_{int} + N_{frac}) \tag{4}$$

The feedback divider ratio is changed between N and N+1 by the modulator to attain the fractional part of the frequency. When the modulator's full cycle is completed, the fractional part is obtained on an average of the feedback divider ratio. The feedback divider ratio of a fractional PLL can be expressed as in (5) and (6), where C is the total cycle number of the modulator and C_{frac} is the number of fractional cycles.

$$N = \frac{(C - C_{frac}) \cdot N_{int} + C_{frac} \cdot (N_{int} + 1)}{C} \tag{5}$$

$$C_{frac} = f_{PFD} \cdot N_{frac} \tag{6}$$

The tuning step sizes are defined by the modulator cycle number. Therefore, Hz grade tuning step sizes are achieved by the fractional PLL topology. Besides, small PFD frequencies and higher feedback divider ratios are not necessary. Thus, the phase noise reduction problem is eliminated due to higher PFD frequencies in fractional PLL topology. The theoretical noise reduction by using fractional PLL is expressed as in (7).

$$PhaseNoiseReduction = 20 \cdot \log(\frac{PFD_{Fractional}}{PFD_{Integer}}) \tag{7}$$

On the other hand, the spurious response, which is called fractional or N-boundary spurs, is created by modulator operation. The fractional spur location can be specified by the PFD frequency and feedback divider ratio. Offset between VCO output frequency and the spurious product can be expressed as in (8).

$$f_{VCO} - f_{spur} = \begin{cases} (N - \lfloor N \rfloor) \cdot f_{PFD}, & \text{if } N - \lfloor N \rfloor < 0.5 \\ (N - \lceil N \rceil) \cdot f_{PFD}, & \text{if } N - \lfloor N \rfloor \geq 0.5 \end{cases} \tag{8}$$

Spurious products should be filtered away by a well-characterized loop filter. However, spurious products may be located in the pass-band region of the loop filter due to smaller step sizes and cannot be filtered. Besides, poor lock times are caused by narrow loop filters. [1, 2]

3. Spurious-free synthesizer design

It is shown that the spur location is directly related to the PFD frequency as in (8). The feedback divider ratio is specified by PFD frequency at a specified output frequency as well as the fractional part of the feedback divider. Changing the PFD frequency is a solution for moving spurious signals out of the loop-filter pass-band region. Besides, loop filter configuration is an issue for lock time instead of spurious response in that case.

Various PFD frequencies are required for proper spur reduction in this method. The required PFD frequencies can be obtained by the changing reference clock divider or changing the reference clock frequency. The specific PFD frequencies cannot be obtained by changing the reference divider ratio. Therefore, changing the reference clock frequency is the solution for applying this method.

PFD frequency can be changed by a reference clock divider, which is located in the RF PLL. The degradation in phase noise is caused by decreasing the PFD frequency. For proper operation, intermediate PFD values are required, and these values are obtained from tunable reference sources. Based on the operation, several different reference clocks are required to obtain a proper spurious reduction, especially for very small step sizes. [3–5]

3.1. Proposed application of spurious-free synthesizer design

In the application of the method [6], the RF PLL should be driven by a PLL-based clock source to obtain the required reference clock frequencies for the RF PLL. In a receiver system, the low jitter clock signals are required by ADCs as well. Therefore, the application of the method [6] was configured as a frequency synthesizer hardware for which clock signals to high-speed ADCs are provided by an integer PLL-based clock generator and spurious-free local oscillator signals to the RF section are provided by the fractional PLL-based RF synthesizer.

Besides the fractional spurious phenomenon, integers spur are the other spurious phenomenon, generally referred to as "reference sidebands" or "spurs". The desired frequency is generated as an integer multiple of the PFD frequency by the integer PLL device. The performance degradation in the ADC is also caused by integer spurs. Likewise, if the RF PLL is driven by a reference clock that has a spurious response, the spurious products exist at the RF VCO output. Thus, jitter cleaner or reference side-band signal cleaner PLL and a VCO structure as a clock source were used for eliminating integer reference spurious products. Therefore, AD9524 from Analog Devices is selected as an integer PLL-based clock distribution device and two PLL structure are included to provide a jitter-less clock to the RF synthesizer, ADC/DAC, and other systems [7].

The external tunable stable oscillator (VC-TCXO), which operates at 40 MHz, is required and is driven by the first PLL of the AD9524. The internal high-frequency VCO of AD9524, which has a tuning range of 3600–4000 MHz, is driven by the second PLL of the AD9524. The block diagram of the AD9524 is given in Figure 3 [7].

On the other hand, the clock distribution PLL was programmed once after the power-up. Only the output dividers were changed to obtain the desired reference clock frequencies and the PLL of the AD9524 preserves its lock condition during this process. Therefore, the elapsed time for this operation was the register update time. The extra time was not added to RF PLL's lock time [7].
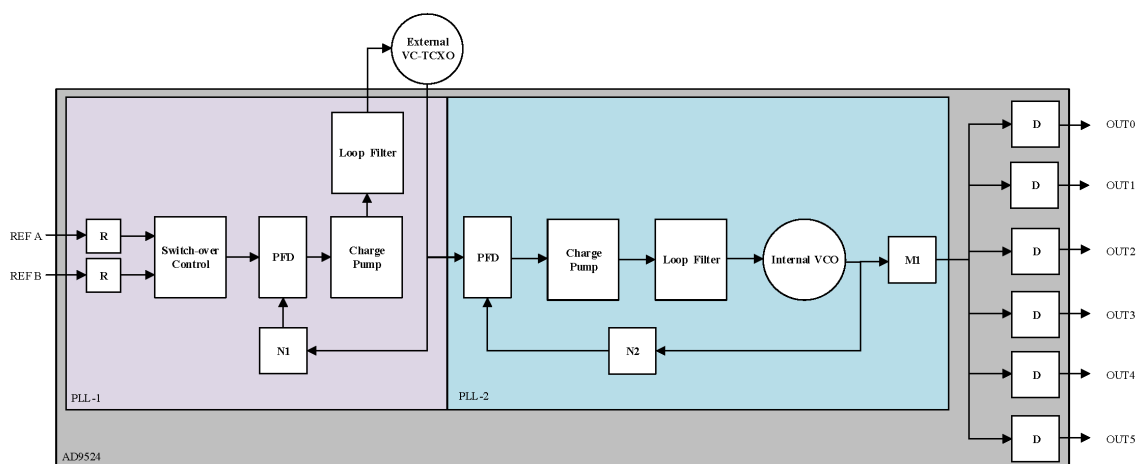
Figure 3. Block diagram of integer PLL-based clock generator (AD9524).

In this application, the second PLL of the AD9524 was programmed to lock at 3720 MHz VCO frequency. The output ports of the clock distribution device (AD9524) are also individually programmable. Two frequency dividers exist in the clock distribution device (AD9524), which is in a cascaded operation to obtain the desired output frequency. The spur reduction method was analyzed and measured at around 50 MHz reference clock frequency in the proposed application. The required divider ratios at the output of the clock distribution PLL to obtain the desired clock frequencies are given in Table 1.

Table 1. Required reference clock frequencies for spur reduction.

Output frequency of AD9524 (MHz)	M1 (common divider of AD9524)	D(Channel divider of AD9524)	Total division ratio (M1xD)
58.125	4	16	64
57.23	5	13	65
53.14	5	14	70
51.666	4	18	72

RF PLL timing and phase noise performances were also observed using simulation tools. HMC830 was used as a fractional type RF PLL, which is a product of Analog Devices. The HMC830 includes an internal VCO that operates between 1500 MHz and 3000 MHz. On the other hand, the output frequency of the HMC830 can be obtained between 25 MHz and 3000 MHz by output frequency dividers. The block diagram of the HMC830 is given in Figure 4. In this application, the spurious response of the RF PLL was analyzed between 880 MHz to 1380 MHz since it is designed for an L-band receiver system [8].

The required configuration to obtain a proper phase noise response was specified by simulations. In addition, the lock time was observed in simulations. The frequency changing speed was defined by the lock time of the PLL. The lock time at HMC830 output, whose frequency was 2GHz, was approximately 150 microseconds with 1 Hz error when the loop bandwidth (LBW) of the loop filter was 45 kHz. The PLL time simulation results at these specific conditions are given in Figure 5 [3, 8, 9].
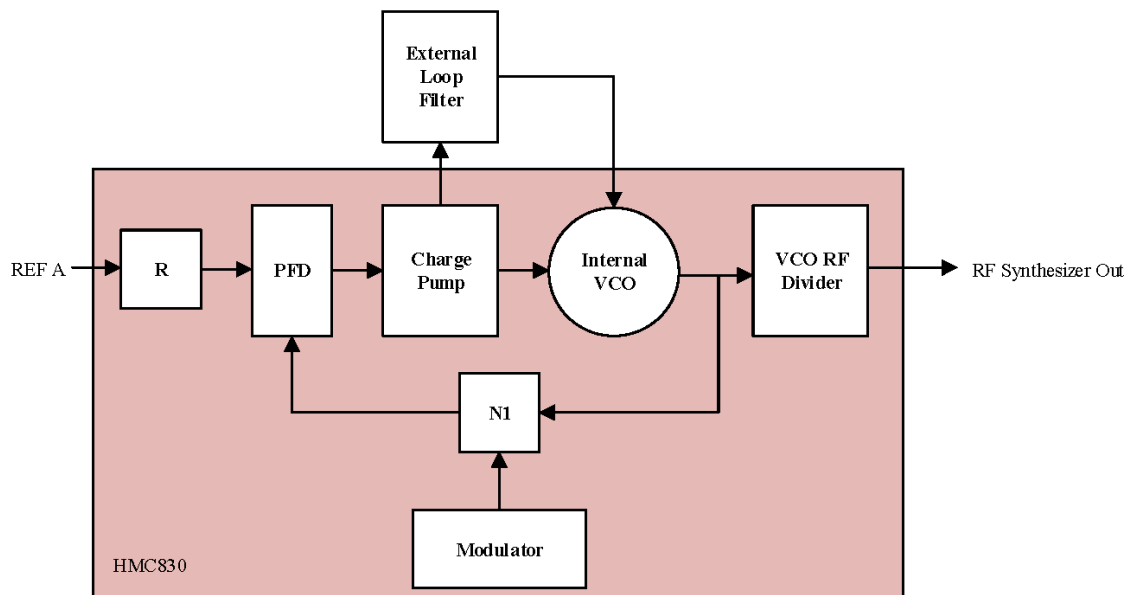
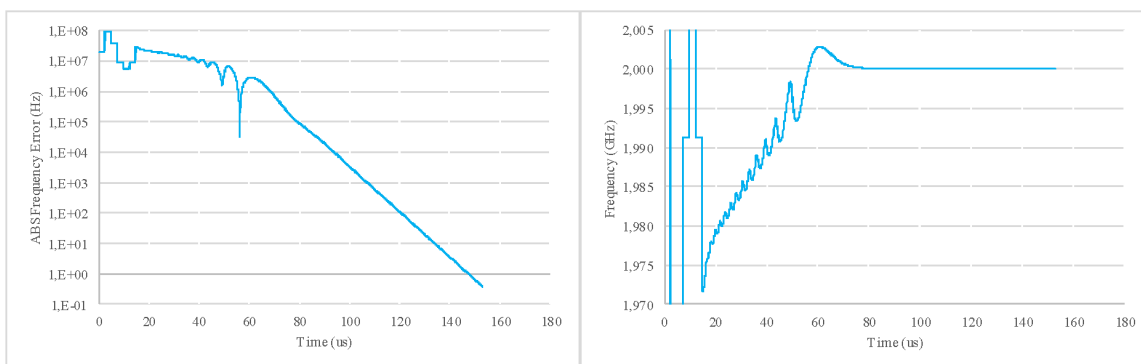**Figure 4**. Block diagram of fractional PLL-based RF synthesizer (HMC830).

Figure 5. Lock time when loop filter bandwidth is 45 kHz.

The block diagram of the proposed hardware is given in Figure 6. The AD9524 and HMC830 were placed in cascaded operation to apply the spur reduction method. One output channel of AD9524 was used as a tunable clock source for HMC830. In addition, two output channels, marked as AUX-1 and AUX-2 in Figure 6, can be used as stable and jitter-less clock sources for ADC and DAC. The reference clocks are required by the other hardware in the systems to obtain synchronization between systems. Thus, the other auxiliary ports of the AD9524 can be used as a clock reference for other systems. Therefore, the proposed hardware was designed as a frequency synthesizer for both other digital and RF hardware.

Spur reduction by applying the tunable reference frequency method was examined with the ADISim Frequency Planner simulation tool. The predefined parameters, which were loop filter bandwidth and reference
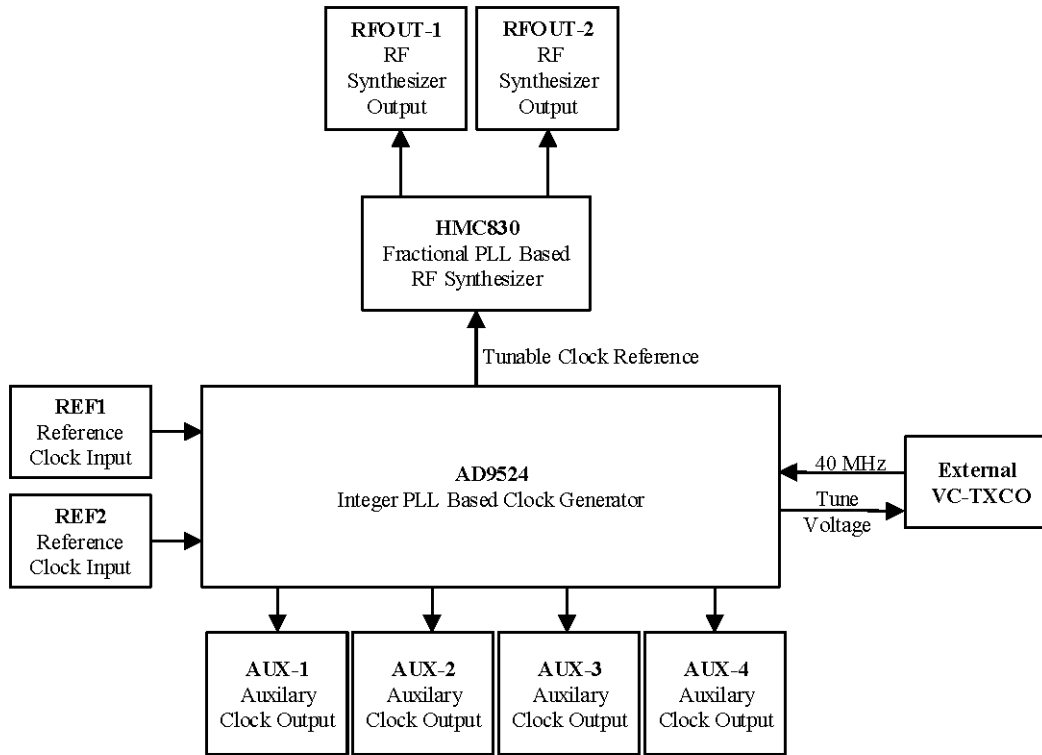
Figure 6. Block diagram of the proposed hardware.

clock frequencies, are given in Table 1. The spur reduction simulation was conducted between 880 MHz to 1380 MHz with a 100 kHz frequency step size. The simulation result is given in Figure 7.
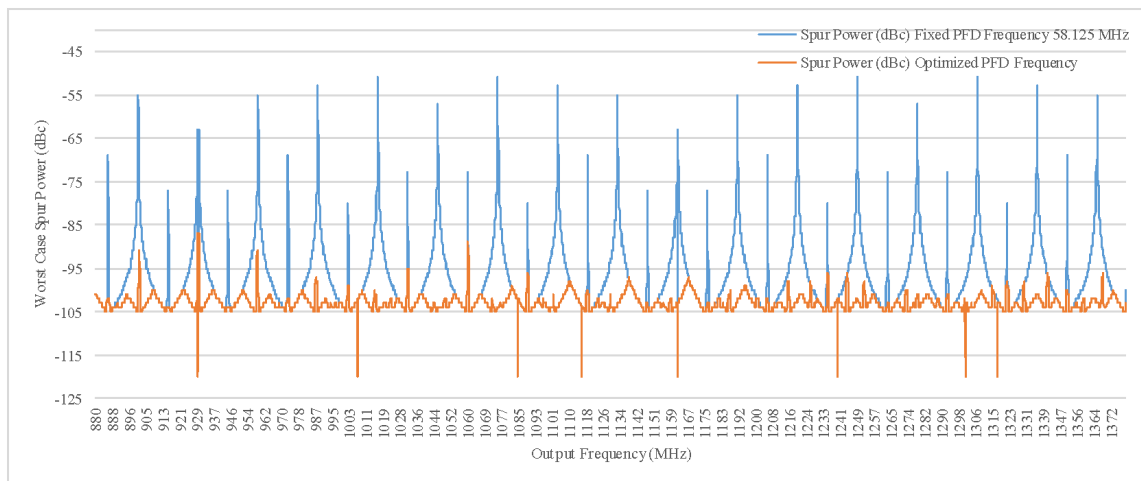

Figure 7. Spur reduction simulation when loop filter bandwidth is 45 kHz.

The best spur reduction occurs at 1017.2 MHz. The spur value was –50.3 dBc when the input reference was 58.125 MHz, while the spurious power response was –98.3 dBc when the reference value was 57.231 MHz. For 58.125 MHz as the reference input, the n-boundary spur occurred 12.5 kHz away from 1017.2 MHz, so it was not filtered out. However, when 57.231 MHz was applied as the reference, the spur occurred 12.95 MHz away from 1017.2 MHz. Moreover, this spur was filtered out by the loop filter. As a result, spur reduction was achieved. On the other hand, spurious response suppression is related to the loop filter bandwidth. Smaller power response of spurious product is obtained by using narrower loop bandwidth. However, the narrower bandwidth causes poor lock time. There is a trade-off between the spurious response and the lock time. The relation between the lock time and the LBW is expressed as in (9), where LBW is loop-filter bandwidth.

$$LockTime \sim= \frac{4}{LBW} \tag{9}$$

The spurious reduction performance and the lock time were also observed for 150 kHz loop bandwidth. According to simulations, lock time was approximately 50 microseconds when the loop filter bandwidth was configured as 150 kHz. The simulation result is given in Figure 8.
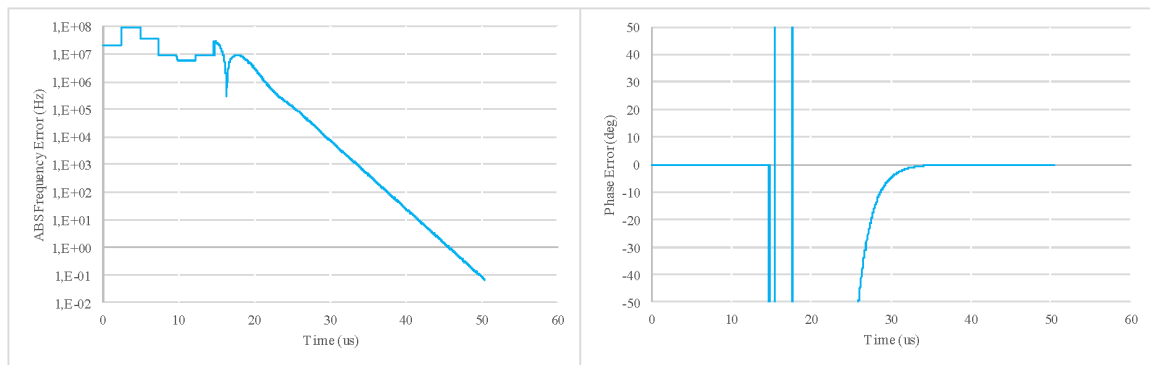

Figure 8. Lock time when loop filter bandwidth is 150 kHz.

In these circumstances, the spurious reduction was analyzed. The result of the spur reduction simulation is given in Figure 9. The worst spurious response occurred at 928 MHz and its power response was about –77 dBc. The spurious product at 928 Mhz was reduced by about 20 dB, which is the same as in previous conditions by a proposed design when it was compared with a fixed reference clock frequency. Enlarging the loop bandwidth resulted in 10 dB of degradation on the worst spurious signal power while the lock time was reduced by three times. However, the spur reduction method still presents the same reduction values and superior spurious response.

4. Prototypes and measurements

The postproduction image of the proposed design is shown in Figure 10. The phase noise and lock time measurements were conducted at the same frequency as the simulation frequency, 2000 MHz, in order to validate the simulation results.

The comparison between simulation and measurements in terms of phase noise is given in Table 2. Moreover, Table 2 includes a comparison between telecommunication standards. Furthermore, the proposed
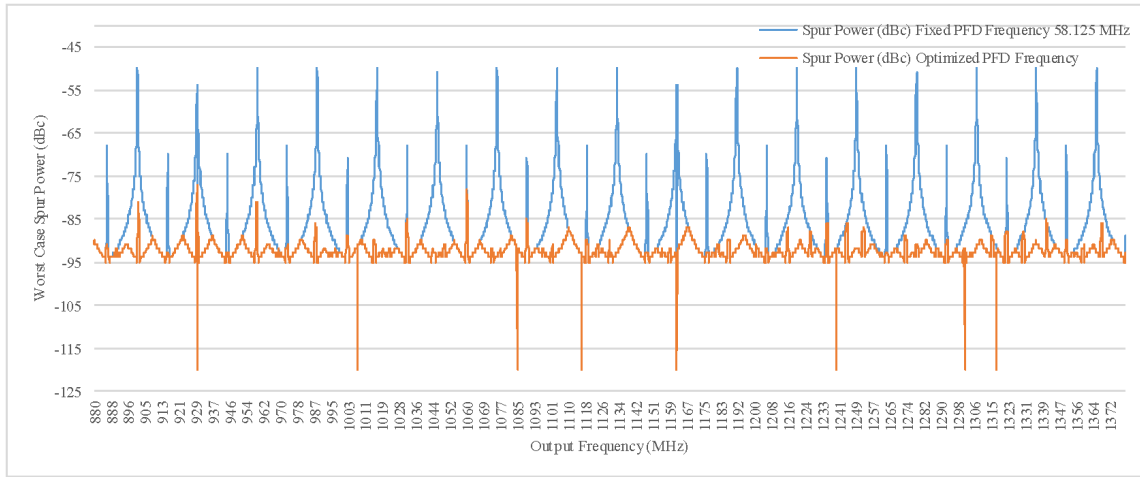
Figure 9. Spur reduction simulation when loop filter bandwidth is 150 kHz.
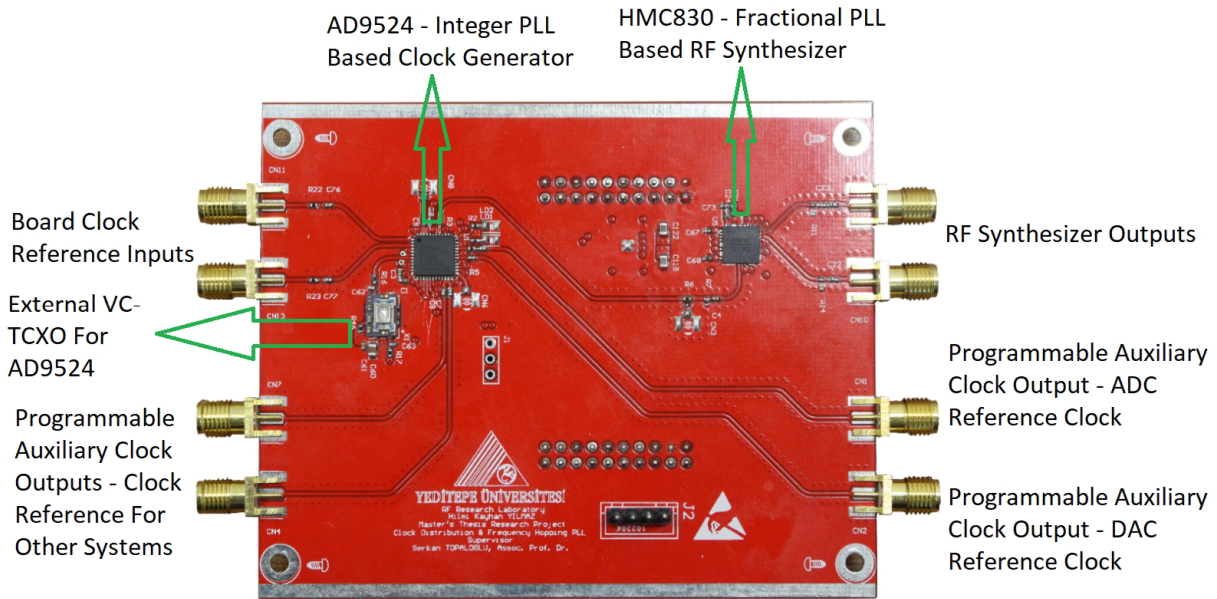

Figure 10. Prototype of the proposed design.

application meets the minimum requirements of telecommunication standards. Therefore, the proposed design is compatible with ITU and IESS standards.

Furthermore, the lock time of the RF PLL was measured with the signal source analyzer feature of the spectrum analyzer at the same frequency of simulations. The bandwidth capability of the spectrum analyzer is limited, so the frequency lock time was observed within 10 kHz frequency change. The frequency lock time measurement is shown in Figure 11. The lock time was measured as 186 microseconds, which was specified as 150 microseconds in the simulations. Both RF PLL lock time and changing reference frequency occurred within 186 microseconds. The measured time included both RF PLL lock time and update time for clock distribution

Table 2. Phase noise comparison.

Offset from carrier	Simulation	Measurement	ITU Standards	IESS-309 Standards
0.1 kHz	-78 dBc/Hz	-74 dBc/Hz	-	-60 dBc/Hz
1 kHz	-97 dBc/Hz	-95 dBc/Hz	-	-
10 kHz	-104 dBc/Hz	-102 dBc/Hz	-90 dBc/Hz	-
100 kHz	-112 dBc/Hz	-111 dBc/Hz	-	-90 dBc/Hz
1000 kHz	-141 dBc/Hz	-132 dBc/Hz	-	-

PLL registers. Therefore, the measured data were very close to simulations and verify the simulation results. Thus, the proposed design is suitable for FFHSS systems that have at least 200 microseconds of guard time between frequency changes.
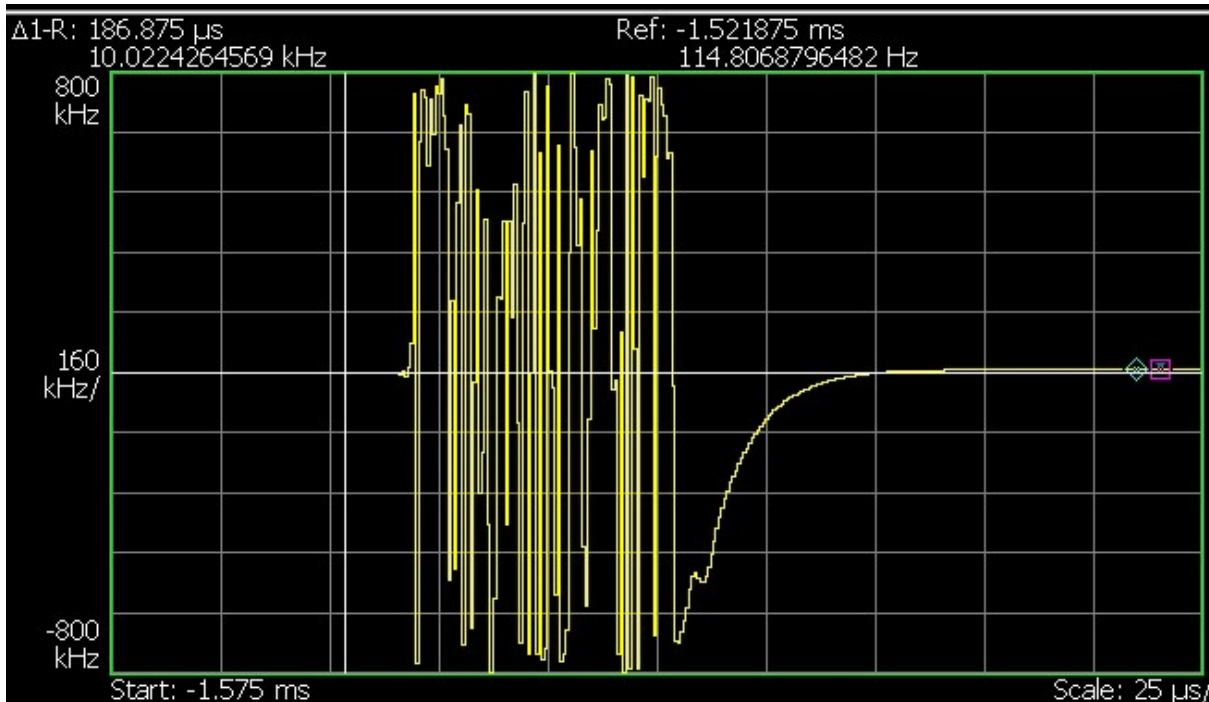

Figure 11. The lock time measurement result.

Spur performance of the proposed design was also measured at 1017.2 MHz to verify simulation results. The measured spectral view of HMC830 output at 1017.2 MHz when the reference frequency was 58.125 MHz is shown in Figure 12. VCO of HMC830 was locked at 2034.4 MHz and divided by 2 to obtain 1017.2 MHz output. The spur location was observed 25 kHz away from 2034.4 MHz at the VCO output. On the other hand, the spur was observed 12.5 kHz away from 1017.2 MHz as the VCO output of HMC830 was divided by 2 to obtain desired signal. Therefore, the spurious product was also divided by 2. In this condition, the spurious signal was located in spectral view as expected and its power response was 33 dBc.

As stated in the simulation section, spurious-free response was expected when the reference clock frequency was changed to 57.231 MHz to obtain the same VCO output frequency, 1017.2 MHz. The spectrum
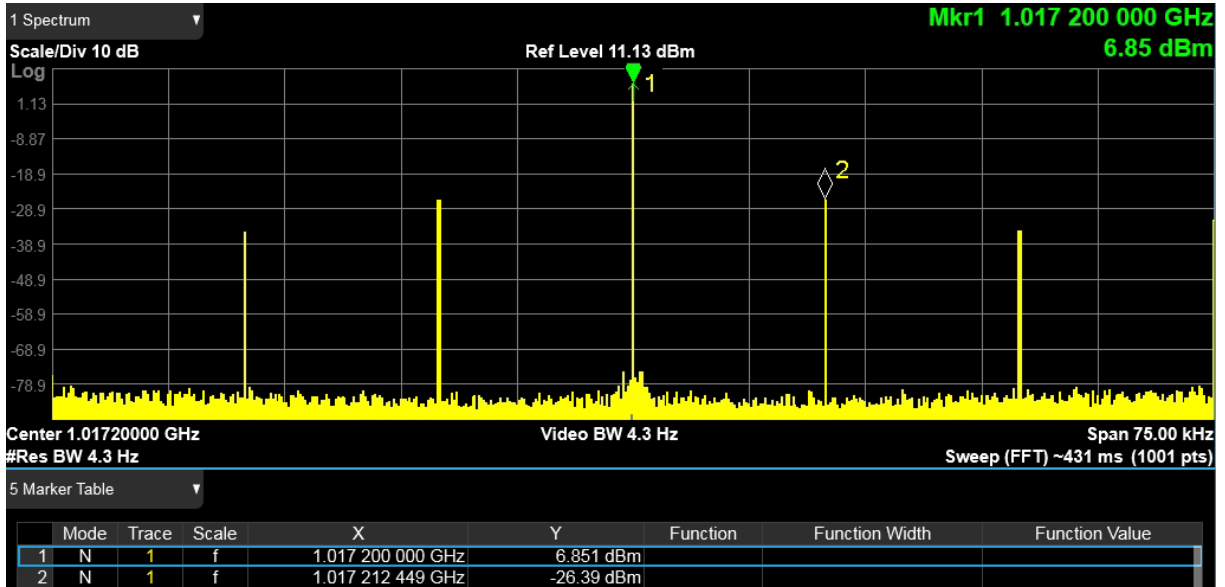
Figure 12. Spectral view of RF VCO output when the spur reduction method is not applied.

view of the measured response of VCO output is shown in Figure 13. The spurious response was eliminated in comparison to the previous measurement. By using the tunable reference frequency method, 57 dB spur reduction was provided at 1017.2 MHz.
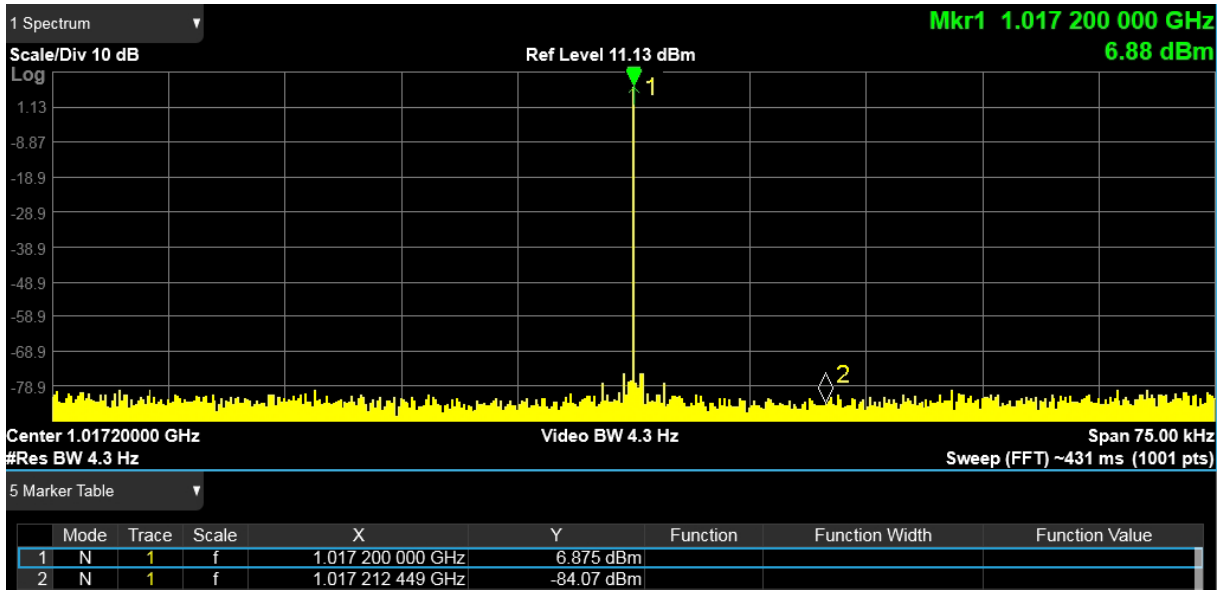

Figure 13. Spectral view of RF VCO output when the spur reduction method is applied.

5. Conclusion

The proposed spur reduction hardware, which is based on tuning the reference clock frequencies, is presented for fractional PLL-based frequency synthesizers. The hardware was designed as a clock distribution unit to provide spurious-free signals to both ADC and RF sections. Also, the proposed design was investigated for different

loop filter configurations to observe the effect of spur performance. Then the spur reduction performance was measured by using the proposed hardware and it was observed that it resulted in a 57 dB spur reduction. The performance of the proposed design was also compared with previous works and products given in Table 3 in terms of spur reduction and phase noise. Thus, the convenience of the spur reduction was proven by lock time measurements for the fast frequency hopping spread spectrum.

Table 3. Comparison with previous works.

	[10]	[11]	[12]	[6]	Proposed design
Type	IC	IC	IC	Discrete	Discrete
Supply (V)	1.8	2.5	2.5	3.3	3.3
Power (mW)	20	18	13.5	1500	1500
Frequency (GHz)	2.5 - 2.7	2.4/4.8	5.14 - 5.17	2	0.025 - 3
Phase noise (dBc/Hz)	-105	-104	-116	-140	-132
Spur reduction (dB)	20	10	20	48	57

Acknowledgment

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