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Replica bias circuit for common-source amplifier

Burak KELLECİ*
Department of Electrical and Electronics Engineering, İstanbul Okan University, İstanbul, Turkey

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Abstract: A replica bias circuit to set the current of common-source amplifier to reduce the gain variations across process, voltage, and temperature (PVT) changes is proposed. The gain of a common-source amplifier is set by the load resistor and transistor transconductance which is set proportional to a resistor using a constant-gm bias circuit. The success of constant-gm biasing depends on the accuracy of copying of generated current to the transistor. The leakage current at the transistor gate due to the electrostatic discharge protection diodes prevents the matching of the common source transistor current to the constant-gm circuit current. A low-power replica of the common-source amplifier is used to determine the current error which is minimized using a feedback circuit. Corner simulations indicate that gain variation across PVT reduced to ± 1.9 dB using the proposed biasing method as opposed to ± 9.9 dB for traditional biasing method for 1 μA leakage current. Monte Carlo simulations with process and mismatch indicate that the standard deviation of the gain is reduced to 0.34 dB from 3.57 dB.

Key words: Common-source amplifier, low-noise amplifier, design for manufacturing

1. Introduction

Common-source amplifier topology is preferred in low-noise amplifiers due to their high gain and low noise. Its input impedance is usually set using inductive degeneration or resistor feedback with DC blocking capacitor [1]. The gain of common-source amplifier is determined by transconductance of the transistor and the load resistor. Since transistor transconductance and resistor value do not track each other across process, temperature, and voltage (PVT) variations, the amplifier gain varies significantly. These PVT variations are mitigated by setting transistor transconductance proportional to a resistor using constant-gm circuit [2, 3]. The current of constant-gm circuit is usually copied using current mirrors and converted to voltage using a diode connected transistor to set the gate-source voltage of common-source amplifier. To reduce the bias circuit noise, a bias resistor is also used, as shown in Figure 1. Since the success of this technique depends on how well the constant-gm cell current is copied to the main amplifier, a high-precision bias circuit which uses a replica of the main amplifier is also proposed in the literature [4, 5]. However, these approaches do not set the bias current if there is a leakage current at the transistor input due to electrostatic discharge (ESD) protection diodes or any circuit component connected to the gate of the common-source amplifier. Moreover, the leakage current increases with temperature and it can be at mA level at 125° C [6]. Due to the extra voltage drop on the bias resistor, the current of common-source amplifier becomes a function of the leakage current. This increases the variation of performance parameters such as gain and bandwidth.

*Correspondence: kellecib@hotmail.com

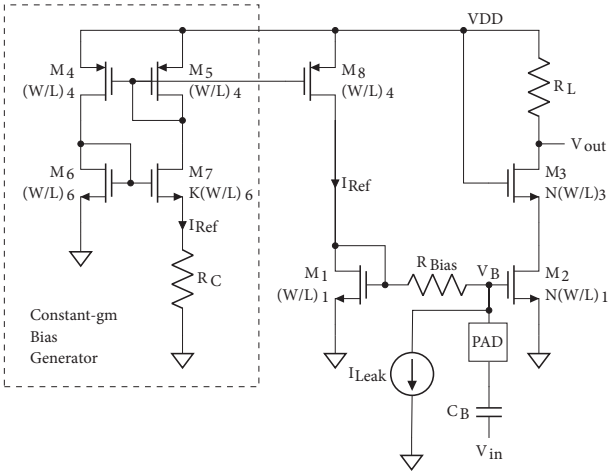


Figure 1. Traditional common-source amplifier with constant-gm circuit.

In this work, a biasing technique is proposed to compensate the effect of leakage current at the input of common-source amplifier. The current of the amplifier is determined using a replica circuit of the main common-source amplifier and this current is compared with the reference current. The error current is amplified and used to set the current of diode-connected transistor to achieve the desired bias current.

The rest of the paper is organized as follows. Mathematical background and design equations are discussed in Section 2. Simulation results are presented in Section 3. Concluding remarks are given in Section 4.

2. Replica bias circuit

The common-source amplifier with replica biasing technique is shown in Figure 2. Transistors M_2, M_3 and resistor R_L form the main common-source amplifier. The input signal V_{in} is AC coupled using external C_B capacitor. A low current replica of this main amplifier is formed using transistors M_9 and M_{10}. The unit transistor sizes in the main amplifier and in the replica circuit are selected as the same. To achieve the desired bias current, transistor sizes in the main amplifier are selected N times of the transistor sizes of the replica circuit. The current of replica circuit is copied using M_{11} and M_{12}. The reference current which is generated by the constant-gm circuit is subtracted from the current of M_{12} to determine the error current between actual current of the replica circuit and reference current. The error current is amplified by the current mirror formed by transistors M_{13} and M_{14}. The ratio M between M_{14} and M_{13} determines the current gain. The current of M_{14} is then subtracted from the current of M_8 and the resulting current is converted to voltage using diode connected transistor M_1. This voltage is applied to the gates of M_2 and M_9 through R_{Bias} resistor which is used to filter out the bias circuit noise. The current source I_{Leak} models the unwanted current due to ESD protection diodes or other external circuits connected to the gate of M_2. Since this leakage current generates voltage drop on the R_{Bias} resistor, the proposed method increases the current of M_1 so that the current of M_9 tracks the I_{Ref} current.

The current of M_9 differs from the current of M_1 due to the voltage drop on R_{Bias} and is given as

$$I_9 = \left[\sqrt{I_1} - R_{Bias} I_{Leak} \sqrt{\frac{1}{2}\left(\frac{W}{L}\right)_1 \mu_n C_{ox}}\right]^2, \tag{1}$$

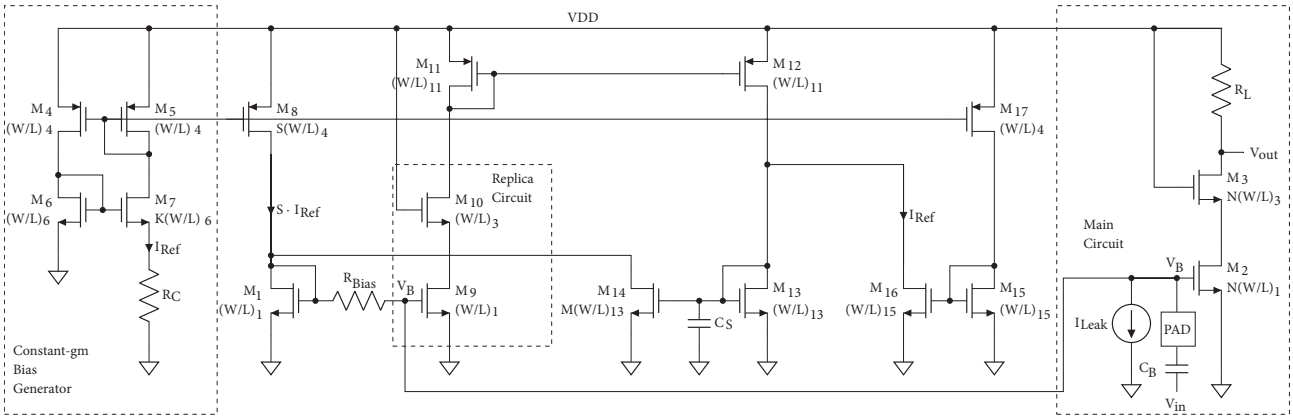


Figure 2. Proposed common-source amplifier with constant-gm circuit and replica bias circuit.

where μ_n is the NMOS transistor mobility and C_{ox} is the oxide capacitance per area. The drain current difference between M_9 and M_1 is

$$I_{Diff} = R_{Bias}^2 I_{Leak}^2 \frac{1}{2}\left(\frac{W}{L}\right)_1 \mu_n C_{ox} - 2\sqrt{I_1} R_{Bias} I_{Leak} \sqrt{\frac{1}{2}\left(\frac{W}{L}\right)_1 \mu_n C_{ox}}. \tag{2}$$

The current of the replica circuit is copied using M_{11} and M_{12}. The copied current is given as

$$I_{12} = I_9 = I_1 - I_{Diff}. \tag{3}$$

The reference current which is generated by the constant-gm circuit is subtracted from the current of M_{12} to determine the error current between actual current of the replica circuit and the reference current. The error current is given as

$$I_{Err} = I_9 - I_{Ref}. \tag{4}$$

The error current is amplified by the current mirror formed by transistors M_{13} and M_{14}. The ratio M between M_{14} and M_{13} determines the current gain. The current of M_{14} is then subtracted from the current of M_8 to set the current of M_1. The resulting current is given as

$$I_1 = S \cdot I_{Ref} - M \cdot I_{Err}. \tag{5}$$

Combining (3), (4), and (5) to solve I_9 results in

$$I_9 = \frac{S+M}{1+M} I_{Ref} - \frac{I_{Diff}}{1+M}. \tag{6}$$

Equation (6) indicates that I_9 is equal to I_{Ref} if S is equal to 1 and the current difference due to leakage is zero. Moreover, the current difference due to the leakage is also reduced by $1+M$.

The maximum leakage current that the proposed circuit can tolerate occurs if the feedback current drops to zero or in other words M_{13} and M_{14} operate at the edge cut-off region. In that case, the maximum tolerable leakage current is given as

$$I_{Leak,max} = \frac{1}{R_{Bias}} \sqrt{\frac{I_{Ref}}{\frac{1}{2}\left(\frac{W}{L}\right)_1 \mu_n C_{ox}}} \left(\sqrt{S} - 1\right). \tag{7}$$

The square root term in (7) is equal to overdrive voltage of M_9. Therefore, (7) is rewritten as

$$I_{Leak,max} = \frac{V_{ov,9}}{R_{Bias}} \left(\sqrt{S} - 1\right). \tag{8}$$

The S term determines the maximum leakage current tolerance and the relationship between I_9 and I_{Ref} as given in (6). Since setting S to 1 makes the maximum tolerable leakage current to zero, S value must be higher than one, but high S value increases mismatch between I_9 and I_{Ref}. To have a good matching between M_5 and M_8 the S value should be selected as an integer number. As a result, in this work S is selected as 4.

The replica bias circuit sets the desired current using a feedback circuit formed by M_9, M_{10}, M_{11}, M_{12}, M_{13}, M_{14}, M_1, and R_{Bias}. The loop consists of three common-source amplifiers. The first amplifier is formed using M_9 and diode connected M_{11}. The output of this amplifier is applied to the second amplifier which is formed using M_{12} and diode connected M_{13}. The output of the second amplifier is applied to the third amplifier which is formed by M_{14} and diode connected M_1. Therefore, assuming that the transconductance of a transistor is higher than its output conductance, the loop transfer function is given as

$$H(s) = \frac{gm_9}{gm_{11} + sC_{11,12}} \cdot \frac{gm_{12}}{gm_{13} + s\left[C_{13,14} + C_S\right]} \cdot \frac{gm_{14}}{gm_1 + sC_{14,1}} \cdot \frac{1}{sR_{Bias}C_{2,9} + 1},$$

where gm is the transconductance of the respective transistor; $C_{11,12}$ is the total gate capacitance of M_{11} and M_{12}; $C_{13,14}$ is the total gate capacitance of M_{13} and M_{14}; $C_{14,1}$ is the total gate capacitance of M_{14} and M_1; and $C_{2,9}$ is the total gate capacitance of M_2 and M_9. Since the transconductance of a MOS transistor is the ratio of its current to its overdrive voltage, the DC gain of first amplifier is the ratio of overdrive voltages of M_9 and M_{11}. The second amplifier has the highest gain since the current of M_{13} is the error current and lower than the current of M_{12}. The third amplifier gain is the ratio of transconductance of M_{14} to M_1.

Since all three amplifiers have pole frequencies close to each other, the feedback is third order. To stabilize the loop, one of the amplifiers output node should determine the dominant pole. In this work, the output of second amplifier is selected to determine the dominant pole because the second amplifier output node has higher capacitance value than the first and third amplifiers. Therefore, C_S capacitance is added at the output of the second amplifier. The output node of second amplifier is also an internal node and not affected by the change of the input capacitance of the main amplifier. To suppress the bias circuit noise, bias resistor is added between the input of first amplifier and the output of third amplifier. The nondominant pole is determined by the bias resistor which forms a RC filter with the gate capacitance of M_2, M_9, and external circuit capacitance. If the external capacitance is high enough, the dominant pole is set by the RC filter. In that case, the first and second amplifier output nodes determine the nondominant pole.

3. Simulations

The circuit with traditional biasing technique in Figure 1 and the circuit with the proposed replica biasing technique in Figure 2 are implemented and simulated in 0.18 μm CMOS technology with a nominal supply voltage of 1.8 V. The nominal gain of the main amplifier is set to 19.5 dB. The maximum leakage current that can be tolerated is calculated using (8). Since the overdrive voltage of M_9 is 150 mV, the maximum tolerable leakage current is 1.5 μA. Therefore, the leakage current is modeled using a current source with a nominal value of 0 A and maximum value of 1 μA. The supply voltage variation is $\pm$0.1 V. The minimum temperature is –40 °C and the maximum temperature is 85 °C. Leakage current, supply voltage and temperature are assumed uniform distributed in the Monte Carlo simulations. The component parameters are summarized in Table 1.

Table 1. Transistor and component sizes.

$(W/L)_1$	$4\ \mu m/0.18\ \mu m$	$(W/L)_3$	$1\ \mu m/0.5\ \mu m$
$(W/L)_4$	$20\ \mu m/2\ \mu m$	$(W/L)_6$	$4\ \mu m/0.18\ \mu m$
$(W/L)_{11}$	$20\ \mu m/2\ \mu m$	$(W/L)_{13}$	$4\ \mu m/2\ \mu m$
$(W/L)_{15}$	$4\ \mu m/2\ \mu m$	R_{Bias}	$100\ k\Omega$
R_c	$3\ k\Omega$	R_L	$1.4\ k\Omega$
M	20	N	20
K	4	S	4
C_S	50 pF		

The DC gain and phase margin for nominal condition is shown in Figure 4. The low frequency loop gain at 10 kHz is 24.3 dB at nominal condition and between 10.35 dB and 25.83 dB across PVT. The gain-bandwidth product of the loop is 2.87 MHz at nominal condition and between 0.36 MHz and 4.28 MHz across PVT. The phase margin is 70° at nominal condition and 60.8° at worst case condition across PVT.

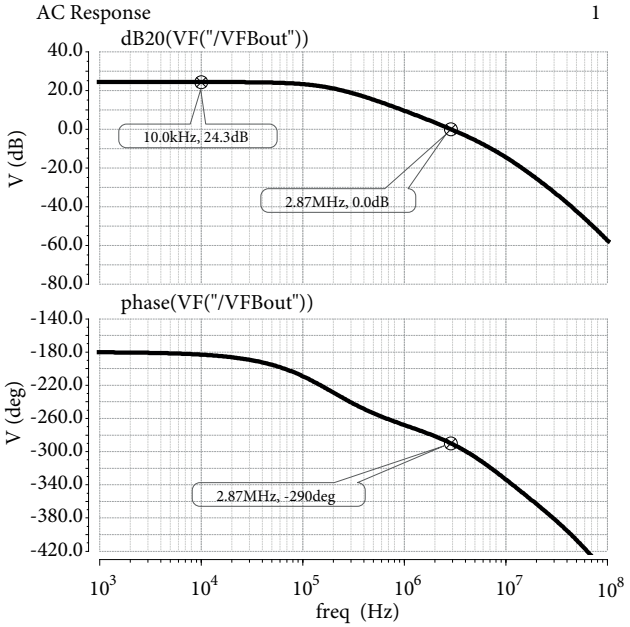
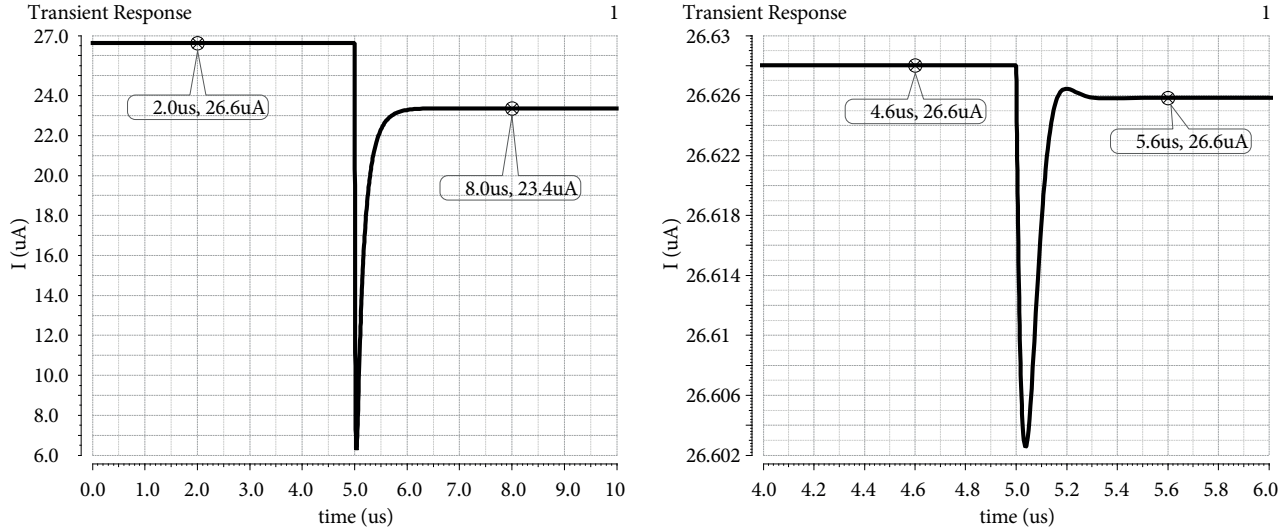


Figure 3. Phase margin and DC gain of the loop.

The settling of the replica biasing technique is simulated by applying a current pulse as a leakage current. The current of M_9 is settled within 1 μs as shown in Figure 4 for 1 μA. The current of M_9 is settled within 0.4 μs as shown in Figure **??** for 1 nA. The bias current for both large and small leakage step currents the circuit settles fast without significant ringing.

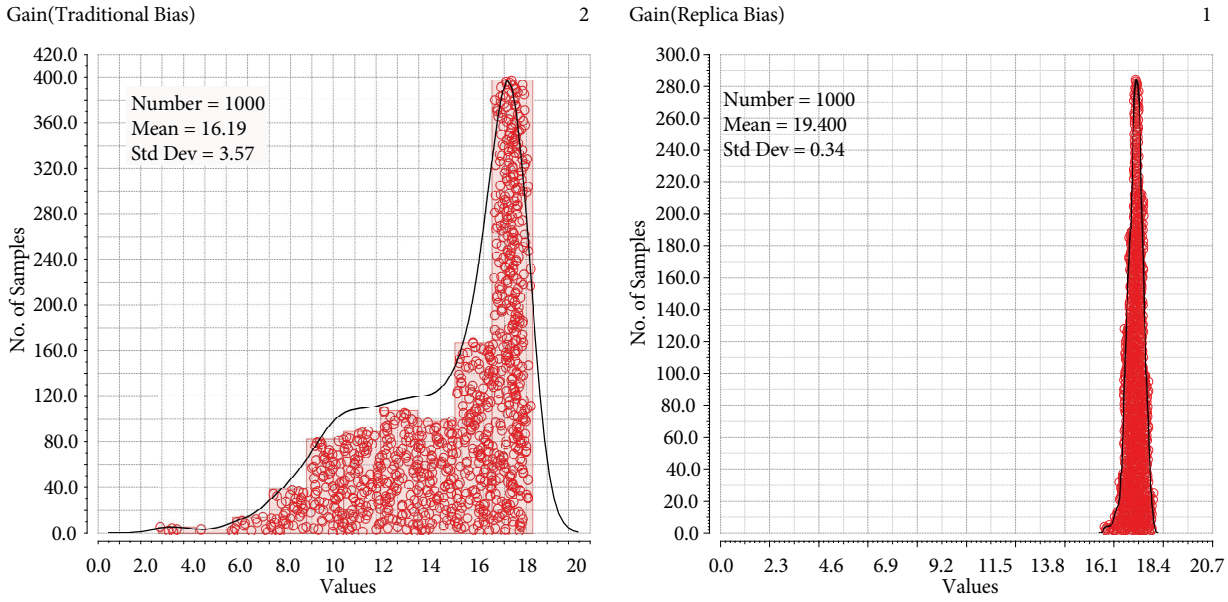
The maximum gain of the main amplifier is 21.3 dB across PVT for traditional and replica biasing techniques. The minimum gain of the main amplifier is 17.5 dB for replica biasing technique and 1.5 dB for traditional biasing technique. The current consumptions of replica and traditional biasing circuits for nominal conditions without current consumption of main amplifier and constant-gm cell are 176.7 μA and 24.6 μA, respectively. Since the number of current mirrors is higher in replica biasing technique than in traditional



(a) 1 µA Pulse Current (b) 1 nA Pulse Current

Figure 4. Transient response of the M_9 current.

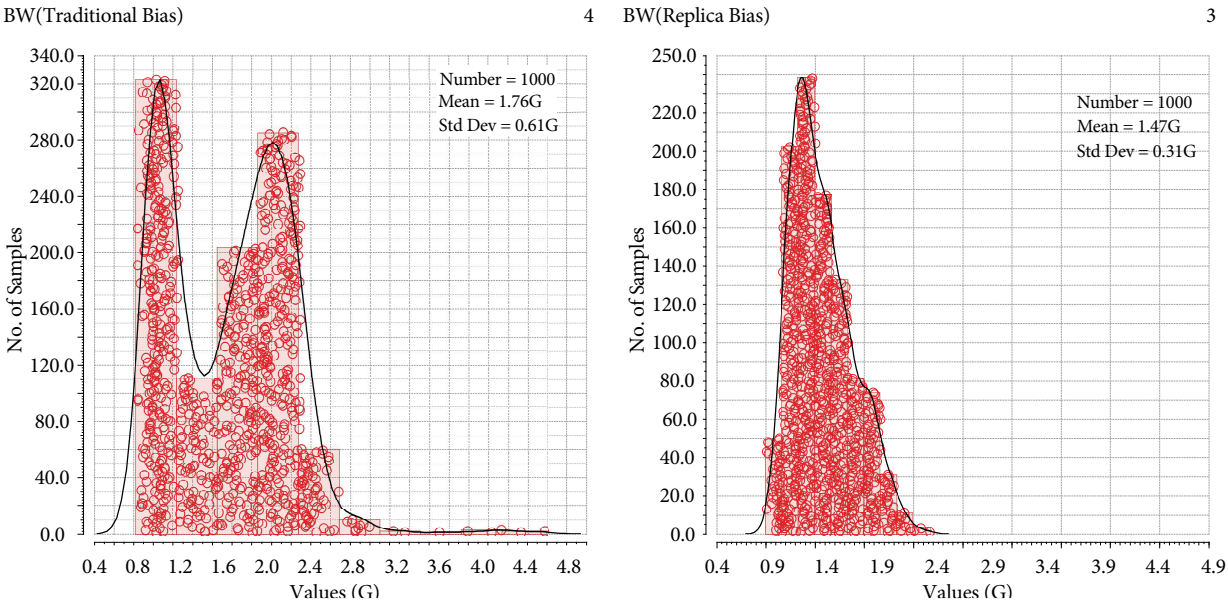
biasing technique, Monte Carlo simulations with process and mismatch are also performed. The correlation due to the proper layout of current mirrors is also taken into account. Monte Carlo simulation results for circuit with traditional bias shown in Figure **??** indicate a mean gain of 16.19 dB and 3.57 dB standard deviation. Monte Carlo simulation results for proposed circuit shown in Figure 5 indicate a mean gain of 19.4 dB and 0.34 dB standard deviation.



(a) Traditional bias circuit (b) Proposed replica bias circuit

Figure 5. Monte Carlo simulation results of the Gain (dB) with process and mismatch errors.

The bandwidth variation of the main amplifier is also reduced from 0.61 GHz for traditional biasing technique as shown in Figure **??** to 0.31 GHz for replica biasing technique as shown in Figure 6.



(a) Traditional bias circuit (b) Proposed replica bias circuit

Figure 6. Monte Carlo simulation results of the Bandwidth (GHz) with process and mismatch errors.

4. Conclusion

A replica biasing technique to stabilize the current of common-source amplifier across PVT in the presence of leakage current is proposed. Monte Carlo simulations indicate that the proposed technique reduces the standard deviation of gain and bandwidth of common-source amplifier compared to the traditional biasing technique. Corner simulations indicate that it is possible to achieve less than ± 2 dB gain variations for common-source amplifier across PVT in the presence of leakage current.

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