Turkish Journal of Electrical Engineering & Computer Sciences

http://journals.tubitak.gov.tr/elektrik/

Research Article

Turk J Elec Eng & Comp Sci
(2020) 28: 2493 – 2506

doi:10.3906/elk-1909-47

Low power and low phase noise VCO with dual current shaping for IoT applications

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Received: 07.09.2019 • **Accepted/Published Online:** 21.01.2020 • **Final Version:** 25.09.2020

Abstract: In this paper, two low phase noise and power consumption VCO circuits, which are suitable for Internet of things (IoT) applications, are proposed. In the first structure, in order to have more control of the current consumption, the current shaping technique is used in the PMOS and NMOS biasing circuit. In the second structure, for increasing the oscillation amplitude and reducing the phase noise, independent biasing for the NMOS section is used. In both structures, to increase the frequency tuning range (FTR), without using a capacitor bank, the varactor is used in the biasing structure. In the first structure the supply voltage, output frequency, power consumption, and phase noise are 0.8 V, 2.44 GHz, 0.37 mW, and -117.5 dBc/Hz, respectively, but in the second structure, the supply voltage, output frequency, power consumption, and phase noise are 0.8 V, 2.44 GHz, 0.62 mW, and -120 dBc/Hz, respectively. It should be noted that the two structures are designed and simulated in 65-nm CMOS technology. Finally, the results show that the figure-of-merit for the first and second structures is –190 dBc/Hz and –190.2 dBc/Hz, respectively.

Key words: Internet of things, LC voltage-controlled oscillator, low power, current shaping

1. Introduction

The Internet of things (IoT) is modern technology that provides the ability to send data through communication networks for many things. With this technology, the things collect useful data from the surroundings by using different sensors and transfer them to a central system for processing and decision-making. The IoT can play a significant role in many fields such as medicine, smart cities, urban security, and radio frequency identification (RFID) [1]. Power consumption management is one of the main challenges of IoT chips. In order to increase the lifetime of the chip, solar cells, thermoelectricity generators (TEGs), or electromagnetic waves are usually used. Since these sources have limited power generation to manage the power of the chip, the subblocks must consume as little power as possible.

One of the main blocks in IoT chips and other electronic devices, such as receivers and radio transmitters, satellites, and GPS, is the frequency synthesizer. This block generates the required frequency levels accurately. In a special frequency band, the block is used to select the desired channels in the band. As shown in Figure 1, the synthesizer consists of phase frequency detector (PFD), charge pump (CP), voltage-controlled oscillator (VCO), and frequency divider subblocks [2]. The VCO block that produces the desired frequency is one of the most important synthesizer subblocks. The VCO has higher power consumption than the other synthesizer blocks, so designing a VCO with low power consumption is important for IoT applications.

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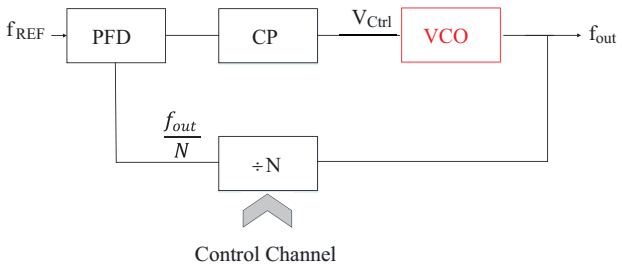

Figure 1. Block diagram structure of synthesizer.

Single-port or LC oscillators operate using an inductor and capacitor structure and the internal resistor has been removed by a parallel negative resistor in this structure. Colpitts, Clapp, and cross-coupled circuits creating the negative resistor are important for LC oscillator circuits. Colpitts and Clapp circuits require more transconductance (G_m) than cross-coupled circuits to make oscillation conditions, which increases power consumption. For this reason, these oscillators are rarely used. The cross-coupled circuit oscillates with less power, and its high reliability and flexibility make its structure more popular [3].

According to the above statements, the reduction of power consumption and phase noise are the main challenges in VCO circuit design. Typically, various techniques are used to reduce power consumption.

The triple-well technique is often used in digital CMOS circuits for body-biasing and low-power circuits with high efficiency. In analog circuits, this technique is often used to reduce noise. In a triple-well system, the insulation p-well layer and the combination of deep-n-well and n-well layers are used. The capacitors of the mentioned layers in this structure are in series and therefore the effect of the drain-bulk capacitor is reduced [4, 5].

A dynamic body bias technique in MOS transistors is one of the solutions for voltage threshold management. In addition, in semiconductor technology, this technique is used to control the leakage current when the transistor is off and also to enhance its performance. The body bias voltage dynamically changes with the variations in the gate voltage value of MOS transistors. When the gate voltage is high, the switching transistors are turned ON and the threshold voltage and delay will be decreased. If the gate voltage is low, the switching transistors are turned OFF and the changing threshold voltage decreases leakage current and static power [6].

In the feedback technique of the output voltage, the output signal is first transferred to the biasing input section, and after ensuring the oscillation of the circuit, by using sampling its output signal, the biasing voltage, is reduced and this reduction decreases the power consumption of the circuit [5, 7].

With the advancement of technology transistors have become smaller than before, so noise has become one of the main problems in the VCO circuit, which is investigated according to the phase noise parameter. There are many approaches to reduce phase noise. In [8, 9], designing a three-path inductor with a suitable quality factor, phase noise was greatly improved, but this structure increases the chip area, and on the other hand, in this approach BiCMOS as an expensive technology is used. Therefore, this structure is not suitable for IoT applications.

In the LC VCO structure with a cross-coupled circuit using the current reuse technique, the G_m value has been doubled by using cross-coupled PMOS transistors. There is always a trade-off between power consumption and phase noise in VCO circuits, and it should be noted that a better phase noise can be achieved in this circuit with lower power consumption relative to the other circuit. This structure plays an important role in creating

a robust start-up [10]. In order to reduce power consumption, the circuit usually transfers to lower power consumption classes after ensuring the oscillation of the circuit in the start-up process. The VCO operation class plays an important role in power management. Generally, the FoM of class-C is better than class-B VCOs [11, 12].

In some circuits, current-reuse structures have been used to increase the main core G_m without increasing the high current consumption [8, 9]. Using this structure, the G_m value is almost doubled and it improves phase noise, so the power consumption becomes lower than before. In [13], current shaping techniques are used to reduce phase noise. In this method, by controlling the current of tail transistors, the effective value of the impulse sensitivity function (ISF) is reduced and the phase noise is improved.

In this paper, two low power VCOs are designed. For the purpose of improving FOM and reducing phase noise, a dual current shaping technique is used in the first circuit. With the help of this technique, the main current of the circuit can be more controllable and also the power dissipation and phase noise are decreased. In the second VCO structure, with biasing tail NMOS transistors, the phase noise is improved by about 3 dBc/Hz. The rest of this paper is organized as follows: In Section 2, two proposed designs are presented. In Section 3, the results of the simulation are explained, and finally the conclusion is presented in Section 4.

2. Proposed structures

As mentioned in the previous sections, the current shaping technique is used to improve the control ability of phase noise and power consumption [13]. The phase noise is defined as in (1):

$$L(\Delta\omega) = 10log[\frac{\frac{i^2}{\Delta f}}{2q_{max}^2\Delta\omega^2}\Gamma_{rms}^2]. \tag{1}$$

In this equation, Γ_{rms} is the effective value of the ISF, $\frac{i^2}{\Delta f}$ is power spectrum density of current noise, q_{max} is the maximum charge displacement across the capacitor, and $\Delta\omega$ is offset frequency. According to this equation, if Γ_{rms} is reduced, the phase noise will be improved. In the current shaping method, at the zero crossing point of the VCO output, the ISF has the highest value. Therefore, in this point, the transistor current will be cut off and the effective value of the ISF is decreased, and the phase noise is improved [14, 15].

The conventional VCO circuit structure with current shaping technique is shown in Figure 2. In this circuit, the amount of current consumption is determined by the output voltage applied to the gate of tail transistors. As a result, the power consumption is determined according to the output voltage amplitude. Thus, controlling the current consumption becomes difficult in this condition.

2.1. Proposed VCO I structure

The proposed VCO I circuit is shown in Figure 3. In this structure, for solving the problems and controlling power consumption, dual current shaping circuits have been used. The first current shaping circuit includes C_{var3} and C_{var4} capacitors and M_{n3} and M_{n4} transistors. The outputs of this circuit mean that V_{O+} and V_{O-} are applied to the gate of the M_{n3} and M_{n4} transistors. By adjusting the V_{cr} voltage switches the tail transistors could be properly turned on and off.

Since the current reuse technique has been used in the proposed circuit, to have better control of power consumption and to achieve the best phase noise, another current shaping structure is also used in the bias

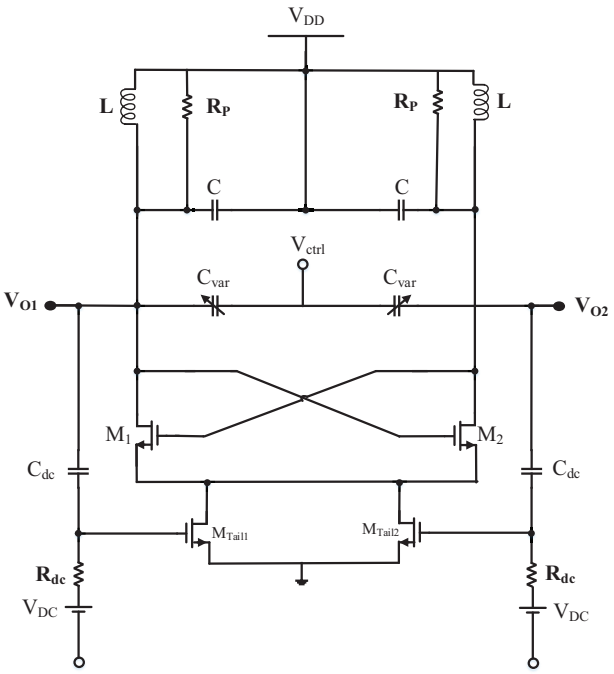

Figure 2. Conventional VCO circuit structure with current shaping technique [13].

section of the cross-coupled PMOS transistors. These current shaping structures can have more control of current consumption of the cross-coupled transistors of the PMOS and NMOS sections. Thus, the current and power consumption can be adjusted to the optimum level that is suitable for IoT applications. In order to improve the phase noise of the circuit, according to Equation (1), the amount of current consumption and thus the ISF at zero crossing point have the lowest value. Due to the voltage amplitude applied to the gate of transistors of current shaping structures, the effects of NMOS transistors are greater than those of PMOS. The amount of variations in V_{cr1} and V_{cr2} are determined according to the output voltage, C_{var}, and R_{dc}. Circuit performance can be improved by adjusting these parameters.

Also, to remove the second harmonic at nodes Y and X, the capacitors C_1 and C_2 at the Y node and C_3 and C_4 at the X node, which have a good effect on improving the phase noise of the circuit, were used. In the proposed structure, the resistor from VDD to ground is high, which reduces the power consumption of the circuit. On the other hand, the use of C_1, C_2, C_3, and C_4 reduces the effect of these resistors. Therefore, the amount of these capacitors that has the best effect on phase noise and power consumption should be chosen optimally. The independent bias of the PMOS's body is another technique that reduces phase noise in this design. Equation (2) is related to the threshold voltage of the PMOS transistors:

$$V_{Th} = V_{T0} + \gamma(\sqrt{|-2\Phi_F + V_{SB}|} - \sqrt{|-2\Phi_F|}). \tag{2}$$

In this equation, V_{T0} is the threshold voltage of the PMOS transistors for when the voltages of the body are the same as that of the source. γ is the coefficient of the body effect that depends on the capacity of the gate oxide layer, the doping ratio, and the silicone layer diffusion. Φ_F is the surface potential and V_{SB} is the source-body voltage. By changing the body voltage (V_B), the V_{SB} voltage and thus the V_{TH} are changed. By

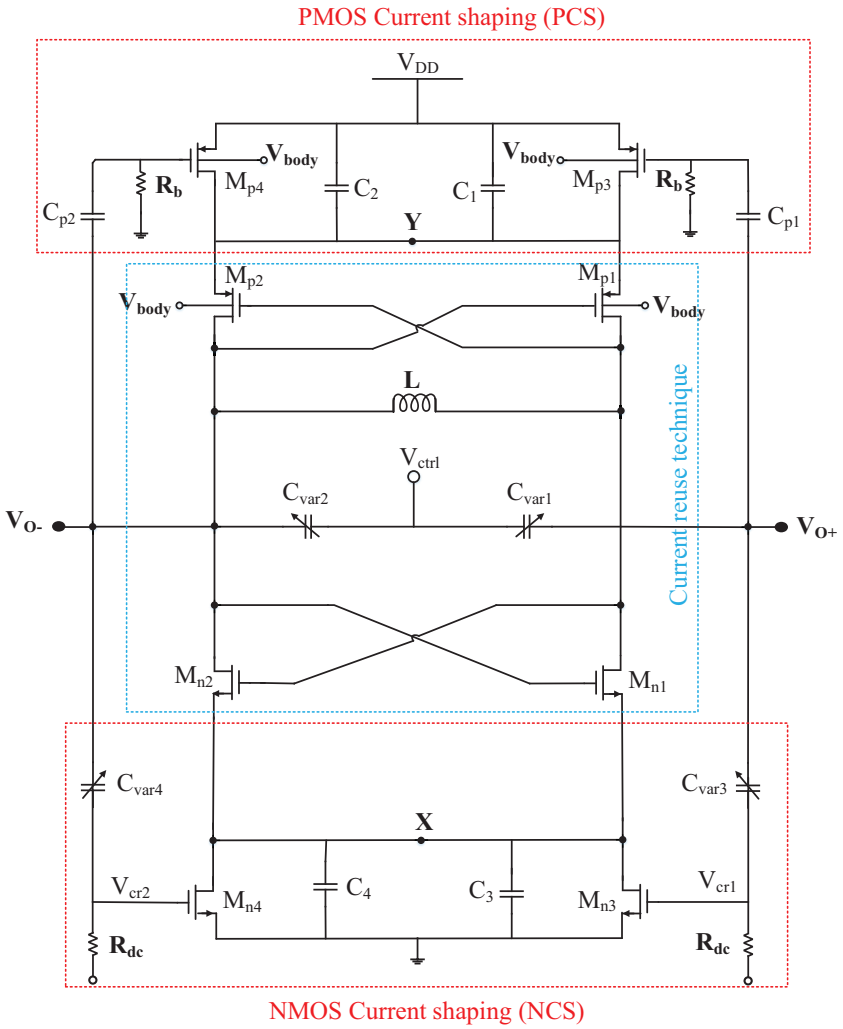

Figure 3. Proposed VCO I circuit.

changing the V_{Th}, the current consumption as well as the phase noise could be improved. Here, the trade-off between phase noise and power consumption should be considered by choosing the proper voltage of the body of the PMOS transistors.

By appropriately adjusting the dimensions of the transistors, the output waveforms, power consumption, phase noise, and figure-of-merit (FoM) are improved. FoM is defined as in Equation (3):

$$FoM = L(f_{offse}) - 20log(\frac{f_0}{f_{offset}}) + 10log(\frac{P_{DC}}{1[mW]}). \tag{3}$$

In this equation, $L(f_{offse})$ is the phase noise in the offset frequency f_{offset}, f_0 is the central frequency, and P_{DC} is the power consumption of the VCO core. The VCO performance is improved by FoM reduction.

2.2. Proposed VCO II structure:

Generally, the output phase noise is improved by increasing the amplitude of oscillation [7]. However, increasing the output amplitude usually increases the power consumption. In VCO I, due to the use of the current shaping technique in the NMOS and PMOS biasing transistors, the output amplitude is low. To solve this problem, the VCO II circuit has been proposed. The output amplitude and phase noise are improved by this design. The proposed VCO II is shown in Figure 4. The difference between VCO I and VCO II is their biasing characteristics. Thus, the tail transistors of the NMOS current source are directly biased with DC voltage and the current shaping technique is only used in the PMOS current source. By applying the appropriate voltage to the gate of the tail transistors, better phase noise could be obtained. However, the direct bias of the tail transistors will increase the current and power consumption of the circuit rather than the previous design. The amount of bias is regulated by considering the current consumption and the phase noise improvement. The range of voltage variations of V_{CTRL} is selected according to the allowed range of bias voltage in 65-nm CMOS. As a result, the reliability of the circuit will be improved. The simulation results of these two circuits are presented in the next section according to the mentioned analysis.

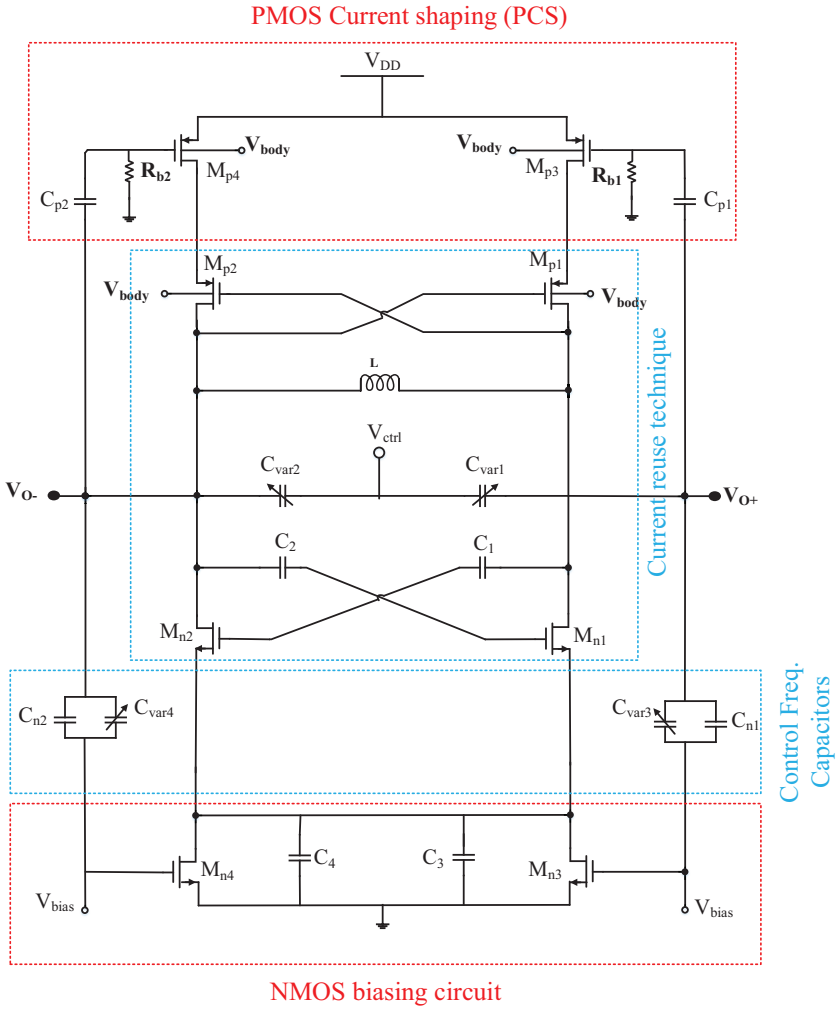

Figure 4. Proposed VCO II circuit.

3. Simulation results

Simulations of the two proposed structures based on 65-nm CMOS technology in the frequency range of the S band are presented in this section. It should be noted that postlayout simulations have been done in Cadence software.

3.1. Results of the postlayout simulation of the VCO I

The VCO I output from start-up to steady state is shown in Figure 5. As can be seen from this figure, the circuit reaches a stable point at 10 ns. The output oscillation amplitude in this circuit is about 360 mV and the frequency of this VCO is about 2.44 GHz.

Applying V_{O+} and V_{O-} to the gate of current-shaping transistors related to NMOS and PMOS bias, the current consumption of the circuit is shown in Figure 6. Zero crossing points of the output waveform have the lowest current consumption, while the ISF is maximum. The effective value of the ISF is obtained according to Equation (4):

$$\Gamma_{eff}(\omega_{0t}) = \Gamma(\omega_{0t})\alpha(\omega_{0t}). \tag{4}$$

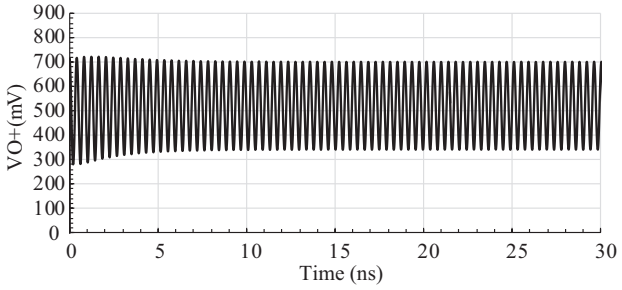

Figure 5. Start-up and steady state of VCO I output.

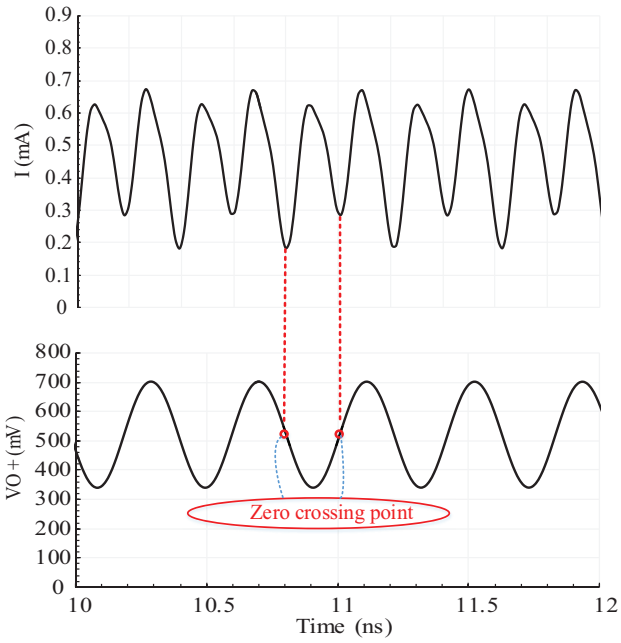

Figure 6. Current consumption variations according to output voltage waveform.

In this equation, $\alpha(\omega_{0t})$ is the noise modulation function (NMF) [14, 15]. This equation indicates that the thermal noise of the switching transistors is not constant and is changed by $\alpha(\omega_{0t})$. By decreasing the NMF, which is dependent on oscillations in the current waveform, the ISF value is reduced, and according to Equation (1), the phase noise is reduced. The current amplitude is varied from 0.18 mA to 0.67 mA, which has less amplitude than conventional ones. The DC value of this current is approximately 0.46 mA.

The phase noise of VCO I against offset frequency variations is shown in Figure 7. The phase noise ratio at offsets of 1 MHz and 3 MHz are –117.5 dBc/Hz and –127.4 dBc/Hz, respectively. According to the results and Equation (3), the FoM at offset of 3 MHz is about –190 dBc/Hz.

The range of output frequency according to the V_{CTRL} voltage variations are shown in Figure 8. By changing the control voltage from 0 to 0.7 V, the frequency varies from 2.43 GHz to 2.53 GHz. The value of K_{VCO} is acceptable in these frequency variations and the circuit is not sensitive to low changes of control voltage.

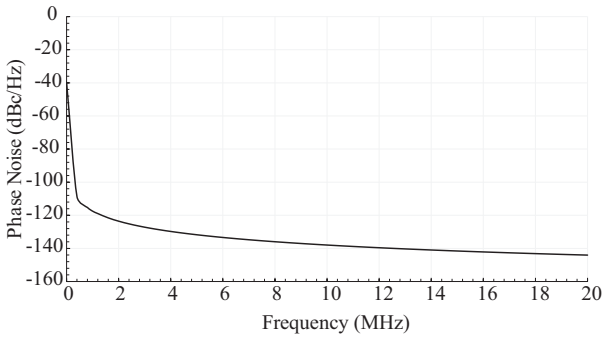

Figure 7. Phase noise of VCO I against offset frequency.

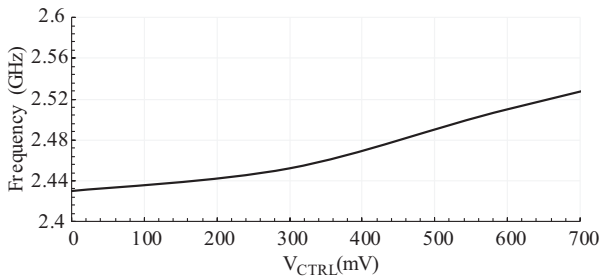

Figure 8. Range of output frequency according to V_{CTRL} voltage variations.

The effect of temperature variations relative to frequency and phase noise for VCO I is shown in Figure 9. The temperature coefficient (TC) of these parameters is defined as in Equations (5) and (6):

$$TC_{Freq} = \frac{Freq_{Max} - Freq_{Min}}{Freq_{27\circ} \times (T_{Max} - T_{Min})}, \tag{5}$$

$$TC_{PN} = \frac{PN_{Max} - PN_{Min}}{PN_{27\circ} \times (T_{Max} - T_{Min})}. \tag{6}$$

In these equations, T_{Max} and T_{Min} are the maximum and minimum operating temperatures. $Freq_{27}$ and $P_{27\circ}$ are the frequency and phase noise at 27 °C, respectively. In Equation (5), Fre_{Max} and Fre_{Min} are the highest and lowest frequencies, and in Equation (6), P_{Max} and PN_{Min} are the maximum and minimum phase noise. In the best temperature range, the TC values of frequency and phase noise parameters are 127 ppm and 270 ppm, respectively.

The curve of frequency variations of VCO I versus supply voltage variations is shown in Figure 10. With 20% change in supply voltage, the frequency is varied by about ±13 MHz.

In Figure 11, the Monte Carlo simulations for frequency and phase noise of the VCO I are shown for process and mismatch variations over 1000 runs. The mean value (μ) and standard deviation (σ) for frequency are 2.44 GHz and 28.4 MHz, respectively. The mean and standard deviation for phase noise are –117.9 dBc/Hz and 0.56 dBc/Hz, respectively. As a result, the variation coefficient (σ/μ) for frequency and phase noise are about 1.1% and 0.47%, respectively.

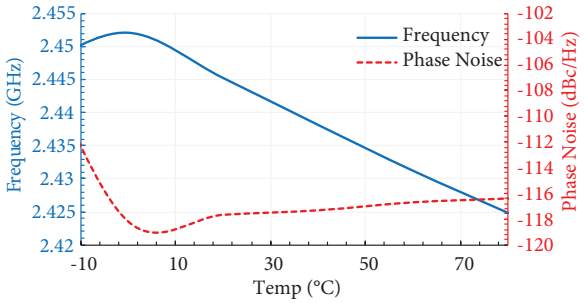

Figure 9. The effect of temperature variations relative to frequency and phase noise for VCO I.

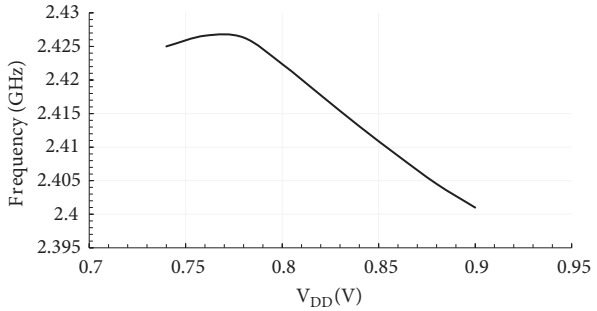

Figure 10. Frequency variations of VCO I versus supply voltage variations.

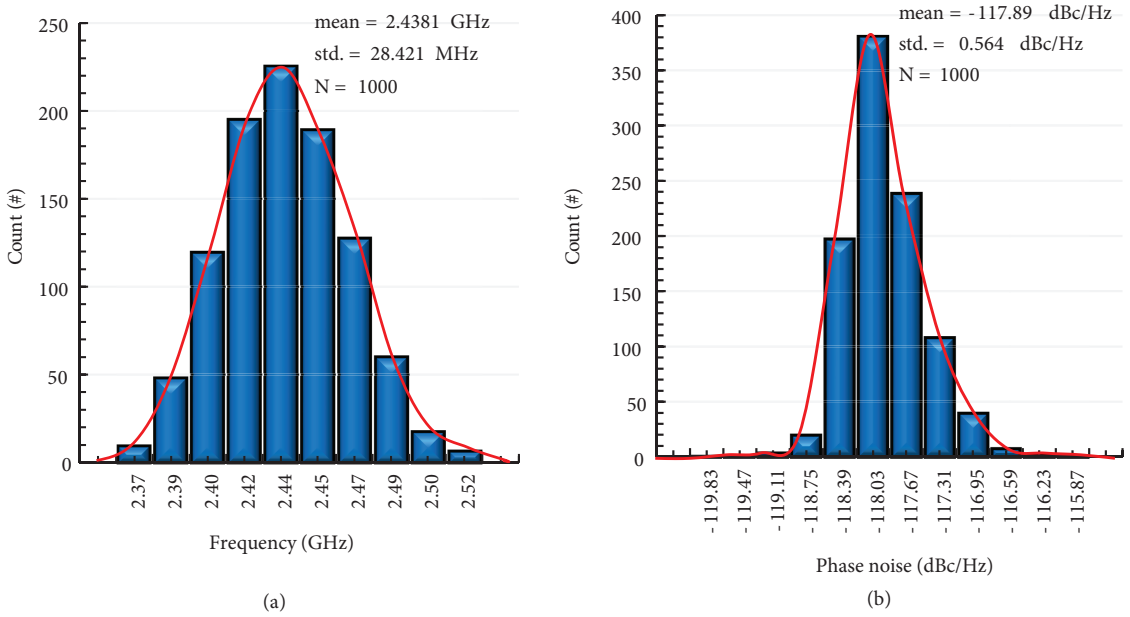

Figure 11. Monte Carlo simulation of VCO I for a) frequency, b) phase noise.

3.2. Results of the postlayout simulation of the VCO II

As discussed in the previous section, due to the use of the current shaping technique in the bias section of the NMOS and PMOS transistors, the output amplitude of VCO I is low. By solving this problem in the VCO II, the oscillation amplitude and phase noise are improved. The output of the VCO II from start-up to steady state is shown in Figure 12. The output oscillation amplitude of this circuit is about 520 mV. The output circuit reaches a stable point at 5 ns and the frequency of this VCO is about 2.44 GHz.

Figure 13 shows the current consumption of the circuit according to the output waveform. The DC consumption current is increased because the direct bias of NMOS transistors is used in the VCO II. Since the current shaping structure in NMOS transistors is not used, the current loss at zero crossing times is less than in the previous circuit.

The phase noise according to offset frequency is shown in Figure 14. The phase noise ratio at offset frequencies of 1 MHz and 3 MHz are –120 dBc/Hz and –130 dBC/Hz, respectively.

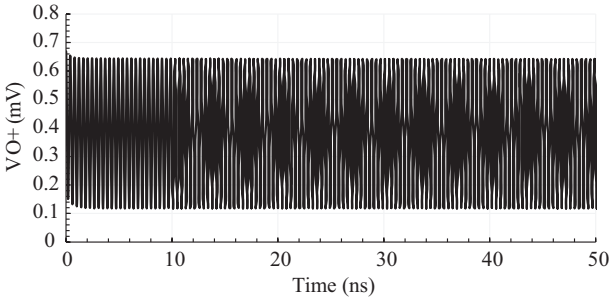

Figure 12. Start-up and steady state of VCO II output.

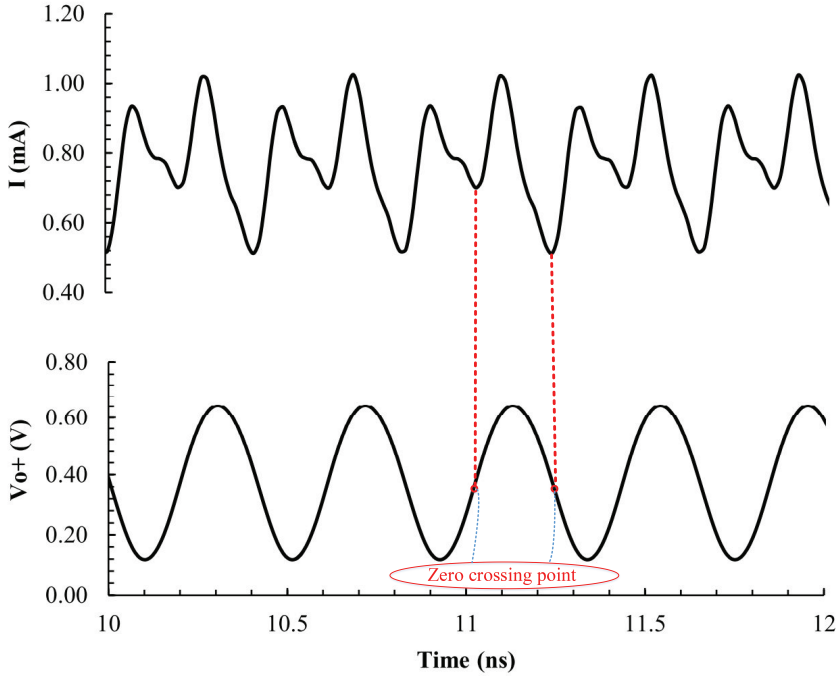

Figure 13. Current consumption variations versus the output voltage waveform.

The effect of temperature variations relative to frequency and phase noise of the VCO II is shown in Figure 15. These parameters are investigated within temperature variations from –10 °C to 80 °C. According to this figure and Equation (5), the TC values of frequency and phase noise are 104 ppm and 250 ppm, respectively.

The curve of frequency variations of VCO II versus the voltage variations is shown in Figure 16. These variations are about ±17 MHz.

A set of 1000 runs of Monte Carlo simulations for frequency and phase noise of VCO II are shown in Figure 17. These simulations are related to mismatch and process variations. The mean value (μ) and standard deviation (σ) for frequency are 2.41 GHz and 24.76 MHz, respectively. The mean and standard deviation for the output phase noise were determined as –119.8 dBc/Hz and 0.6 dBc/Hz, respectively. As a result, the coefficient of change (σ/μ) for frequency and phase noise are about 1% and 0.5%, respectively.

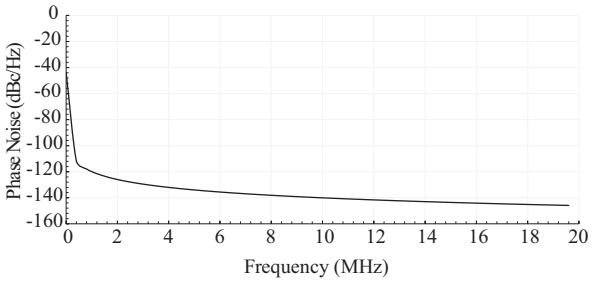

Figure 14. Phase noise of VCO II versus offset frequency.

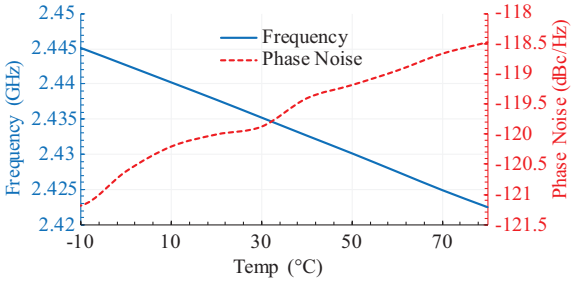

Figure 15. The effect of temperature variations relative to frequency and phase noise.

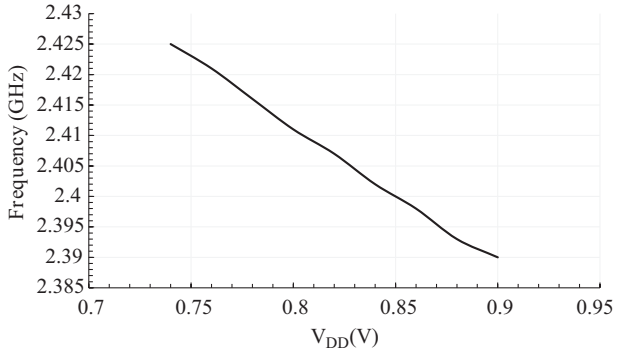

Figure 16. Frequency variations of VCO II versus supply voltage variations.

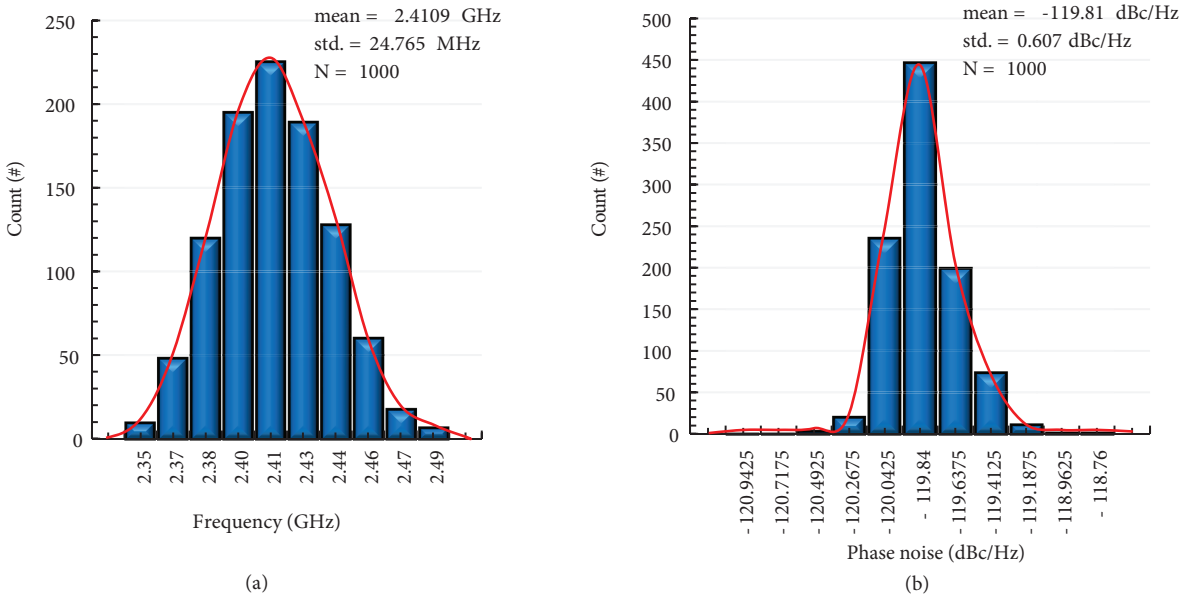

Figure 17. Monte Carlo simulation of VCO II for a) frequency, b) phase noise.

3.3. Discussion of the results

The layout designs of the two proposed circuits are shown in Figure 18. To have proper operation of the circuit in the postlayout simulations, these two circuits have been designed symmetrically. To reduce the parasitic capacitors and resistors of the circuit, the various parameters of each element are appropriately selected. On the other hand, suitable metal layers are used for connections between elements of the circuit. The layout dimensions of VCO I and VCO II are approximately the same and equal to 506 μm $\times$ 622 μm.

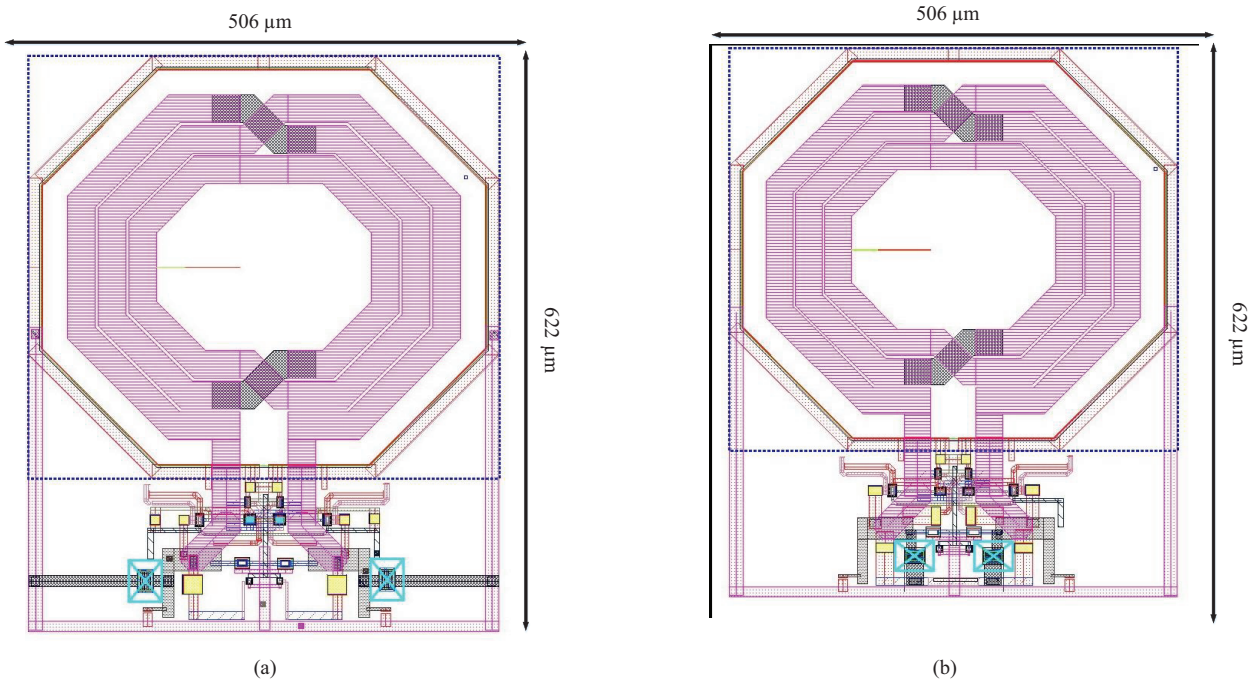

Figure 18. Layout design of the proposed circuits: a) VCO I, b) VCO II.

Table 1 shows the various parameters related to the two proposed structures. By comparing the two structures, VCO I in terms of power consumption and sensitivity to supply voltage variations and VCO II in terms of phase noise, the output amplitude and temperature sensitivity have good performance compared to other structures. Generally, the FoMs of two circuits are approximately same.

Table 2 shows the comparison results of the two proposed structures with the other designs presented in recent years. The last column is related to the used techniques for the purpose of decreasing the noise figure. In [10], [18], and [19] the current shaping technique has been used to reduce phase noise. The power consumption and FoM of the proposed circuits are improved in comparison with the other referenced circuits. The other parameters such as phase noise and the range of frequency variations are acceptable. In comparison with different designs, the technology and trade-off between the various parameters of structures should be considered.

4. Conclusions

In this paper, two LC VCOs are presented and simulated in 65-nm CMOS technology. In the first proposed VCO, to decrease the power consumption and phase noise, two current shaping structures are utilized. By using this technique, the current consumption of the circuit becomes more controllable. Therefore, by appropriate

Table 1. Various parameters related to the two proposed structures.

Parameters	VCO I	VCO II
Frequency (GHz)	2.44	2.44
V_{DD} (V)	0.8	0.8
I_{DC} (mA)	0.46	0.77
P_{DC} (mW)	0.37	0.62
PN (dBc/Hz)	-117.5 @ 1MHz -127.4 @ 3MHz	-120 @ 1MHz -130 @ 3MHz
Oscillation amplitude (mV)	360	520
Start-up time (ns)	10	5
FoM (dBc/Hz)	-189.6 @ 1MHz -190.0 @ 3MHz	-189.7 @ 1MHz -190.2 @ 3MHz

Table 2. Comparison of the two proposed structures with some VCO circuits in recent years.

Ref.	Process (nm)	Freq. (GHz)	PN (dBc/Hz)	P_{DC} (mW)	Supply (V)	Area (mm^2)	FoM (dBc/Hz)	Sim./ meas.	Noise reduct. technique
[5]	65	2.43	-111 @1MHz	0.57	0.3	0.28	-181.1 @1MHz	Meas.	Class C
[10]	180	4	-116.8 @1MHz	1	1.8	0.2	-188.9 @1MHz	Sim.	Tail current shaping
[16]	65	5.4	-113 @1MHz	8.71	0.65	0.33	-178.2 @1MHz	Meas.	N/A
[17]	65	2.47	-110 @1MHz	0.58	0.5	N/A	N/A	Meas.	Digital control
[18]	180	10	-107.8 @1MHz	1.45	1.8	N/A	-186.2 @1MHz	Sim.	Tail current shaping
[19]	180	5.28	-119.3 @1MHz	11.2	1.4	0.77	-183.2 @1MHz	Meas.	Tail current shaping
This work	65	2.44	-117.5 @1MHz -120 @1MHz	0.37 0.62	0.8	0.31	-189.6 @1MHz -189.7 @1MHz	Sim.	Dual current shaping

selection regarding current value, power dissipation and phase noise improved significantly. In this circuit, at 0.8 V as supply voltage, 0.37 mW of power dissipation is attained. Also, phase noise is achieved as –117.5 dBc/Hz and –127.4 dBc/Hz with respect to 1 MHz and 3 MHz as offset frequency, respectively. Direct biasing in NMOS tail transistors for more reduction of phase noise and increment of output oscillations was employed in the second proposed VCO. In this case, 0.62 mW as power consumption at 0.8 V as supply voltage was acquired. Moreover, at 1 MHz and 3 MHz as offset frequency, –120 dBc/Hz and –130 dBc/Hz phase noises are achieved, respectively. Output frequency and FoM for both circuits were identical, approximately equal to 2.44 GHz and –190 dBc/Hz, respectively. Both proposed circuits with equal area occupation, 0.31 mm^2, showed improved

performance in terms of power consumption and noise figure in the considered range of frequency compared to the other well-known designs. Due to the different characteristics including the range of operating frequency, low power, and small area consumption related to the two proposed architectures, they can be nominated as competent cells for IoT applications.

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