Turkish Journal of Electrical Engineering & Computer Sciences

http://journals.tubitak.gov.tr/elektrik/

Research Article

Turk J Elec Eng & Comp Sci
(2020) 28: 3402 – 3418

doi:10.3906/elk-2005-141

A new configuration for four-switch three-phase inverters based on a switched-capacitor step-up cell for electric vehicles application

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Received: 20.05.2020 • **Accepted/Published Online:** 11.09.2020 • **Final Version:** 30.11.2020

Abstract: This paper proposes a new configuration for four-switch three-phase inverters based on a step-up switched-capacitor cell, which is called switched-capacitor four-switch three-phase inverter (SCFSTPI). This converter includes eight power switches and two DC-link capacitors. Voltage step-up feature, high efficiency, integrated structure, and bidirectional power flow are the main contribution of this new configuration. A modified space vector modulation (SVM) strategy is presented to generate appropriate pulses for the converter. This modulation method also eliminates the effect of capacitors voltage imbalance problem on the inverter output voltage and current. Simulation and experimental results are presented and investigated to confirm the performance of this topology. Results validate the operation of the proposed topology and its modulation. SCFSTPI is applicable in electric vehicle (EV) drive systems and similar applications that need step-up inverters.

Key words: Switched-capacitor, three-phase inverter, space vector modulation, four-switch inverter, step-up inverter

1. Introduction

In recent years, switched-capacitor based circuits have been widely developed for electronic filters and step-up converters [1, 2]. Many switched-capacitor converters have been introduced previously, which have been reviewed by [2]. Switched-capacitor circuits can be used in either DC/DC or DC/AC converters [3–6]. Step-up switched-capacitor circuits can be employed in various applications like photovoltaic systems, energy storage devices, electric vehicles, and hybrid storage systems. In these applications, the available voltage source has a lower voltage level than the essential value [7]. Low boost factor and low efficiency in the conventional boost converter prompted to develop new design methods for step-up converters. Several methods have been proposed by articles including impedance-based converters [8, 9], switched-inductor topologies [10], and switched-capacitor based step-up converters [11]. Lee [5] presented a new switched-capacitor based inverter. This topology generates multilevel output voltage from a single voltage source by using a specific configuration of twelve power switches. Adding a switched-capacitor cell to a single-phase bridge inverter is the main concept of [5] in order to design a new step-up topology. However, requiring the high number of power switches is still a problem that increases the cost of implementation. Ye et al. [7] introduced a switched-capacitor based inverter with the same concept. It requires many power switches with floating source/emitter that increases the design complexity of gate drivers. Jahan et al. [4] presented a new switched-capacitor cell with four power switches and one capacitor. By connecting these cells together, a novel multilevel single-phase inverter has been made. A new switched-

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capacitor based inverter has been suggested by [12]. This topology consists of two parts. The first part includes a switched-capacitor network, which has been combined with a quasi-z-source boost converter. The second part is an H-bridge inverter. The output gain is controlled by the duty cycle of one power switch. The proposed converter operates in continuous current mode (CCM). However, this topology is not bidirectional, and the efficiency is 90%. A similar idea has been presented for T-type inverters by [13]. Chang and Wu [14] proposed a new single-phase inverter with some switched-capacitor based multipliers. The application of quasi-z-source networks for four-switch three-phase inverters (FSTPI) has been presented by [1]. However, the application of switched-capacitor cells for the design of step-up FSTPI is not presented before. FSTPI is the cost optimized version of the classical six-switch three-phase inverters (SSTPI). Two switching legs with four power switches and one power leg with two serial capacitors form the structure of the FSTPI. Since the number of power switches is reduced in comparison to the SSTPI, the switching and conduction losses are decreased significantly. Therefore, FSTPI affords better efficiency than SSTPI. Numerous studies have been conducted to expand the FSTPI application in AC electrical machine drive systems [15]. FSTPI has a different structure and, its modulation method is a bit different. For this purpose, advanced modulations have been proposed for FSTPIs. Amongst them, the space vector modulation (SVM) technique has attracted the most attention due to its simplicity and easy implementation by digital signal processors [16–27]. SVM is extremely adapted to machine drive algorithms [15–17, 28, 29]. The capacitor-based part of FSTPI includes two split capacitors, which one phase of the load is connected to the midpoint of them. The voltage balancing of these capacitors is the main problem because it affects the output current harmonics directly. The voltage imbalance problem maybe happened due to using the four-switch structure and low switching frequency. Some papers have tried to solve the above problem by adding some restrictions to the traditional modulation strategies [19, 20, 24, 30, 31]. As an example, Kazemlou and Zolghadri [30] introduced a different vector location detection technique to solve this issue. In [30], in each sampling interval, the amplitude and angle of active vectors are determined. Also, in each sampling interval, new regions are defined as sectors and help to select correct voltage vectors. Different switched-capacitor based DC/DC converters have been proposed until now. Nevertheless, matching a switched-capacitor based cell with the conventional inverter topologies requires accurate knowledge about the common features of them. This paper concentrates on switched-capacitor based inverters. The main contribution of this paper is to propose a new step-up inverter by combining a switched-capacitor based switching cell with a four-switch three-phase inverter. High efficiency, unified structure, bidirectional power flow, and step-up feature are obtainable by a simpler structure than the previous topologies. The simplicity means that the discussed topology has only eight power switches and two capacitors, and it does not need any other special components. The proposed topology can operate in both inverter and rectifier modes [32]. Nevertheless, this paper only focuses on the inverter operating mode of the converter. This paper also suggests a modified SVM strategy, adapted to the proposed converter, to eliminate the effect of the voltage imbalance problem of capacitors. This converter is called SCFSTPI in the following. This configuration has not been implemented before. It can be used in EV drive systems and other applications as a step-up inverter. Simulation and experiment have been done to evaluate the performance of this topology and its modulation. Results validate the performance of this topology and its modulation. This paper is organized as follows: Section 2 explains the operating principle of the proposed topology and the proposed improved SVM. Sections 3–5 represent simulation and experimental results and compares them with past works. All achievements have been summarized in Section 6.

2. Operating principle of SCFSTPI

2.1. Overview of the proposed converter and its modulation strategy

Figure 1a shows the proposed converter topology. The SC circuit (Q_1, Q_2, Q_3, Q_4, C_1, C_2, C_3) is an interface between the input voltage source and the four-switch inverter. Capacitors C_2 and C_3 are common components of both the SC stage and the four-switch inverter. An electric machine is connected to this SCFSTPI as a load. The FSTPI stage includes four power switches (S_1-S_4) and two capacitors (C_2 and C_3). The phase A is connected to the midpoint of serial capacitors C_2 and C_3. Figure 1b shows another configuration for the presented structure that the location of the low voltage source is swapped with the capacitor C_3. This displacement does not affect the operating principle of the proposed topology. In the following, the operating principle of the proposed topology is demonstrated.

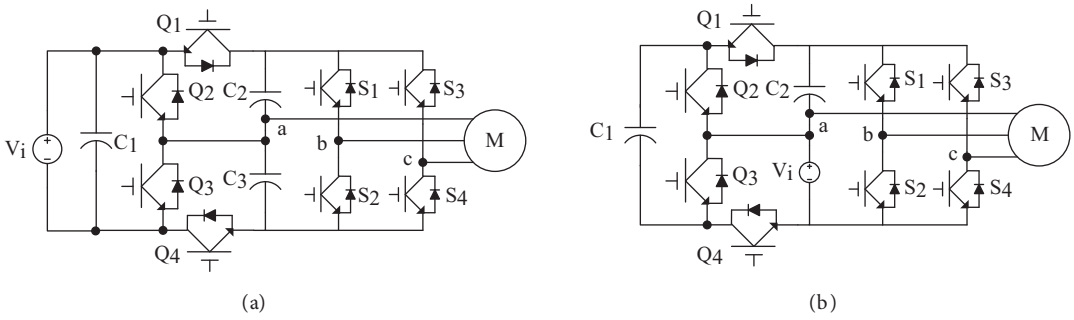

Figure 1. Circuit schematic of the proposed converter (a) first configuration, (b) second configuration.

2.2. Operating principle of the SC circuit

The SC stage incorporates four power switches and three capacitors, which produces two switching states in each switching period. Figures 2a and 2b depict two switching states. The voltage of C_1 is equal to the input voltage source. When Q_1 and Q_3 are turned on, the Q_2 and Q_4 are turned off. So, the voltages of C_1 and C_2 are identical. As shown in Figure 2a, the input current (I_i) passes through C_2. The voltage ripple of C_2 is obtained by (1). D and T_s indicate the duty cycle and the switching period of all power switches, respectively.

$$\Delta V_{C2} = \frac{I_i D T_s}{C_2} \tag{1}$$

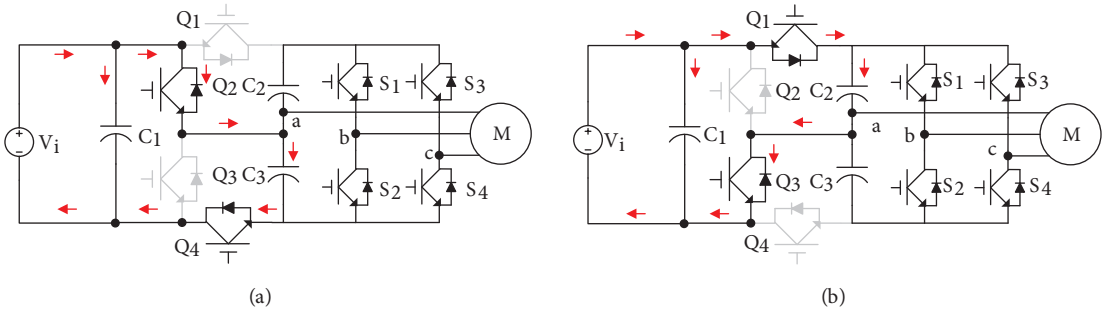

Figure 2. Switching states of SC circuit, (a) Q1 and Q3 are on, (b) Q2 and Q4 are on.

When Q_2 and Q_4 are turned on, the Q_1 and Q_3 are off. Therefore, the voltages of C_1 and C_3 are identical because they became parallel together. As illustrated in Figure 2b, the input current passes through capacitor C_3. Hence, the voltage ripple of C_3 is determined by (2).

$$\Delta V_{C3} = \frac{I_i D T_s}{C_3} \tag{2}$$

In this structure, the voltage stress on power switches is limited to the voltage of capacitor C_1, and the voltage of capacitor C_1 is equal to the input voltage. The switching frequency of the SC circuit is important parameter. It is assumed that f_{SC} indicates the switching frequency of the SC part and f_{FSTPI} is relevant to the switching frequency of FSTPI. Three possible choice exist for the SC circuit as follows: $f_{SC}=f_{FSTPI}$ and $f_{SC}>f_{FSTPI}$ and $f_{SC}<f_{FSTPI}$. The SC switching frequency should be higher than the FSTPI switching frequency to guarantee the voltage balance of C_2 and C_3. Voltages of C_2 and C_3 are constant in all conditions.The duty cycle of power switches must be 50%. Of course, if the load of one capacitor is more than another capacitor, the SC circuit cannot solve the capacitor voltage imbalance problem even with higher switching frequency. In this case, the modulation method of the FSTPI stage must solve this problem by choosing appropriate voltage vectors. All turn on and turn off actions must be equipped with dead-time. In order to summarize the operating principle of the controller, Figure 3 illustrates a block diagram. The reference voltage block in Figure 3, which has been highlighted by the blue color, can be substituted by the output reference vectors of various machine control strategies. This paper does not investigate machine control strategies because it is not the object of this paper. This study reveals that the connection of this SC circuit to FSTPI is not stable under all conditions, and this new structure requires a complementary strategy to guarantee stability. The proposed modified SVM method solves this problem.

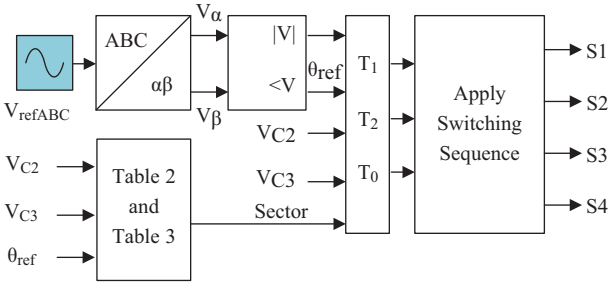

Figure 3. Control diagram of the proposed SCFSTPI.

2.3. Space vector modulation of FSTPI

Figure 4a shows the space vector diagram of FSTPI, which the phase-A is connected to the center tap of capacitors. Figure 4b depicts the space vector diagram for a condition, in which phase-B is linked to the center tap, and Figure 4c relates to a FSTPI, which phase-C is connected to the midpoint of C_2 and C_3. There are only four orthogonal voltage vectors in these three connections. However, the location of space vectors is different for these three models. The location of these vectors divides the space vector plane into four regions. The reference vector rotates inside these regions. It is possible to rebuild the reference vector with two adjacent nonzero vectors. FSTPI does not have zero voltage vectors. Table 1 identifies the amplitude and angle of each vector. In this case, it is assumed that the voltage of capacitors C_2 and C_3 are equal to V_{dc}. Table 1 is true

for capacitors voltage balance condition. Table 2 describes the dependency of those four voltage vectors on the voltage of capacitors. The angle of V_2 and V_4 is varied by the variation of V_{C2} and V_{C3}. Also, all vectors have a new amplitude when the voltages of C_2 and C_3 are changed[30]. According to the volt-second principle, the reference voltage vector can be rebuilt by two adjacent vectors in each switching interval by (3).

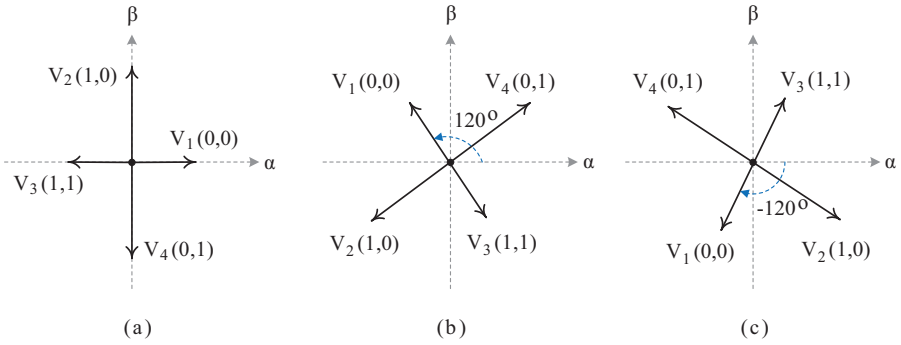

Figure 4. Space vector diagram of FSTPI (a) connection of phase-A to the center tap, (b) connection of phase-B to the center tap, (c) connection of phase-C to the center tap.

Table 1. Possible switching states for the FSTPI stage.

Vector no.	S_1	S_3	$\boldsymbol{\lvert V\rvert = \sqrt{\alpha^2+\beta^2}}$	$\boldsymbol{\measuredangle V}$
V_1	0	0	$\frac{V_{dc}}{3}$	0
V_2	1	0	$\frac{V_{dc}}{\sqrt{3}}$	$\frac{\pi}{2}$
V_3	1	1	$\frac{V_{dc}}{3}$	π
V_4	0	1	$\frac{V_{dc}}{\sqrt{3}}$	$\frac{3\pi}{2}$

Table 2. Switching states of FSTPI under the capacitor voltage imbalance.

Vector no.	**S1**	**S3**	$\boldsymbol{\lvert V\rvert = \sqrt{\alpha^2+\beta^2}}$	$\boldsymbol{\measuredangle V}$
V_1	0	0	$\frac{2V_{C3}}{3}$	0
V_2	1	0	$\sqrt{\left(\frac{V_{C3}-V_{C2}}{3}\right)^2+\left(\frac{V_{C2}+V_{C3}}{\sqrt{3}}\right)^2}$	$tan^{-1}\left(\frac{3(V_{C3}+V_{C2})}{\sqrt{3}(V_{C3}-V_{C2})}\right)$
V_3	1	1	$-\frac{2V_{C2}}{3}$	π
V_4	0	1	$\sqrt{\left(\frac{V_{C3}-V_{C2}}{3}\right)^2+\left(-\frac{V_{C2}+V_{C3}}{\sqrt{3}}\right)^2}$	$tan^{-1}\left(-\frac{3(V_{C3}+V_{C2})}{\sqrt{3}(V_{C3}-V_{C2})}\right)$

$$\begin{aligned} V_{ref}T_s &= V_1T_1 + V_2T_2 \\ T_s &= T_1 + T_2 + T_0 \end{aligned} \tag{3}$$

Switching times (T_1, T_2, T_0) are determined from (3). If the summation of T_1 and T_2 is not equal to Ts, then one semizero vector should be applied. T_0 denotes the switching time of a semizero vector. Switching times are varied in each sector.

Sector 1 Sector 1 starts from zero and limits to 90° in balance condition. However, in an imbalance mode, it places inside another region, as shown in Table 2. In an ideal situation, switching times are deduced

as follows, where m_a and θ_{ref} represent the modulation index ($\frac{|V_{ref}|}{V_{dc}}$) and the angle of the reference vector, respectively. For imbalance mode, T_1 and T_2 are changed.

$$\begin{aligned} T_1 &= 3m_aT_s\cos(\theta_{ref}) \\ T_2 &= \sqrt{3}m_aT_s\sin(\theta_{ref}) \end{aligned} \tag{4}$$

Sector 2: In Sector 2, the angle of the reference vector varies from 90° to 180°. However, for voltage imbalance condition, it differs from the ideal model, as can be seen from Table 2. In an ideal status, switching times are obtained from (5).

$$\begin{aligned} T_1 &= -3m_aT_s\cos(\theta_{ref}) \\ T_2 &= \sqrt{3}m_aT_s\sin(\theta_{ref}) \end{aligned} \tag{5}$$

Sector 3: In Sector 3, the angle of the reference vector varies from 180° to 270°. However, for voltage imbalance condition, it is different from ideal mode, as can be seen from Table 2. In an ideal situation, switching times are deduced by (6).

$$\begin{aligned} T_1 &= -3m_aT_s\cos(\theta_{ref}) \\ T_2 &= -\sqrt{3}m_aT_s\sin(\theta_{ref}) \end{aligned} \tag{6}$$

Sector 4: In Sector 4, the angle of the reference vector varies from 270° to 360°. However, for voltage imbalance condition, it is different from an ideal status, as shown in Table 2. In an ideal situation, switching times are determined from (7).

$$\begin{aligned} T_1 &= 3m_aT_s\cos(\theta_{ref}) \\ T_2 &= -\sqrt{3}m_aT_s\sin(\theta_{ref}) \end{aligned} \tag{7}$$

In order to find out the value of switching times for the non-ideal condition, it is assumed that ($V_{C2} = k\ V_{C3}\ ; 0 \le k < \infty$). So, switching times are obtained by inserting the values listed in Table 2 into (3). Hence, the following values are deduced.

Sector 1:

$$\begin{aligned} T_1 &= \left(\frac{|V_{ref}|}{2V_{C3}}\right)\left(3\cos(\theta_{ref}) - \frac{\sqrt{3}(1-k)}{1+k}\sin(\theta_{ref})\right)T_s \\ T_2 &= \frac{\sqrt{3}|V_{ref}|}{(1+k)V_{C3}}T_s\sin(\theta_{ref}) \end{aligned} \tag{8}$$

Sector 2:

$$\begin{aligned} T_1 &= \frac{\sqrt{3}|V_{ref}|}{(1+k)V_{C3}}T_s\sin(\theta_{ref}) \\ T_2 &= \left(\frac{|V_{ref}|}{2V_{C3}}\right)\left(-3\cos(\theta_{ref}) - \frac{\sqrt{3}(1-k)}{1+k}\sin(\theta_{ref})\right)T_s \end{aligned} \tag{9}$$

Sector 3:

$$T_1 = -(\frac{|V_{ref}|}{2V_{C3}}) \left(\frac{3}{k}\cos(\theta_{ref}) \ + \frac{\sqrt{3}(1-k)}{1+k}\sin(\theta_{ref}) \right) T_s$$
$$T_2 = -\frac{\sqrt{3}|V_{ref}|}{(1+k)V_{C3}} T_s \sin(\theta_{ref}) \tag{10}$$

Sector 4:

$$T_1 = -\frac{\sqrt{3}|V_{ref}|}{(1+k)V_{C3}} T_s \sin(\theta_{ref})$$
$$T_2 = (\frac{|V_{ref}|}{2V_{C3}}) \left(\frac{3}{k}\cos(\theta_{ref}) \ + \frac{\sqrt{3}(1-k)}{1+k}\sin(\theta_{ref}) \right) T_s \tag{11}$$

An essential stage in SVM is sector determination. The exact location of the reference vector is necessary. In [18], a novel method has been introduced to find the location of the reference vector. This useful method is used in sector determination. The location of basic vectors is determined by Table 2. Then, these locations are used to discovering the reference vector location. The reference vector location might be changed by the voltage of DC-link capacitors. So, it may be different for each switching period. Table 3 classifies all intervals needed for sector determination. Also, a switching pattern is required for applying selected voltage vectors. Figures 5a and 5b exhibit a pattern for applying voltage vectors. This pattern has six switching sequences, as same as SSTPI SVM. Vector V_3 has been selected as a virtual zero vector because FSTPI has no actual zero vector.

Table 3. Table of sector determination.

Reference vector angle (θ_{ref})	**Sector number**	**Reference vector angle (θ_{ref})**	**Sector number**
$0 \le \theta_{ref} < \theta_{V2}$	Sector 1	$\pi \le \theta_{ref} < \theta_{V4}$	Sector 3
$\theta_{V2} \le \theta_{ref} < \pi$	Sector 2	$\theta_{V4} \le \theta_{ref} < 2\pi$	Sector 4

3. Design method

This section covers the design method of this inverter. According to Figure 1, capacitors C_1, C_2, and C_3 should be designed based on the output power as follows:

$$\left(\frac{P_{out}}{\eta}\right)\left(\frac{1}{f_{out}}\right) = \frac{1}{2}C\ V^2 \tag{12}$$

Where f_{out} is the output frequency, and V is the DC-link voltage. Power switches Q_1, Q_2, Q_3, and Q_4 must withstand the maximum value of the input voltage. Also, they must tolerate the maximum output current. FSTPI section contains four power switches that each of them must tolerate the maximum output current and DC-link voltage. Choosing the right switching frequency is an important parameter for output harmonic rejection and efficiency. Lower switching frequencies (about 1–5 kHz) are necessary for high-power applications. The FSTPI stage operates with the mentioned switching frequency. Also, the SC circuit can be switched on/off with the same frequency as the FSTPI. Yet, to provide better dynamic response and improve the DC-link voltage ripple characteristics, it is better to choose higher switching frequency for SC stage regard to the FSTPI switching frequency. In low-power applications, the recommended switching frequency is 5 or 10 times greater than the inverter switching frequency.

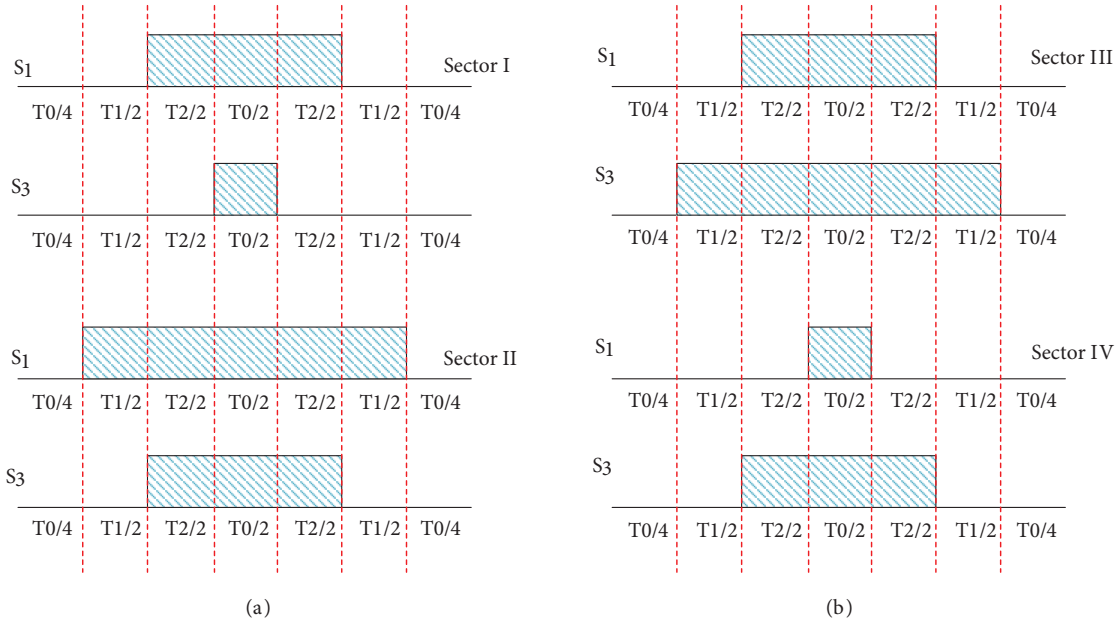

Figure 5. Switching sequences of the proposed FSTPI-SVM (a) switching strategy of Sectors 1 and 2, (b) switching strategy of Sector 3 and 4.

4. Results and analysis

The proposed converter and its theory of operation are evaluated by simulation and experimental results. Simulations have been done by MATLAB/Simulink software, and the experiments have been executed on a typical prototype that its specifications have been organized in Table 4.

Table 4. The specifications of simulation and experimental system

Parameters	**In simulation**	**In experiment**
Input voltage	150 V	150 V
Output phase current and power	5 App/350 W	5 App/350 W
Inverter switching frequency	5 kHz	5 kHz
SC circuit switching frequency	50 kHz	50 kHz
Capacitors	2200 μF	2200 μF
Power MOSFETs	-	IRFP460A
Load resistance	20 Ω	20 Ω
Load inductance	50 mH	50 mH

At first, the simulation results are investigated. Figure 6a shows the determined dwell-times according to sectors for one cycle of the output voltage. The switching period is 200 μs. So, some of T_1, T_2 and T_0 must be limited to 200 μs in each switching interval. Figure 6b shows the gate signals of S_1 and S_3, which are complementary S_2 and S_4. Figure 6c illustrates the gate signals of Q_1 and Q_2. Figures 7a–7d show the output line voltage, the output line current, the voltage of capacitors, and the current THD test result, respectively. Waveforms of Figures 7a–7d correspond to the normal operating condition, in which the capacitors C_2 and C_3

meet the same energy consumption from the load. The output voltage is equal to the reference value (300V). The output current reaches to 2.5 A in the full-load condition, and all capacitors have the same voltage value (150 V). The voltage of capacitors is equal to half of the DC-link voltage because of their serial connection. The simulation result of current THD test shows the THD is equal to 0.37%, which is lower than the IEEE519 standard value (5%). However, it is expected that this value is increased in experimental results due to adding dead-time.

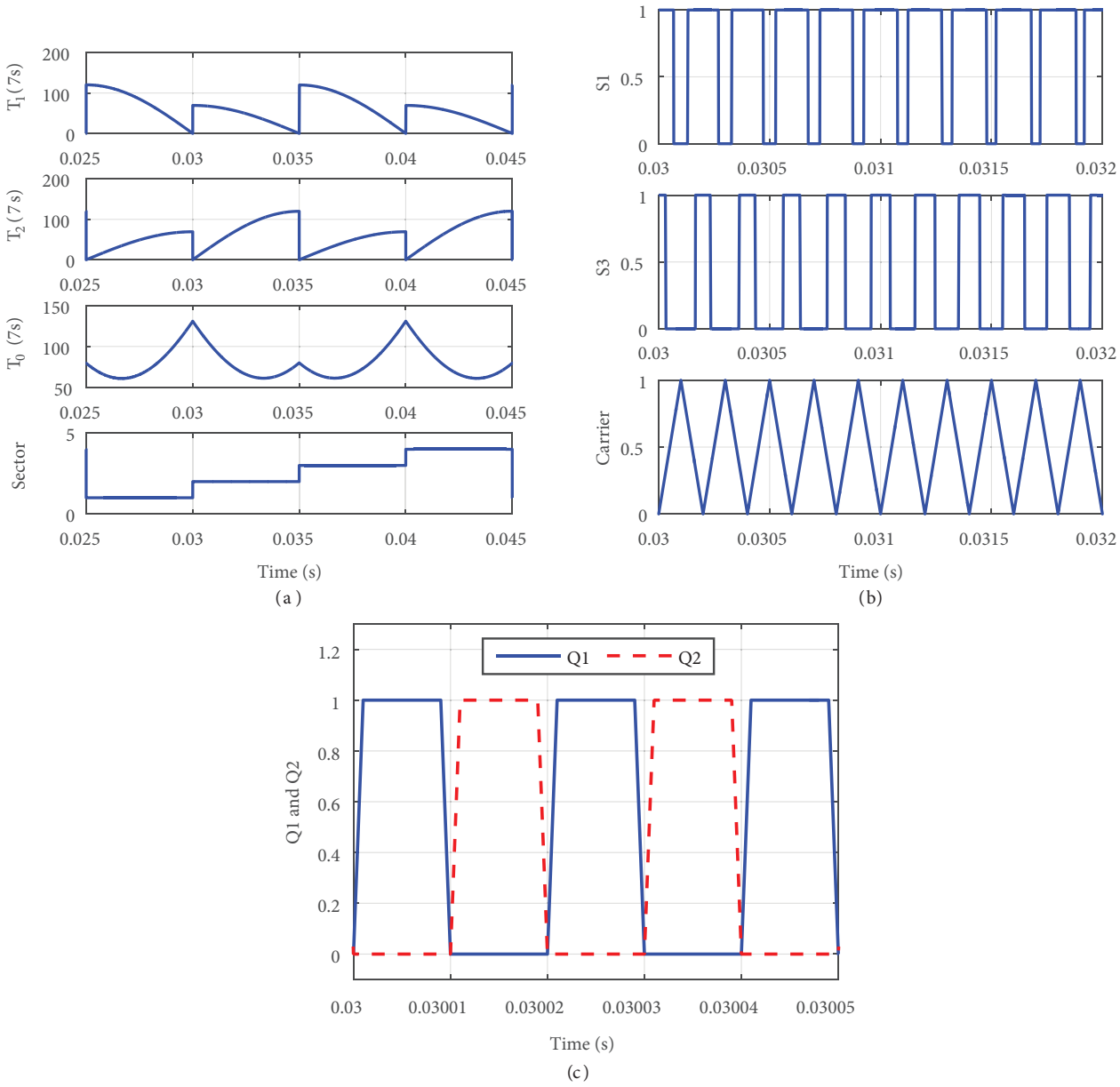

Figure 6. Waveforms of the control system (a) dwell-times for one cycle of output voltage respect to sector change, (b) command signals of S1 and S3 subject to the carrier waveform, (c) command signals for SC stage.

In the next case, the voltage imbalance condition is afforded, such that the voltage of capacitor C_2 is suddenly reduced to 138 V. This state is imposed to the capacitor C_2 by connecting an extra resistor across

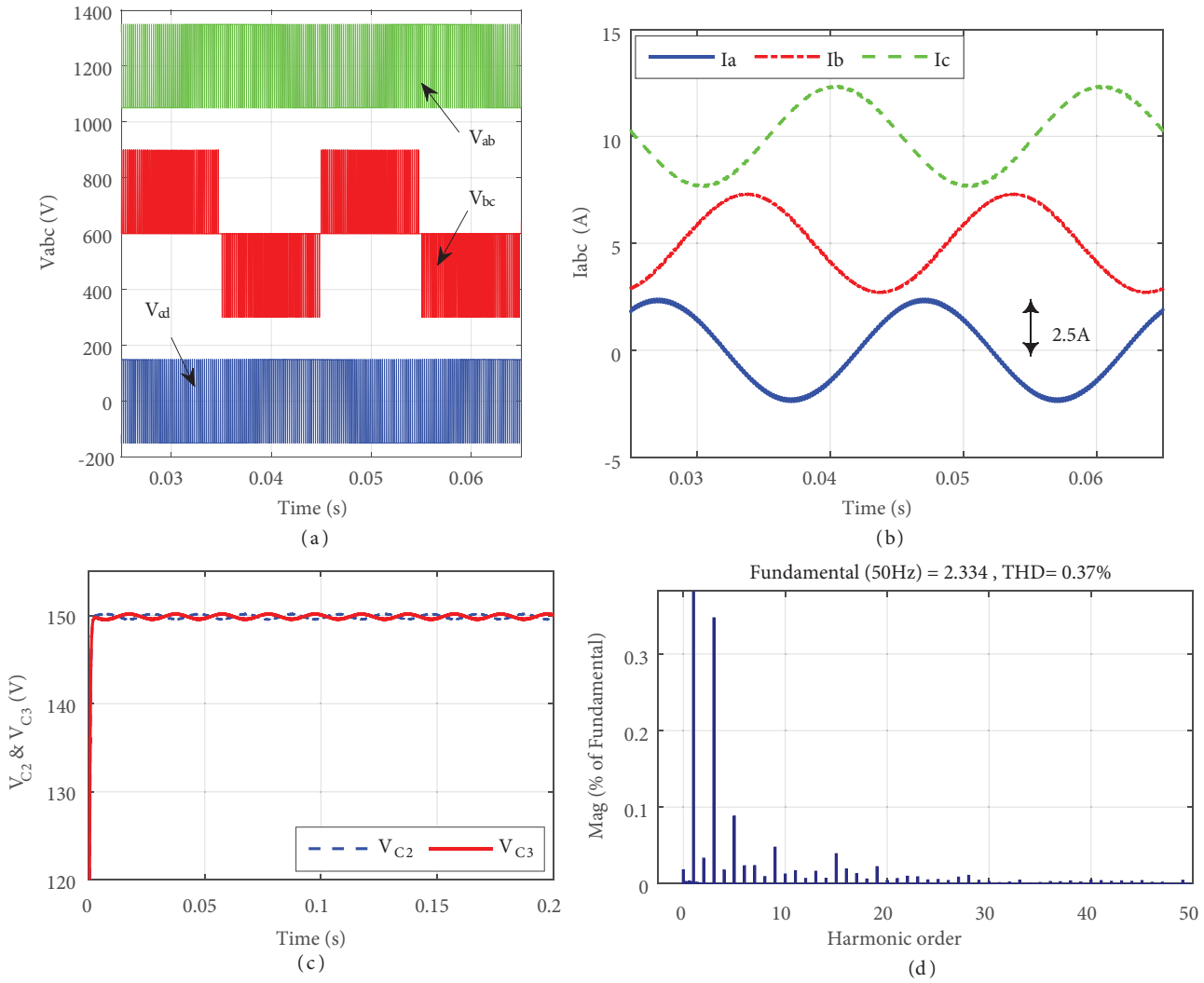

Figure 7. Waveforms of the SCFSTPI (a) output voltages, (b) output currents, (c) capacitors voltages, (d) output current THD.

it. Furthermore, no excess energy consumption is imposed to the capacitor C_3. Figure 8a shows the voltage of capacitors C_2 and C_3. The voltage imbalance condition is applied to the converter after t=0.1s, and the voltage of C_2 is reduced, as expected. Nevertheless, the line currents characteristics such as the shape and amplitude remain unchanged even after t = 0.1 s, as represented by Figure 8b. So, this result confirms that the presented SVM strategy has been worked correctly in suppressing the effect of the voltage imbalance problem on the output line voltage and current. This SVM strategy calculates the new amplitude and location of the space vectors after t=0.1s and defines new sectors based on the theory. Suitable voltage vectors are selected based on newly defined sectors.

Next, the common-mode characteristics of this converter are investigated. According to [33], common-mode voltage (CMV) and current (CMC) are measured by adding a parasitic capacitance between the load and the input power source. A 220 nF capacitor is selected based on the method mentioned in [33]. This capacitor is inserted between the neutral point of the load and the negative side of the input power supply. Based on the

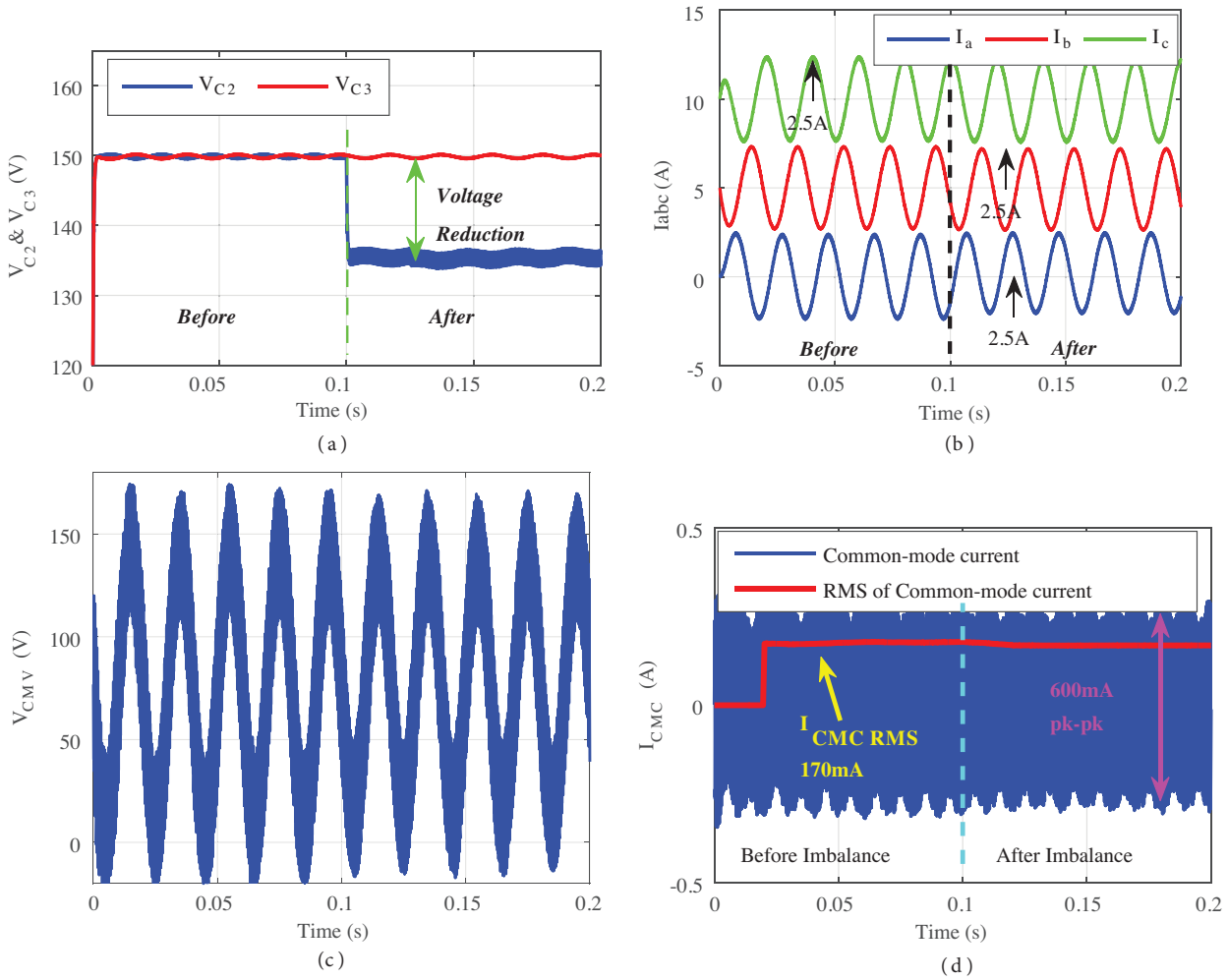

Figure 8. Key waveforms of the SCFSTPI under voltage imbalance condition (a) capacitors voltages, (b) output currents, (c) common-mode voltage, (d) common-mode current (RMS value = 170 mA).

simulation results, as shown in Figures 8c and 8d, the RMS value of the leakage current is 170 mA. After t = 0.1 s, when the voltage imbalance condition is applied to the capacitors C_2, the CMC is not affected significantly. SCFSTPI carries the power bidirectionally. If the power switches of FSTPI stage are switched off. In this mode, the reverse current flows through the body-diodes of S_1-S_4 and charges the capacitors C_2 and C_3. The switching method of the SC circuit does not need any changes. This mode is applicable for EV drive system.

Figure 9 shows the designed experimental prototype. A control board based on TMS320F28335PGFA processor generates necessary PWM signals. PWM signals are fed to two boot-strap gate drivers IR2110 [34]. A GW-INSTEK 2074 digital oscilloscope is used to capture all waveforms. Also, the setup specifications have been specified in Table 4. Figures 10a–10d show the experimental results of the SCFSTPI under the normal operating condition. Figure 10a illustrates the line voltages (V_{ab}, V_{bc}), which are similar to the Figure 7a in terms of the amplitude, shape and frequency. Figure 10b presents the line currents. Similar to the simulation results, as displayed in Figure 7b, the line currents are sinusoidal due to supplying an inductive load. Also, their amplitude and frequency are equal to 2.5 A and 50 Hz, respectively. Figure 10c represents the voltage of capacitors (C_2 and C_3). Both DC-link capacitors have the same voltage (150 V). Figure 10d shows the result

of the output current THD test. THD test results are different because parameters like dead-time have not been considered in simulations. Nevertheless, the output current THD is 2.62%, which is still lower than 5% (IEEE Std. 519).

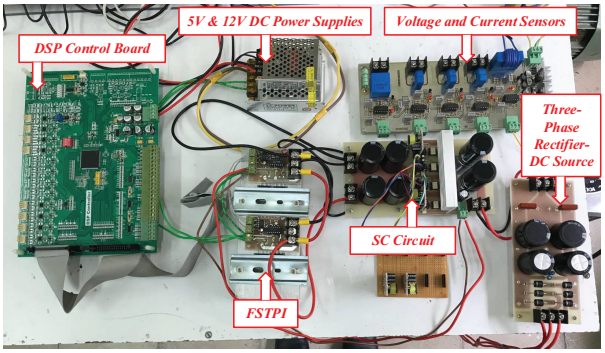

Figure 9. The experimental prototype.

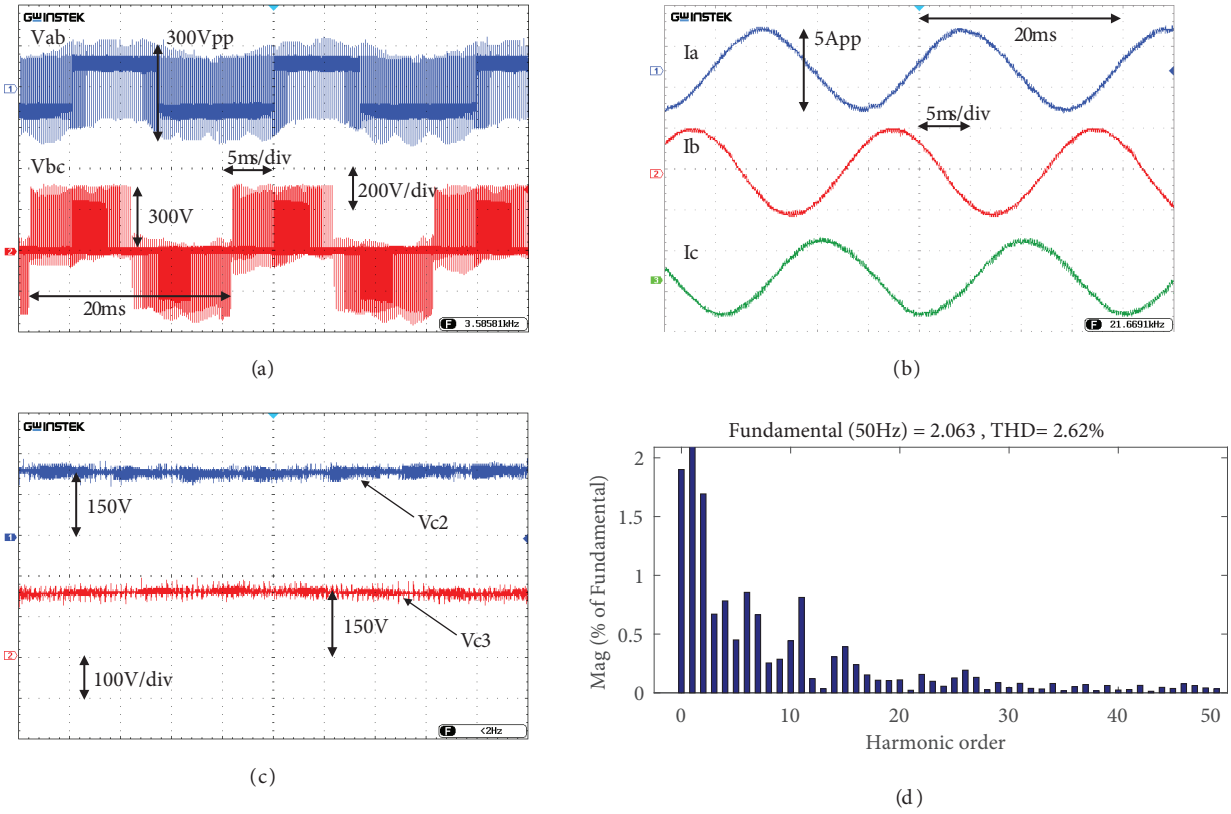

Figure 10. Waveforms of the SCFSTPI under normal condition (a) output voltages, (b) output currents, (c) capacitors voltage, (d) current THD.

Figures 11a–11d are relevant to the nonideal condition, where the voltage of DC-link capacitors is not identical. Figure 11a depicts the output line voltage for other phases. As expected, the amplitude of the line voltage is not changed after applying the imbalance condition. Figure 11b shows the line current waveforms

that the amplitude of line currents are equal to 2.5 A. Figure 11c presents the voltage of capacitors, which is not identical. Similar to the simulations (Figure 8a), one external resistor is connected across to capacitor C_2. The voltage of this capacitor is decreased to 100 V after connecting this extra load. As presented by Figures 11a and 11b, the output line voltage and currents are not affected by this event. So, the experimental result also confirms the operation of SVM in suppressing the effect of the voltage imbalance problem. Figure 11d shows the current THD analysis result. The measured experimental THD is 3.3%, which is lower than the standard value (5%).

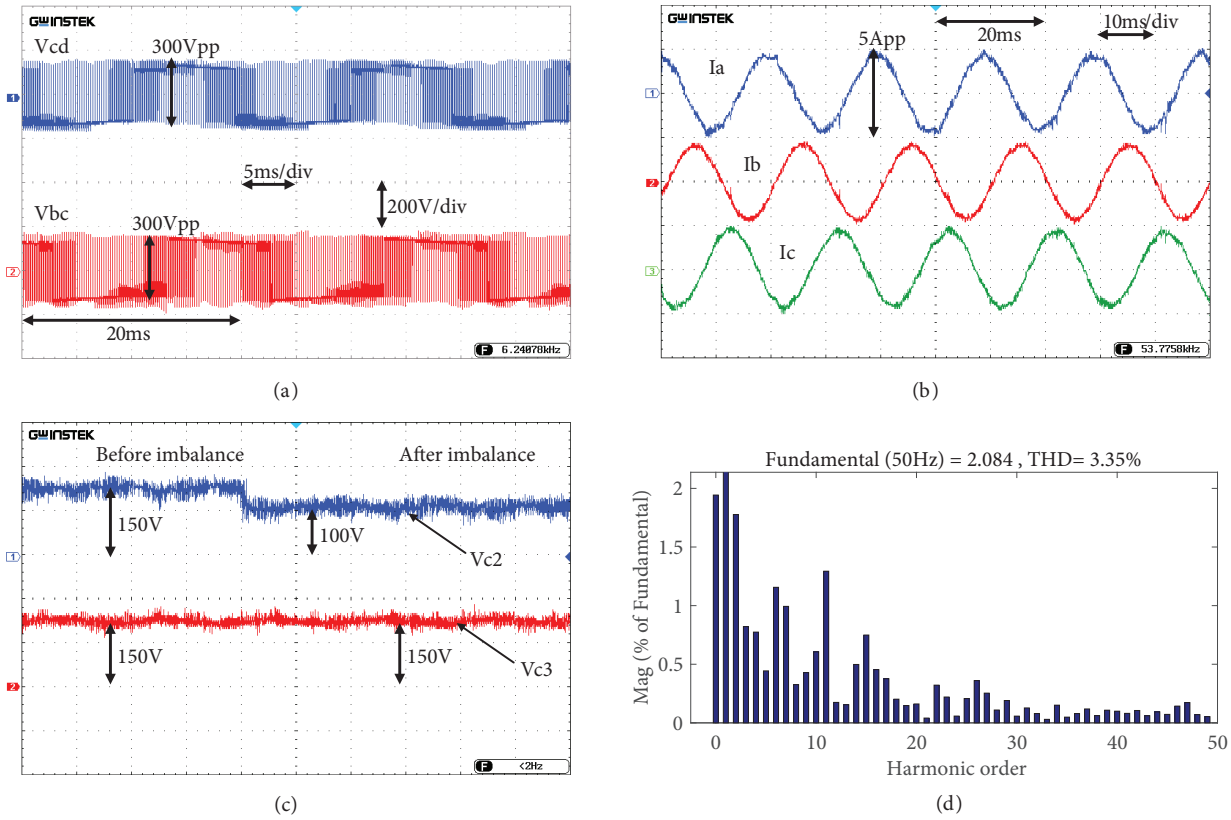

Figure 11. Key waveforms of the SCFSTPI under the voltage imbalance problem (a) output voltages, (b) output currents, (c) capacitors voltage, (d) current THD.

Another parameter is the CMC, which can make different faults in a system. Figure 12a illustrates the test circuit, designed according to [33]. One 220 nF nonpolarized capacitor has been chosen as $C_{Parasitic}$, similar to the simulation. The current passing through this capacitor is measured by LEM LA-55 current sensor. Figure 12b shows the CMC waveform. The RMS value of the CMC is 164 mA, and it is 45% smaller than the standard value that mentioned in [33] (300 mA). Figure 13a displays the efficiency test result. The measured efficiency under the full-load condition is equal to 94%. Also, the loss distribution curve has been presented by Figure 13b, which shows the sum of switching and conduction losses for different output loads in SC and FSTPI circuits. The conduction loss is reduced in lower output currents. So, efficiency is improved. The switching loss is approximately constant in all conditions. The converter efficiency is obtained by using $P_{O_{ac}}/P_{i_{dc}}$, which $P_{O_{ac}}$ is equal to $V_{O_{rms}}I_{O_{rms}}$ and $P_{i_{dc}}$ can be obtained from $V_{i_{dc}}I_{i_{dc}}$.

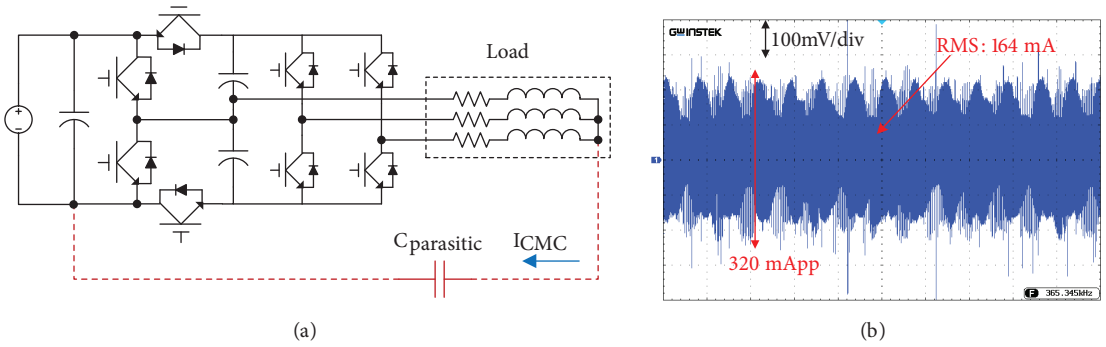

Figure 12. Common-mode current (a) circuit model for test, (b) common-mode current waveform.

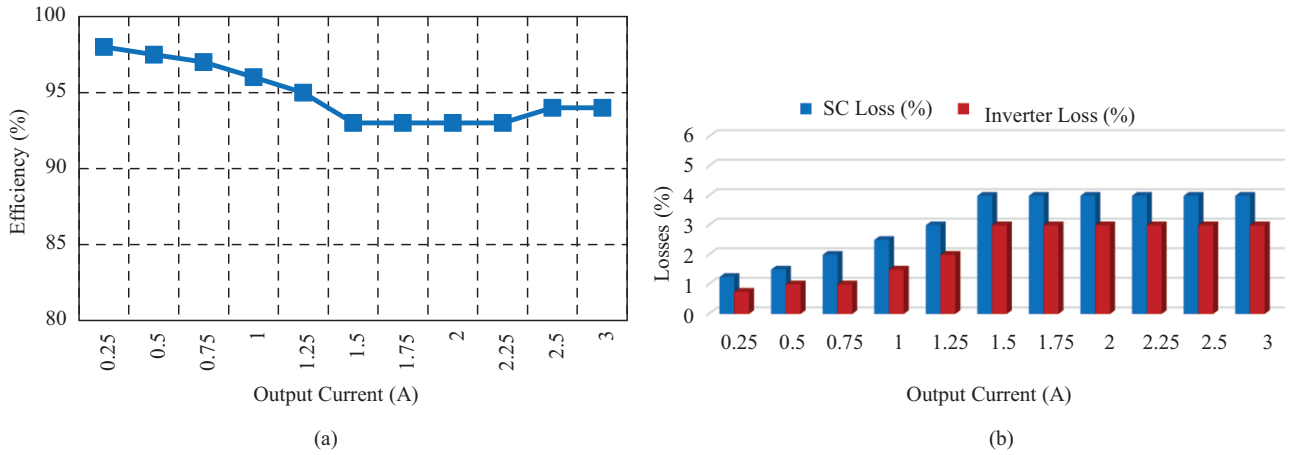

Figure 13. Efficiency analysis (a) overall efficiency curve vs. output current in experiments, (b) each stage losses vs. output current.

5. Comparative study

Table 5 compares the proposed inverter with a conventional FSTPI, a switched-capacitor based inverter [12, 35], and some non-SC-based FSTPI. Nguyen et al. [12] suggests a single-phase SC-based step-up inverter. However, in three-phase mode, it requires enormous numbers of switches than proposed SCFSTPI. A minimum loss topology with a soft-switching method has been introduced by [35]. The input stage of the converter in [35] provides conditions for zero-voltage and zero-current switching. So, it improves efficiency. However, using magnetic elements increases the cost. A z-source FSTPI has been introduced in [36]. The proposed structure only requires four power switches. Although the impedance source-based inverters can tolerate the shoot-through states, such networks have low efficiency. Power diodes add reverse-recovery loss to the converter overall losses. In the proposed topology, there are no power diodes. As a result, this converter has better efficiency if compared with other converters, even with a higher number of power switches.

6. Conclusion

A new configuration for step-up inverters has been presented in this paper that is called SCFSTPI. This topology includes eight power switches and two DC-Link capacitors, which is never implemented before. A battery or other suitable storage system can be connected to the input port of SCFSTPI. As a result, it is

Table 5. Comparison between the SCFSTPI and previous converters.

Topology	Switches	Diodes	Caps.	Inductors	Step-up	η	Bidir.	Imbalance rej.
Proposed	8	0	3	0	√	94%	√	√
Ref. [28]	4	0	2	0	×	95%	√	×
Ref. [12]	5	3	2	1	√	90%	×	×
Ref. [36]	7	1	1	2	×	94%	×	×
Ref. [37]	4	2	2	2	√	91%	√	×

appropriate for EV propulsion systems. An optimized space vector modulation strategy has been implemented to resolve the effect of the capacitor's voltage imbalance problem on the inverter output voltage and current. The suggested SCFSTPI provides high efficiency, seamlessly structure, bidirectional power flow, step-up of voltage, and control-compatible topology, as can be seen in results. Simulation and experimental results validate the proposed structure. The efficiency curve shows that this converter provides uniform efficiency in different loads. Furthermore, the proposed topology improves past efforts according to the comparative analysis.

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