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A step-down isolated three-phase IGBT boost PFC rectifier using a novel control algorithm with a novel start-up method

Hüseyin KÖSE*, **M. Timur AYDEMİR**
Department of Electrical and Electronics Engineering, Gazi University, Ankara, Turkey

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Abstract: For some industrial converter applications such as battery chargers, a DC/DC converter is needed to step down the high DC (direct current) voltages generated by PWM (pulse with modulated) rectifiers to lower voltage levels such as 110V/220V. These both complicate the design and decrease the efficiency. In this paper, a novel topology that includes a step-down transformer and a novel control algorithm is proposed. The proposed current, which is synchronized, look-up table based, sinusoidal PWM control method (CS-LUT-SPWM method) using switching frequency-oriented synchronization (SWFOS) results in a very fast PWM generation and stable operation. Finally, a new thyristor-based start-up circuit providing safe operation when there is energy black out is proposed. A 32-kW converter has been designed, built, and tested to prove the concepts. The proposed converter has an efficiency higher than 94%, an input current total harmonic distortion (THDi) less than 5%, and a power factor closer to 0.99. Theoretical calculations and experimented results show that proposed converter has better efficiency (94%–96%) compared to classical PWM boost rectifiers with a series DC/DC converter topology (92%) in the literature. Fast PWM control algorithm, less complexity, low switching noises, one-stage conversion circuit, and novel start-up circuit are other advantages of the proposed converter.

Key words: Start-up of boost rectifier, six switch boost rectifier, current synchronized look-up table based control method, isolated boost rectifier

1. Introduction

Active three-phase power factor corrected (PFC) rectifiers are used to generate high quality DC (direct current) voltage from AC (alternating current) line voltages with excellent power quality performance. Thanks to high frequency switching (generally above 20 kHz), they can achieve better input current total harmonic distortion (THDi) and better input power factor compared to traditional diode and thyristor rectifiers. IEEE Std. 519-2014 [1] describes the voltage and current harmonic limits in power systems and, [2] explains its application and some confusing situations that practicing engineers may come across. Active three-phase PFC rectifiers can provide input current THDi less than 5% and power factor (PF) greater than 0.99 at rated power and thus, can easily meet the requirements of IEE Std 519-1992 [3, 4]. Among the three phase PFC rectifier topologies, bidirectional six-switch PFC rectifier and VIENNA rectifier topology draw more attention in industrial applications due to their lower complexity and low-component stresses [3]. Active three-phase six-switch PFC boost rectifier topology has less switching components and simpler design, and that is why it is of interest for this work.

*Correspondence: huso481@gmail.com

There is a necessity of ohmic isolation between the load and the grid in some high-power applications. In such cases, usually a two-stage power processing unit composed of a front-end six-switch buck or boost rectifier cascaded with an isolated DC/DC converter is used. As a different solution, single-stage high-frequency isolated three-phase AC/DC converter topology is proposed in [5]. Another topology is three-phase PFC rectifier using two single-phase PFC rectifiers with a scott-type transformer [6]. However, they suffer from complexity and high-number of switching components.

There are several papers on control methods of active three-phase six-switch boost PFC rectifier. One study [7] compares five DSP based average current control methods for three-phase six-switch boost PFC rectifiers. Complex algorithms and long mathematical calculations are used to define PWM values. The control method that yields the shortest time was claimed to be the average-current control with three independent controllers. However, 17.6 µs digital signal processor (DSP) calculation time reported in the paper is still long. Another study compares performances of three-step and six-step PWM control in six-switch PFC boost rectifier [8]. It was concluded that the performance of three-step PWM was superior especially at light loads.

Recently, some control studies have been proposed to minimize voltage and current sensors of six switch boost PFC rectifiers. Input voltage sensorless duty compensation control method using two input current sensors and one output DC voltage sensor to estimate input ac voltages and PWM sectors is proposed in [9]. A control strategy using a single high frequency shunt current sensor at the DC side and three input voltage sensors at the AC side to estimate the AC line currents and PWM sectors is suggested in [10].Simple control algorithms for active three-phase rectifiers to minimize current THDi value and output voltage ripple have been proposed in [13–15]. [13] proposes direct power control (DPC) method based on a predefined look-up table (LUT) that can achieve lower THDi values but has higher output voltage ripple. [14] uses model predictive control (MPC) to achieve lower THDi with lower dc voltage ripple. [15] proposes modification on one cycle control (OCC) for a better performance.

Regardless of the control method used, due to the anti-parallel diodes of IGBTs in the topology, there is a start-up problem when ac input comes back after a black-out because of short-circuit behavior of the DC filter capacitor at the output. Thus, the start-up of the circuit has to be controlled to protect the IGBTs, fast fuses and output capacitor from high inrush currents. Unfortunately, there are few papers about the start-up control of three-phase PFC rectifiers. In [16], it is shown that the current spike during start-up can be reduced if duty-cycle feedforward is employed. In [17], a three-step start-up procedure using series resistors and relays was proposed as a solution, but the full-load start-up problem was not evaluated in the study. In reality, extreme inrush currents occur in the start-up at full-load output with a full-discharged capacitor. In [18], start-up techniques of three phase AC/DC PWM converters with diode rectifiers under full-load in DC distribution systems were presented to overcome full-load start-up problem, using serial resistors and an external diode rectifier to pre-charge the bulk capacitors. However, the requirement of high-power rated resistors makes it difficult to use this method for high power applications. A proper high-power resistor should be used for each different power level the converter is designed. Also, resistors and contactors present a reliability problem due to transients, arcs and noises. Furthermore, three contactors are needed for three control circuits. Finally, if the line voltages and frequencies vary, using a resistor to charge the output capacitor at full load may not provide a stable solution at start-ups.

This paper proposes a step-down isolated active three-phase six-switch PFC boost converter, operating with a fast PWM algorithm. Also, a new start-up topology is presented.

Traditionally, the PWM rectifiers have bus voltages in 850–900 V range. If the application is intended for

low voltages such as 110V/220V, this requires the use of another DC-DC converter, resulting in a complicated structures and lower efficiency. In this paper, the bus voltage is reduced by using a step-down transformer. A current synchronized, look-up table based, sinusoidal PWM (CS-LUT-SPWM) control method using switching frequency-oriented synchronization (SWFOS) is also proposed to control the converter. The SWFOS technique results in a very fast PWM generation. In literature [7], the best PWM calculation time is 17.6 µs between three DSP control methods. However, proposed SWFOS algorithm can calculate PWM values in nanoseconds. The less PWM calculation time is, the less complexity of microprocessor unit in terms of clock frequency, ADC sampling frequency, operating frequency. Finally, a novel start-up technique has been proposed for industrial AC/DC rectifier applications. This thyristor-based circuit utilizes a novel switching algorithm to overcome the start-up problems faced in active six-switch PFC rectifier topology.

Both the start-up circuit and the PWM algorithm have less complexity compared to the existing ones [16–18]. The proposed structure utilizes voltage and current sensors at the output and input sides. In order to explain the proposed method, a 32 kW three-phase PFC rectifier with a low frequency step-down input isolation transformer was built and tested. The proposed CS-LUT-SPWM control method was implemented and very low PWM calculation times in nanoseconds were realized. The control methods, block diagrams, flowcharts, design calculations, and experimental results of the proposed structure are presented in this paper.

The paper is organized as follows: Section II describes the proposed converter and the control algorithms. The efficiency analysis and loss considerations are performed in Section III. The design process and the implementation of the proposed converter are explained in Section IV. Section V presents the experimental results.

2. Proposed converter circuit and control algorithms

Figure 1 shows the proposed isolated IGBT (insulated gate bipolar transistor) rectifier with the start-up and control circuits. T1 and T2 are thyristors for soft charging of output capacitors during start-up. Three phase delta-delta connected galvanic isolation transformer can be seen after thyristor blocks. Lf is the low frequency filter. L1, L2, and L3 are the high frequency inductors to get low-THD currents. Q1-Q6 switches are IGBT bridge for PWM rectifier. Thanks to the availability of high-quality input sensing devices and software ability, it is possible to design an IGBT rectifier without neutral connection. Line-to-line input voltages and their zero-cross signals are sensed by a microprocessor to drive the gates of the thyristors and IGBTs. These signals are used to synchronize the current and the voltage so that power factor correction can be made. Output DC voltage and DC current are sensed and fed-back for constant-current constant-voltage battery charging circuits. It means that the proposed converter can be used as a battery charger or a DC power supply. The proposed topology is applicable in all power ranges and all DC levels by using a properly rated input transformer, high frequency inductors, and IGBTs.

2.1. Proposed CS-LUT-SPWM control method

Figure 2 shows the block diagram of the proposed current synchronized look-up table sinusoidal-PWM (CS-LUT-SPWM) control method. Lookup table method is a simple control method [11, 12]. One cycle control method (OCC), direct power control method (DPC), and model predictive control method (MPC) have been suggested to be useful for active three-phase AC/DC converters [13–15]. It requires basic microprocessor calculations to define PWM duty cycles in each switching period, thanks to predefined PWM values in the look-up table. However, input current harmonic distortion has been an increasing problem when the line frequency varies

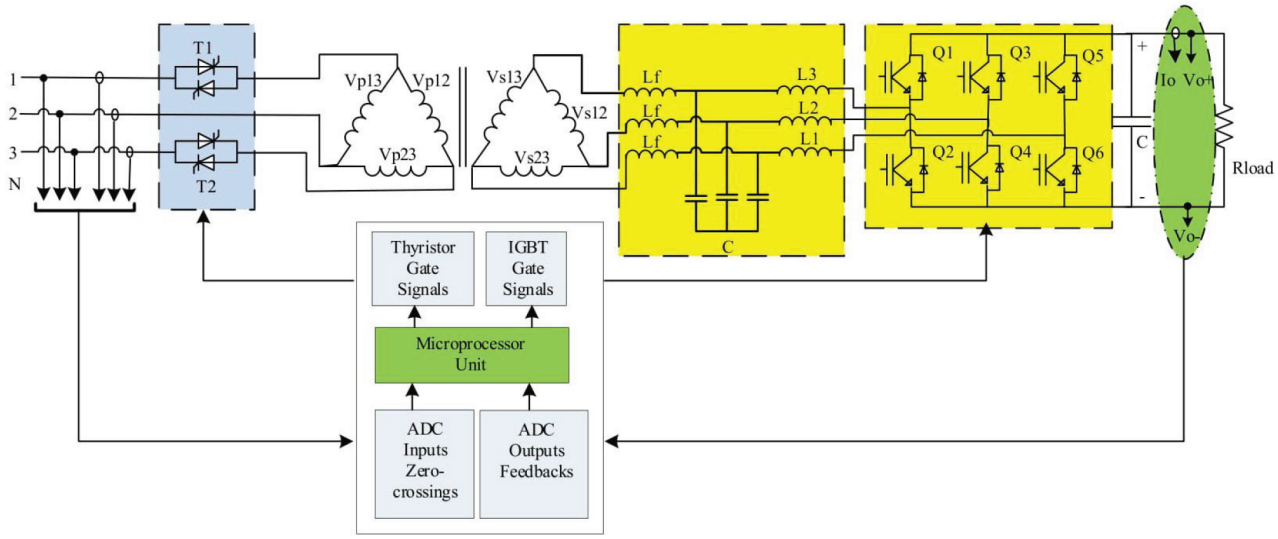


Figure 1. Proposed active three-phase boost rectifier with novel start-up and control circuit.

(oscillates) even in acceptable limits, for example 50 Hz ±5%. Because the predefined look-up table (LUT) includes predefined PWM values and PWM counts, these methods suffer from higher current THDi values and unstable line frequencies.

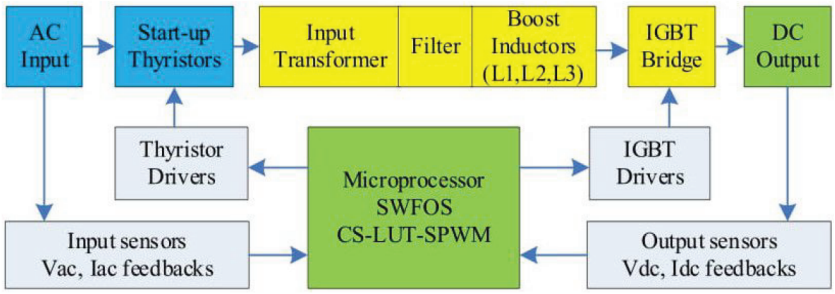


Figure 2. Control block diagram of proposed converter.

Proposed CS-LUT-SPWM control method overcomes this problem using the proposed switching frequency oriented synchronization (SWFOS) method. In order to use just one LUT in the software with oscillating line frequency in a narrowband, switching frequency is also changed in a narrowband to be able to get constant PWM counts in one line period. To get constant PWM counts in one period, switching frequency can be increased at higher line frequencies and can be decreased at lower line frequencies. When the line frequency of IGBT rectifier is sliding slowly in a narrowband (Fline = 50 Hz ±5%), switching frequency is also let to slide slowly in the same band (Fsw = 16 kHz ±5%). Not only the switching frequency, but also the sampling frequency of the microprocessor is changed in a narrowband (62.5 uS ±5%) to be able to get equal sampling of ADC values and zero crossing counts in one period. As a result of using the same sampling counts and same PWM counts in one period, the proposed control method achieves the same performance, operating at the same THDi values and the same power factor even when the line frequency varies.

Equations (1)–(9) establish the fast mathematical background of the proposed control method. These basic calculations show how to get each of six pwm register value in each switching period and how to get switching frequency from line frequency. In these equations, LUT[ ] is a predefined look-up table, which includes per unit (p.u.) sinusoidal PWM integer register values for microprocessor PWM unit. The "$\gg$" sign in the equations means shifting the quantity on the left by the amount shown on the right. G1, G3, and G5 are PWM register values to drive Q1, Q3, Q5. Operator ($\pm$) in the equations (2)-(4) means positive (+) and negative (–) cycles in PWM register value calculations. Low side IGBT gate signals (G2, G4, G6) are complementary of G1, G3, G5 with predefined dead-time value. DUTY is the duty cycle of one-cycle sinusoidal PWM (SPWM). (8) shows the division process, which avoids floating division to generate a PWM between 0 and 1. The number is multiplied by a number between 0 and 256, and the result is shifted 8 bits to the right. 0.5 x Dm means halving the PWM period register value. It is done by shifting the calculated value one bit as shown in (7). Dm is variable in this method because of variable switching frequency. K1, K2, K3 are indexes of the predefined LUT at the operating point. They were used to get 120-degree phase shifted LUT-PWM values. Tk is a constant which shows PWM counts in one cycle of the AC voltage. It can be calculated as 320 at 50 Hz with 16 kHz switching frequency. Fsw is the switching frequency of IGBTs. It is constant in one cycle but varies in a bandwidth ($\pm$5%) with a slew rate. Because Tk is 320, the band in which Fsw may change is calculated as 15.2–16.8 kHz when the line frequency (Fline) varies in 47.5–52.5 Hz band using (9).

$$LUT[] = \{T0, T1, T2, , Tk\} \tag{1}$$

$$G1 = 0.5 \times Dm \pm LUT[K1] \times DUTY \tag{2}$$

$$G3 = 0.5 \times Dm \pm LUT[K2] \times DUTY \tag{3}$$

$$G5 = 0.5 \times Dm \pm LUT[K3] \times DUTY \tag{4}$$

$$K2 = K1 + \frac{Tk}{3};\ if K2 > Tk,\ K2 = K2 - Tk \tag{5}$$

$$K3 = K1 + \frac{Tk \times 2}{3};\ if K3 > Tk,\ K3 = K3 - Tk \tag{6}$$

$$0.5 \times Dm = Dm \gg 1 \tag{7}$$

$$LUT[K1] \times DUTY(0-1) = (LUT[K1] \times DUTY(0-255)) \gg 8 \tag{8}$$

$$Tk = \frac{Fsw}{Fline} \tag{9}$$

Microprocessor (dsPIC) calculates the PWM values very fast, because it requires predefined PWM values, integer adding, subtraction, multiplying, and shift commands from equations (1)-(9). There is no floating point, trigonometric or hard-subroutine required mathematical calculations. Eventually, the proposed algorithm includes only two predefined look-up table (LUT) in the software; one is 50 Hz LUT to operate in 50 Hz $\pm$5% frequencies, and the other is 60 Hz LUT to operate in 60 Hz $\pm$5% frequencies.

In order to achieve power factor correction in different power levels from 0% to 100%, current synchronization (CS) algorithm was applied to synchronize the input current and voltage. Because of the voltage drops on the boost inductors, there is a synchronization angle between the input line-neutral voltage and the current at higher current levels. Therefore, the current synchronization algorithm should be used to generate the PWM signals so that the unity power factor can be achieved.

2.2. Proposed start-up control method

The proposed circuit includes two back-to-back thyristor modules rated at the input current and a simple triggering circuit with a simple firing algorithm. In contrast to the series resistor solution, this circuit is applicable in different designs using different thyristor modules rated for different voltages and currents and provides a stable solution. The start-up thyristors are placed on two-lines only and initially only when the thyristors in the first block are fired. As a result, the equivalent circuit shown in Figure 3(a) can be used to represent the start-up operation. When the thyristors T1 or T2 are fired, line-to-line voltage is applied to the primary of the transformer, and at the secondary side the current flows through line inductors (L1 and L2, thus 2L) and two diodes (D1 and D4, thus 2D). The firing procedure is depicted in Figure 3(b) during the start-up between time instants called t0 and t3. During the time interval [t0–t1], T1 thyristor block is triggered with a firing angle advanced in time from 180° towards 0°. During the time interval [t1–t2], both T1 and T2 thyristor blocks are triggered with full firing angle (0°). During the time interval[t2–t3], IGBT gates are applied with a soft-starting duty cyle. After t3, the circuit reaches the steady-state. There is a soft starting algorithm applied to circuit after each blackout of the AC input or switch off/on. This algorithm is presented in Figure 4.

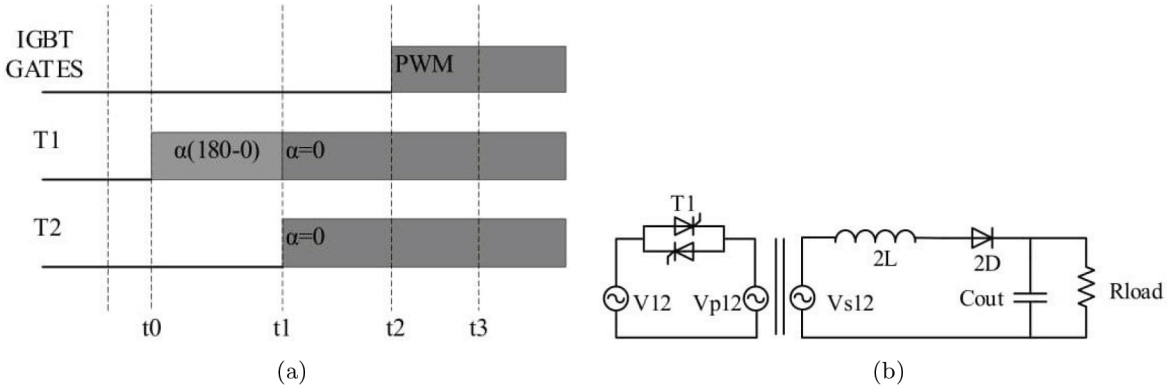


Figure 3. (a) Start-up triggering procedure of proposed converter, (b)Start-up circuit model of proposed converter.

3. Efficiency and power loss considerations

3.1. Start-up circuit losses

The proposed converter has two thyristor modules at the input side of the converter. Since it is placed in the "high-voltage, low-current" side of the transformer, thyristor conduction losses are low. These losses (P(l-su)) depend on the input line current (Is), the number of thyristor modules (NTh), the forward voltage drop (Vf)

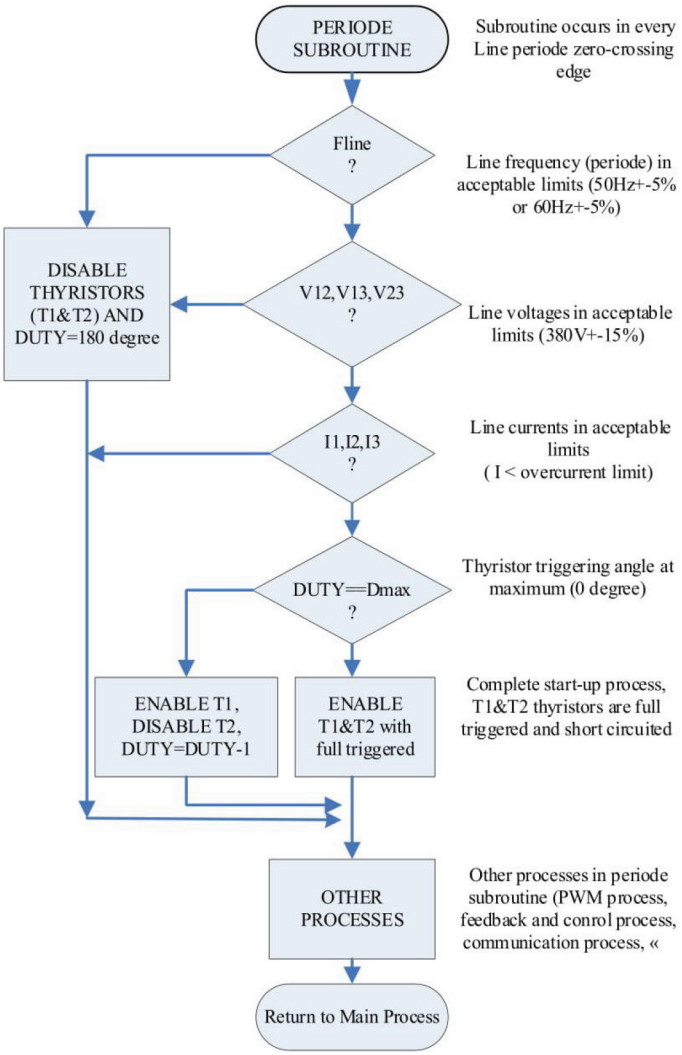


Figure 4. Start-up software algorithm of the proposed converter.

of the thyristors.

$$P(l-su) = NTh \times Vf \times Is \tag{10}$$

The efficiency loss caused by the start-up circuit with respect to the converter input power ($\eta(loss-su)$) can be defined as

$$\eta(loss-su) = \frac{P(l-su)}{Pin} \tag{11}$$

Where Pin is input active power of converter and PF is power factor;

$$Pin = \sqrt{3} \times V12 \times Is \times PF \tag{12}$$

For a 380 V line-to-line voltage (V12) and two thyristor modules (NTh = 2) having a voltage drop of 1 V on each module, efficiency loss caused from the proposed start-up circuit can be calculated as 0.3%.

3.2. Low frequency ısolation transformer losses

Transformer losses (Ptr) are defined as follows:

$$Ptr = Pcore + Pcu \tag{13}$$

Although the equation includes the core losses (Pcore) too, copper losses (Pcu) constitute the largest part at low frequencies, and therefore, the core losses will not be considered here.

Copper losses of the transformer can be calculated by using (14), where Rw is the winding resistance of the primary. It is assumed that the losses on both sides are equal.

$$Pcu = 2 \times (3 \times Is^2 \times Rw) \tag{14}$$

Efficiency loss is expected to be around 1% in a well-designed power transformer [21]. For the proposed design, extra efficiency losses caused from transformer can be expected as 1%.

$$\eta(loss - Tr) = \frac{Pcu}{Pin} \tag{15}$$

$$\eta(loss - Tr) = \frac{(6 \times Is^2 \times Rw)}{(\sqrt{3} \times V12 \times Is \times PF)} \times 100\% = \frac{(6 \times Is \times Rw)}{(\sqrt{3} \times V12 \times PF)} \times 100\% \tag{16}$$

3.3. Boost inductor losses

The losses of the boost inductor (Pind) are defined in (17). It includes the copper losses (P(cu-L)) and core losses (P(core-L)).

$$Pind = P(cu - L) + P(core - L) \tag{17}$$

Again, the copper losses are the most dominant part, and the core losses can be ignored. Copper losses for the three boost inductors are given in (18) where IL means the inductor current.

$$P(cu - L) = 3 \times IL^2 \times R(W - L) \tag{18}$$

For the proposed design, efficiency losses of the inductors ($\eta(loss - L)$) can be calculated as 0.6% using equation (19), with the designed inductor [20] (12 blocks of magnetics large kool-Mu (00K4741B026), 60 turns with 68 = 48 mm2 copper-wire, 150 mm average one-turn length, 60150 = 9 m total length is, R(W-L) = 3mΩ).

$$\eta(loss - L) = \frac{3 \times IL \times R(W - L)}{\sqrt{3} \times V12 \times PF} \times 100\% \tag{19}$$

Due to square-root relationship between the inductor value (L) and inductor turn number (N), it can be obtained that the wiring resistance of inductor (R(W-L)) is in relation with square root of transformer turn ratio ($\sqrt{n}$). Because IL is in relation with n(transformer turn ratio), $\eta(loss - L)$ is in relation with $n^(3/2)$

from equation (19). So that η(loss-L) can be obtained nearly $n^(3/2)$ times greater comparing to conventional topology in the same power. Extra efficiency losses on inductors (η(loss-L$\triangle$)%) caused from the step down transformer high secondary current can be evaluated as 0.5% using equation (20).

$$\eta(loss - L\triangle)\% = (n\sqrt{n} - 1)/(n\sqrt{n}) \times nloss(L)\% \tag{20}$$

3.4. IGBT converter losses

IGBT losses in the six-switch converter circuit (PIGBT) can be estimated by using (21)–(23). A more precise calculation is possible to use the method described in [19]. IGBT losses include the conduction and switching losses. Because of the high secondary currents of the proposed converter, conduction losses (Pcond) are expected to be higher than the conventional topology at the same power. On the other hand, the switching losses (Psw) are expected to be around the same as the conventional topology because the dc bus voltage goes down while the IGBT current goes up, keeping the VDC × IL almost constant.

$$PIGBT = Pcond + Psw \tag{21}$$

$$Pcond = kc \times f[V(IGBT), V(diode)] \times Irms(L1) \tag{22}$$

$$Psw = VDC \times IL \times Fsw \times kf \tag{23}$$

The IGBT power loss difference (P(loss-$\triangle$)) between the proposed circuit (P.C.) and the conventional circuit (C.C.)can be presented as the difference between conduction losses only, due to expectation of the same switching losses. Extra efficiency losses on IGBT circuit caused from the proposed topology comparing to conventional topology can be calculated as n times as much as the conventional circuit using equation (21)-(25), where V(IGBT) is the voltage drop on an IGBT (VCE), V(diode) is the voltage drop on a diode, kc, and kf are the ratios in the formula, IL is 150 A for the proposed circuit an 50 A for the conventional circuit (150/n), Pin is 32 kW. Thus, if the efficiency loss in the conventional IGBT circuit is 1%, efficiency loss in the proposed converter IGBT circuit is expected to be around 3%. As a result, extra efficiency losses on IGBT circuit (η(loss-igbt$\triangle$)%) caused from the proposed topology is expected as 2%.

$$P(loss - \triangle) = Ploss(P.C.) - Ploss(C.C.) \tag{24}$$

$$\eta(loss - igbt\triangle)\% = (Ploss(\triangle)/Pin) \times 100\% \tag{25}$$

3.5. Consideration of the conventional topology with DC/DC converter

Active six switch buck type PFC rectifier topology requires six additional fast diodes [3, 4]. In high-current application, (for example >100 A), this is not an applicable solution. Thus, to be able to design an active three-phase PFC boost rectifier not requiring input neutral connection and having input 380 V AC and output 250 V DC, there is a necessity of high frequency DC/DC converter in the output of active rectifier bridge to convert 750–900 V to 250 V DC. This means a two-stage converter with two-stage efficiency losses [3, 5]. Using a conventional buck converter causes very low efficiency (less than 90%) because of very low duty cycle operations. It is common choice in the literature to use a full bridge isolated dc/dc converter topology to get

higher efficiencies. The energy efficiency of the conventional full-bridge ZVS DC/DC converter is around 92% at rated power conditions [20]. Due to high frequency and high power of DC/DC converter, its efficiency is to be lower than 92%. It means that using a DC/DC converter causes at least 8% extra efficiency losses.

From the perspective of power loss considerations, it can be said that the extra efficiency loss of the proposed converter is about 3.8% (0.3% + 1% + 0.5% + 2%) and therefore, it is a better choice than using an isolated DC/DC converter with 8% extra loss. In other words, the overall efficiency of the proposed converter is expected to higher than that of the conventional converter with DC/DC converter. Furthermore, the proposed converter has fewer switching and high frequency components and controller circuits.

Additionally, switching noises radiated around are not tolerable in high power applications at high dc levels such as 750–900 V DC. Thanks to the step-down isolation transformer, the proposed converter overcomes this problem too.

The proposed converter has some disadvantages, for example a bulky input transformer. Because industrial converters need galvanic isolation as a protection class, this disadvantage become an advantage in industrial converters. Because of additional galvanic isolation transformer, the proposed converter has disadvantage in terms of size and cost comparing with the available rectifiers having DC/DC converter. However, in industrial applications having galvanic isolation transformer and being formed one-stage converter are preferable advantageous.

4. Design and implementation of the proposed converter

A prototype of the proposed converter has been designed for operation from 380 V, 50 Hz input with 250V/125A DC output. This yields a power converter with approximately 32 kW input power. The AC input is assumed to vary between 325 V and 435 V. The principal design equations are given in (26)-(34). Equation (12) can be useful to calculate the thyristor voltage and current ratings. For 32 kW input power and 0.99 power factor, the maximum value of the line current is around 58 A at the lowest AC input voltage of 325 V. Based on the extreme voltage and current values, MCC95-12DA (IXYS) thyristor modules are selected for the design.

Equation (26) can be useful to calculate isolation transformer secondary voltage (VS12)at minimum boost conditions (Dmin = 125%). Thus, the line-to-line secondary voltage of the transformer should be 132 V at the maximum input voltage of 435 V for 250V (VDC) output. For the 32 kW, 380V/127V, 50-Hz power transformer, this yields a turns-ratio of 3 (n = 3).

$$VDC = \sqrt{2} \times VS12/(1 - Dmin) \tag{26}$$

[21] is very useful to design the low frequency high power input isolation transformer having selected properties.

The boost inductance (L1, L2, L3) can be calculated by using equation (27),

$$Lmin > (\frac{2}{3} \times VDC + VS12)/(2 \times Fsw \times \triangle I) \tag{27}$$

where Lmin is the minimum required inductance value in mH, Fsw = 16 kHz is switching frequency, $\triangle$I is the maximum inductor current ripple allowed at the worse condition in continuous conduction mode (CCM) and preferred as 15–20 of maximum current in general. For $\triangle$I=20 A, Lmin is calculated as higher than 0.463 mH.

Boost inductors (L1, L2, L3) design can be carried out by using (28), where μ is the core permeability, Ae is the effective cross section in mm2, le is the core magnetic path length in mm, N is number of turns. Thus, 12 blocks of 00K4741B026 (magnetics large kool-Mu, $\mu = 26$) are used with 60 turns for 0.55 mH inductor design.

$$L = (0.4 \times \pi \times \mu \times N^2 \times Ae \times 10^{-}6)/le \tag{28}$$

From the literature experiences, resonant frequency of filter should be selected between 1/4 and 1/5 of the switching frequency to get best filtering performance. So, resonant frequency (fr) of filter is selected as 3 kHz. Experiences about the LCL filter design advises to select Lf is 1/5 of the L1. So that, Lf is selected as 0.11 mH. To calculate Cf for LC and LCL filter, equations (29) and (30) are determined.

$$fr = \frac{1}{(2 \times \pi\sqrt{L1 \times Cf})} \tag{29}$$

$$fr = \frac{1}{2 \times \pi}\sqrt{\frac{(L1 + Lf)}{(L1 \times Lf \times Cf)}} \tag{30}$$

To make a good decision about filter type, transfer functions of L, LC and LCL filter circuits can be determined as (31)–(33). Using these equations, bode diagrams of filters can be plotted in Matlab (MathWorks, Inc., Natick, MA, USA) program. Figure 5 shows bode diagrams of different filter applications. It can easily be realized from the bode plots that LCL filter has best performance with –113 dB/dec in higher frequencies.

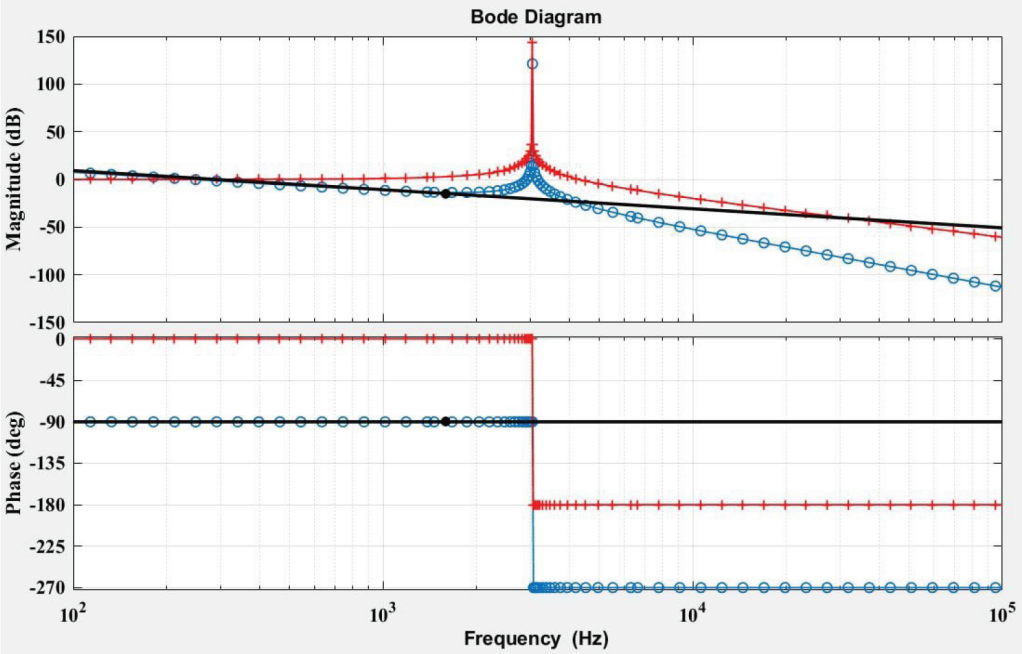


Figure 5. Bode diagrams of different filter applications, blue: LCL, red: LC, black: L

$$G(s) = \frac{1}{(L1)S} \tag{31}$$

$$G(s) = \frac{1}{(L1 \times Cf)S^2 + 1} \tag{32}$$

$$G(s) = \frac{1}{(L1 \times Lf \times Cf)S^3 + (L1 + Lf)S} \tag{33}$$

Each IGBT has $nxIrms(line)$ current rating. This means the maximum current is $58x3 = 174$ A rms and 348 A peak. Maximum secondary line-to-line voltage is 131 V-rms and 185 V-peak. Highest voltage stress on IGBT is 435 V $(185 + 250)$. Thus, CM400DY-12NF (Mitsubishi IGBT module) is selected for the design.

The minimum required output dc capacitor value can be calculated as follows:

$$Cmin = \frac{IDC}{Fsw \times \triangle VC} \tag{34}$$

If Fsw = 16 kHz, IDC = 125 A, $\triangle$VC = 5 V (250 V$\pm$1%) are selected Cmin can be calculated as 1.5 mF. It should be kept in mind that, to increase the stiffness of the supply C should be selected much higher than this value.

Based on these calculations the parameters listed in Table 1 have been chosen.

Table 1. Parameters of the proposed converter.

	Calculated Value	Used Value
Fsw	16 kHz	16 kHz$\pm$15%
Lf	0.11 mH	0.11 mH (iron) $\times$ 3
Cf	30 uF	30 uF (high frequency) $\times$ 3
Cout	1.5 mF	10 mF/350 V $\times$ 3
L1,L2,L3	0.46 mH	0.55 mH (ferrite) $\times$ 3
TRX	380 V/127V	380ac/127ac, 32KW
Q1-Q6	435 V, 348 A	CM400DY-12NF IGBT module $\times$ 3
T1,T2	620 V, 58 A	MCC95-12DA thyristor module $\times$ 2

Figure 6 shows the electronic and control parts of the prototype converter. Mitsubishi CM400DU-12NF IGBT modules and VLA550 IGBT driver IC were used in the IGBT circuit, MCC 95-12 thyristor modules, and isolated gate drivers were used in the thyristor circuit, Microchip's dsPIC30F4011 with 120 MHz processor clock frequency was used in control circuits with special electronic circuits and software algorithms. LEM company current sensor (HAS-200) was used to measure output DC current. Linear AC toroidal current sensors (1/2000) were used to measure input currents. Low power voltage transformers (380/15V) were used to measure the input AC voltage signals. Magnetics block ferrites were used to design high current input boost inductors.

5. Experimental results of the proposed converter

Experimental tests were done with the proposed converter at 245 V, 0–125 A output power with 50 Hz line frequency. The results are presented in Table 2, where V12 is the input ac voltage, VDC is the output dc

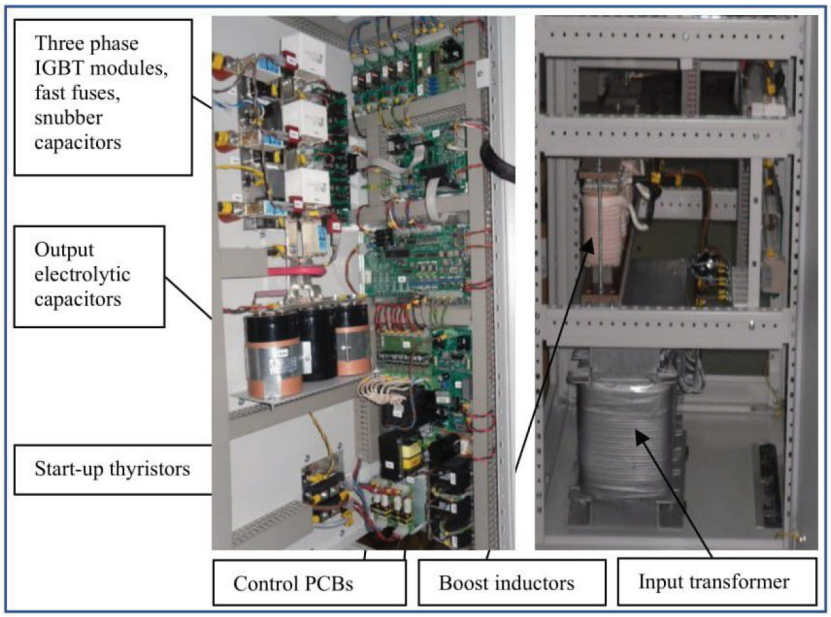


Figure 6. Power and control parts of proposed converter.

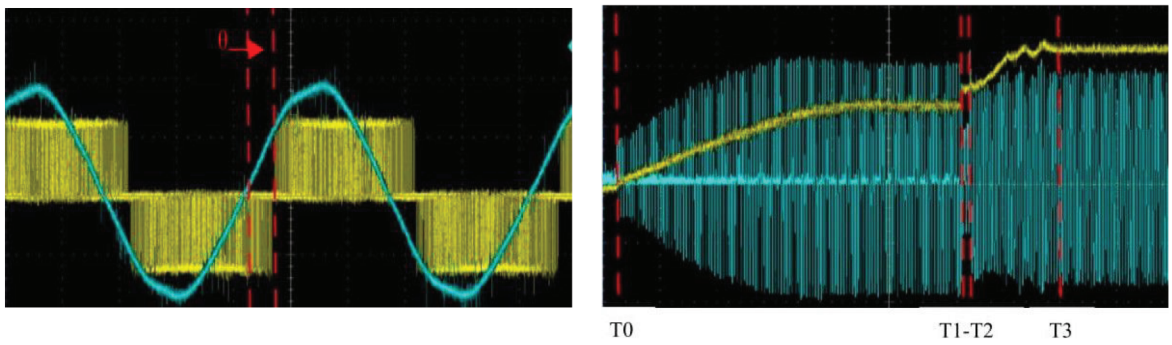
voltage, IL1 is the inductor current, IDC is the output dc current, PF is the input power factor, THDi is the input current total harmonic distortion and η is the efficiency of the proposed converter.

Table 2. Experimental results of the proposed converter

V12(V)	VDC(V)	IL1(A)	IDC(A)	PF	THDi%	η%
325	245	48	34	0.96	4.5	93
325	245	90	66	0.96	4	93
325	245	140	100	0.97	3.5	94
335	245	170	125	0.97	3.5	94
380	245	40	34	0.97	4.5	94
380	245	76	66	0.97	4	94
380	245	115	100	0.99	3.5	95
380	245	141	125	0.99	3.5	95
430	245	37	34	0.97	5	95
435	245	66	66	0.97	5	95
435	245	100	100	0.99	4.5	96
435	245	121	125	0.99	4	96

Figure 7(a) shows the voltage between the mid-points of the IGBT rectifier (16 kHz) and the line current on inductor L1. θ is the phase shift caused by the inductor voltage drop on L1 and L2 at the full power when the PF is 0.99. Because of the high currents flowing through the inductors, there is a phase difference between the transformer secondary voltage and the input voltage of the IGBT rectifier. Since the synchronization algorithm used in the algorithm has feedbacks both from the voltage and the current, high PF is achieved for any load

value.

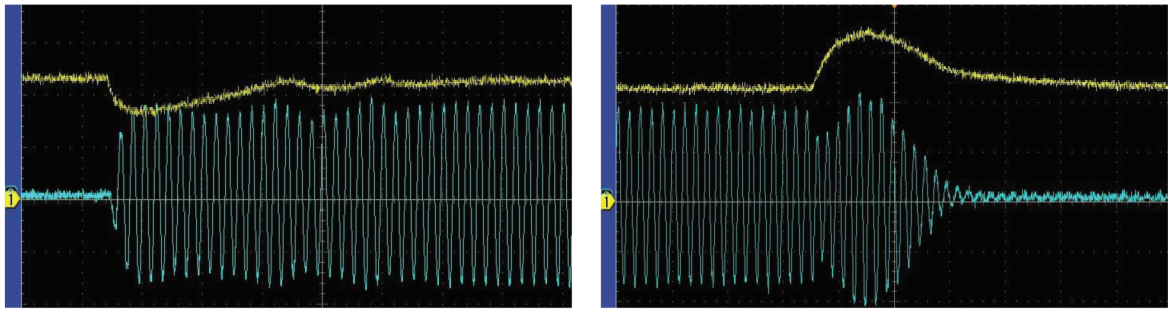


(a) (b)

Figure 7. Waveforms of proposed converter, (a) input voltage of IGBTs (yellow), and the line current (blue) at full load, (b) output voltage of the PWM rectifier(yellow) and the line current (blue) during start-up

Figure 7(b) shows the output voltage and inductor current signals during the start-up of the IGBT rectifier. During the time interval [T0–T2], all IGBTs gates are disabled. During the time interval [T0–T1], the firing angle of thyristor block1 (T1 in Figure 1) is advanced from 180° to 0° while thyristor block2 (T2 in Figure 1) is kept off. In this soft starting period Line1 and Line2 are applied to the transformer and the secondary acts like a single-phase controlled rectifier. At t = T1 both thyristor blocks are triggered with full angle which means thyristor blocks are short circuited and all three phases of the transformer are energized that the secondary acts as a three-phase diode rectifier. As a result of three-phase operation, the input current starts decreasing as seen in Figure 7(b). During time interval [T2–T3], IGBT gate signals are applied with soft starting duty-cycle to boost the output voltage to its desired value. After t = T3 time the IGBT rectifier is in the steady-state mode at full power.

Figure 8(a) shows the 0% to 100% step loading response of the output DC voltage and inductor AC current. Figure 8(b) shows the 100% to 0% step load removal response of output the same quantities. It can be seen in Figure 8(b) that after the load is 0%, IGBT rectifier transfers the regenerated energy from the capacitor to the AC side to discharge the output capacitor to the desired value. This behavior is like a grid-tied inverter.



(a) (b)

Figure 8. Dynamic response of the proposed converter, yellow is output DC voltage 100 V/div, blue is line current 100 A/div, (a) step loading 0% to 100%, (b) step load removal 100% to 0%.

6. Conclusion

In industrial applications, it is very common to use AC/DC converters having 380/400/415VAC input with 110/220V or 450V DC output. In this paper, a novel step-down isolated three-phase PFC rectifier topology with a novel start-up circuit is proposed. The proposed converter is a single stage active three-phase boost PFC rectifier that can operate at low dc levels too. Proposed start-up circuit has soft-start and emergency-stop abilities. Thanks to thyristor triggering control, inrush input currents causing from the uncontrolled-initial-charge of high-mF output capacitors because of reverse diodes of IGBTs can be eliminated. Furthermore, thyristor-controlled start-up circuit provides fast switch-off ability to IGBT rectifier in emergency states such as short-circuits. In comparison to other start-up circuits advised for six-switch IGBT rectifier in literature [3, 4], the proposed circuit is more applicable, more reliable and more stable.

A control strategy called CS-LUT-SPWM was also proposed in this paper along with a switching frequency-oriented synchronization (SWFOS) software method using dsPIC algorithms to enhance the look-up table sinusoidal PWM (LUT-SPWM) to overcome THDi problems at different frequencies in acceptable bandwidths. Proposed CS-LUT-SPWM method has good performance. The main difference of the proposed method is that it completes the calculations in nanoseconds due to the SWFOS method.

In order to explain how the proposed converter works, an isolated 32 kW active three-phase rectifier (converting 380 V/50 Hz AC input to 250 V/125 A DC output) with proposed start-up circuit was implemented, tested, and evaluated in this paper. Experimental results of are presented.

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