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Mismatch error shaping of DAC unit elements in multibit $\Delta\Sigma$ modulators using a novel unified ADC/DAC

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Abstract: This paper presents a unified analog to digital converter (ADC) and digital to analog converter (DAC) for multibit $\Delta\Sigma$ modulators. The unified ADC/DAC circuit provides error shaping for mismatches between DAC unit elements. Hence, the dynamic element matching (DEM) circuit or digital calibration is not required resulting in the area and power saving as well as the elimination of the excess loop delay introduced by DEM circuit. Incorporating a 6-bit unified ADC/DAC, the $\Delta\Sigma$ modulator achieves 16.15-bit resolution utilizing only a second order loop filter and oversampling ratio of 40. The proposed modulator is simulated in a 65-nm CMOS process. Intended for audio applications, it achieves 102-dB dynamic range, and 99-dB signal to noise and distortion ratio in a 25-kHz bandwidth sampled at 2 MS/s. The power dissipation and power supply are 149.8 μW and 1.4 V, respectively.

Key words: DAC mismatch error shaping, dynamic element matching, multibit $\Delta\Sigma$ modulator, unified ADC/DAC

1. Introduction

$\Delta\Sigma$ modulator with a multibit quantizer is a suitable architecture for high resolution and low oversampling ratio (OSR) modulators. The high resolution internal analog to digital converter (ADC) in a $\Delta\Sigma$ modulator reinforces the effect of the noise shaping and oversampling to increase the signal to quantization noise ratio (SQNR). Moreover, the incorporation of multibit internal quantization leads to the more stable modulator, the less sensitivity to the clock jitter and the relaxed slew rate requirement for the first loop filter [1–3].

The implementation of the internal ADC is rather simple, because any errors in ADC are subjected to the maximum noise shaping. But the mismatch error between unit elements of the feedback digital to analog converter (DAC) is directly fed into the input of the modulator, distorting the output of the modulator [4–6].

There are two common methods to achieve the linearity requirements in the literature. One is the digital calibration technique [7] which requires accurate measurements of the DAC mismatch errors and storing them [8, 9]. The other is the dynamic element matching (DEM) technique, which randomizes and shapes the mismatch error between unit elements of the multibit feedback DAC to the high frequencies [10, 11]. Although these techniques are effective, they increase the complexity of the circuit and lead to more power consumption and area occupation [12, 13]. Furthermore, the additional delay caused by the implementation of these methods results in a large excess loop delay (ELD) in the feedback path [14].

In this paper, the mismatch error between unit elements of the feedback DAC is shaped by the noise transfer function (NTF) of the modulator without any need for additional digital circuitry. To achieve this goal

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the internal ADC and feedback DAC are unified and implemented in one circuit. The outputs of the circuit are different quantized levels, fed back to the input of the modulator through an array of switches. The digital output code is generated from the quantized levels. The presented $\Delta\Sigma$ modulator incorporating the proposed unified ADC/DAC is simulated in 65-nm CMOS technology using CADENCE VIRTUOSO. Simulation results indicate the capability of the presented architecture to shape the mismatch error between DAC unit elements.

The organization of the paper is as follows: Section 2 presents the unification of the internal ADC and feedback DAC. Section 3 describes the implementation of the unified ADC/DAC. Section 4 covers circuit design. Section 5 reports the simulation results and Section 6 concludes the paper.

2. Unification of internal ADC and feedback DAC

As shown in Figure 1a, in conventional $\Delta\Sigma$ modulators the mismatch error between unit elements of the feedback DAC superposes to the input signal. According to (1), this error goes to the output without any shaping and degrades the signal to noise and distortion ratio (SNDR) of the modulator output.

$$V_{out}(z) = \frac{H(z)}{1+H(z)}V_{in}(z) + \frac{1}{1+H(z)}E_Q(z) - \frac{H(z)}{1+H(z)}E_{DAC}(z) \tag{1}$$

An N-bit DAC in the feedback path of a $\Delta\Sigma$ modulator, switches K out of $M = 2^N - 1$ unit elements toward the output node under the control of M thermometer codes (M-TC) coming from ADC. In Figure 1a, the DAC is shown in two blocks: M unit elements and M switches. The outputs of the block of M unit elements are M quantized levels (M-QL) weighted $K.\Delta(K = 1, ..., M)$, where $\Delta = V_{FS}/M$ is the least significant bit (LSB) and V_{FS} is the full scale supply voltage. One of the quantized levels is fed back to the input of the modulator through M switches controlled by M-TC. The mismatch error of the unit elements introduces the error in the quantized levels, E_{DAC}.

Let us assume the internal quantizer produces the quantized levels, M-QL, at the output as shown in Figure 1b. In this way, the error of the quantized levels, E_{DAC}, is added to the modulator loop in the feed-forward path and thus shaped by NTF of the modulator given by Eq. 2. To design such a quantizer, the unit elements block of the feedback DAC is moved to the feed-forward path. ADC and unit elements block are implemented in one circuit as a unified ADC/DAC.

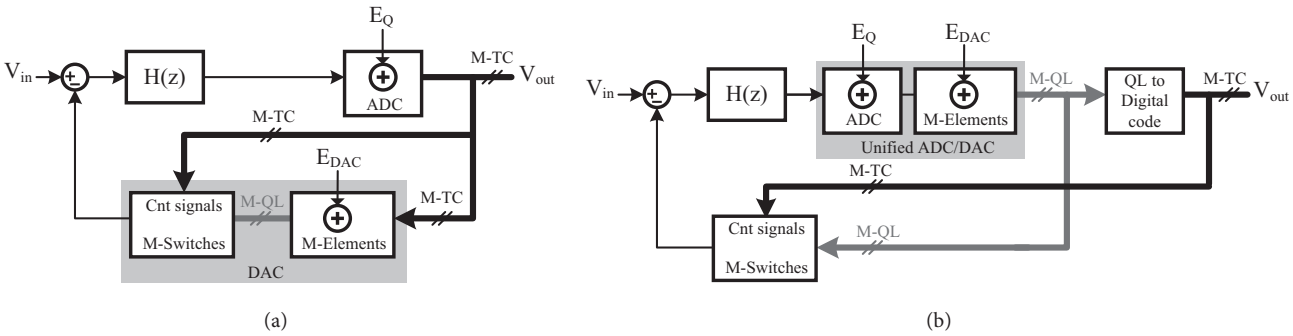

Figure 1. (a) Conventional $\Delta\Sigma$ modulator with feedback DAC shown by two blocks: M unit elements and M switches. (b) $\Delta\Sigma$ modulator with a unified ADC/DAC and a digital block to generate output codes from quantized levels (QL).

$$V_{out}(z) = \frac{H(z)}{1+H(z)}V_{in}(z) + \frac{1}{1+H(z)}(E_Q(z) + E_{DAC}(z)) \quad (2)$$

The internal ADC in a conventional $\Delta\Sigma$ modulator is commonly an N-bit flash ADC implemented by $M = 2^N - 1$ comparators. Each comparator consists of a preamplifier and a regenerative latch as shown in Figure 2a. To unify internal ADC with the unit elements block, a resistive string is used to produce M quantized levels $(V_Q(1), ..., V_Q(M))$. Applying the K^{th} quantized level $(K = 1, ..., M)$ as a power supply of the regenerative latch in the K^{th} comparator, the outputs of the comparators present the required quantized levels, M-QL.

3. Implementation of the unified ADC/DAC

As mentioned, to produce the quantized levels, M-QL, the regenerative latches in the comparators are supplied with the quantized voltages produced by a resistive string. The simplest form of a regenerative latch is a cross-coupled pair shown in Figure 2b. The cross-coupled pair requires a minimum supply voltage of V_{th} to work properly, where V_{th} is the threshold voltage of transistors. Thus, the minimum LSB, Δ, is V_{th}, which limits the resolution of the unified ADC/DAC. In 65-nm CMOS technology, the threshold voltage is about 400–500 mV. Assuming $V_{FS} = 1.4$ V, the resolution of the unified ADC/DAC is not allowed to be more than 2 bits.

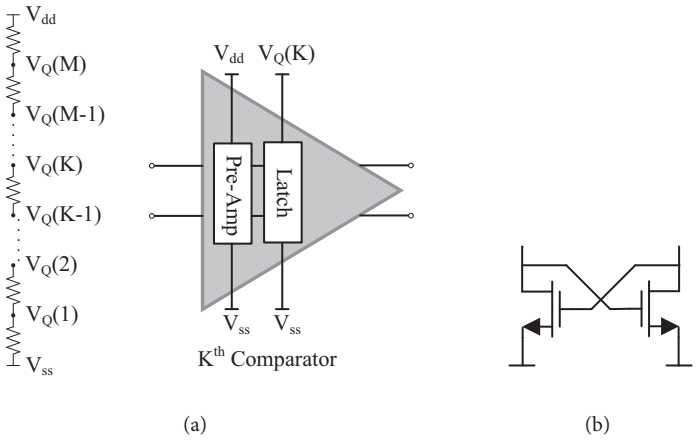

Figure 2. (a) A comparator consists of a preamplifier and a regenerative latch. $V_Q(K)$, produced by a resistive string, supplies the K^{th} regenerative latch. (b) A cross-coupled pair.

However, a unified ADC/DAC with a higher number of bits provides a higher resolution and lower OSR modulator. In this work, a 6-bit unified ADC/DAC is employed with the LSB of 21.875 mV. To produce $2^6 - 1 = 63$ quantized levels in the output of the 6-bit unified ADC/DAC, latches have to work with supply voltages of $K \times 21.875$ mV $(K = 1, ..., 63)$. Obviously, designing the latches for small Ks is practically impossible.

To solve this problem, the technique introduced in [15–17] is applied to reduce the input swing of the comparators. Since the input swing of the comparators diminishes, comparators never used can be removed. Thus, the quantized levels supplying the remained regenerative latches are $K \times 21.875$ mV, where $A < K < B$

and $1 \ll A < B \ll 63$. The minimum value of the quantized levels is $A \times 21.875$ mV which has to be large enough to drive the regenerative latch. The technique introduced in [15–17] adjusts the swing in the input of the comparators, as shown in Figure 3a.

Since successive outputs are significantly correlated due to the multibit quantization and oversampling, the subtraction of successive outputs is lower than the output itself. In Figure 1a the output of the modulator, V_{out}, is the quantized version of the output of the loop filter. Accordingly, the difference between the output of the loop filter and its previous quantized value, V_{out}, results in a low swing voltage at the input of the comparators, as shown in Figure 3a. A digital summation at the output of the modulator compensates the subtraction, leaving the signal transfer function (STF) and NTF unchanged [17]. There are M' thermometer codes (M'-TC) at the output of the ADC which $M' < M$, however, the resolution of ADC is still N-bit ($M = 2^N - 1$).

3.1. Second order $\Delta\Sigma$ modulator using unified ADC/DAC

Figure 3b shows the second order $\Delta\Sigma$ modulator including introduced technique in [15–17] to reduce the input swing of the comparators. As shown, the analog feed-forward path reduces the output swing of the first integrator, relaxing the requirements for the first loop filter.

The subtraction at the input of the comparators in Figure 3b requires an amplifier for implementation, resulting in more power consumption. To avoid this, the path at the input of the comparators is transferred back to the input of the second integrator as shown in Figure 3c, where the analog version of V_{out} is multiplied by $0.5(1 - z^{-1})$ to keep the transfer function unchanged [16, 17]. As shown in Figure 3d, the $(1 - z^{-1})$ can be avoided by taking the feedback from the output of the internal ADC, since $Y_{ADC} = (1 - z^{-1})V_{out}$. Y_{ADC} contains M' thermometer codes, so the feedback DAC uses M' unit elements and switches to convert it to the analog voltage. Besides, a DAC including M unit elements and switches, converts M thermometer codes at the output of the modulator, V_{out}, to the analog voltage.

Applying the unified ADC/DAC as a quantizer to the second order $\Delta\Sigma$ modulator shown in Figure 3d yields Figure 3e. The unified ADC/DAC includes the quantization error, E_Q, and the mismatch error of DAC unit elements, E_{DAC}. Hence, both errors are shaped by NFT of the modulator. A digital circuit generates the digital thermometer code, Y_D, from the quantized levels, Y_Q. In the digital domain, $Y_D = (1 - z^{-1})Y_{out}$ is added to the delayed version of Y_{out} to produce the output digital code, Y_{out}.

M' quantized voltages at the output of the unified ADC/DAC, Y_Q, go through an array of M' switches controlled by M' thermometer codes, Y_D. The selected voltage at the output of the array of switches, V_{DAC}, is fed back to the input of the second integrator. To feed back V_{out} to the input of the loop filters, an M-bit DAC in the feedback path is required. To avoid using an extra DAC, an analog integrator is employed to produce the full swing signal, V_{FB}, from the selected voltage of the array of M' switches, V_{DAC}. The output of the analog integrator, V_{FB}, is fed back to the input of both integrators. Hence, in Figure 3e only M' switches and an analog integrator are required in the feedback path using the unified ADC/DAC circuit and the technique of diminishing the input swing of the comparators.

4. Circuit design

A fully differential implementation of the architecture shown in Figure 3e is designed for audio application with a 25-kHz bandwidth. The sampling frequency, f_s, and OSR are 2 MHz and 40, respectively. Using 6-bit unified

ADC/DAC, the effective number of bits (ENOB) is equal to 16.15. The power supply, V_{FS}, is 1.4 V resulting in an LSB of $\Delta = 21.875$ mV. Applying the technique of [15–17] diminishes the input swing of the comparators to $Y = 170$ mVpp. Thus, in the 6-bit unified ADC/DAC, the number of comparators reduces from 63 to 9.To avoid saturation, two more comparators are added resulting in 11 comparators. The quantized levels at the output of the unified ADC/DAC are $K \times 21.875$ mV, $(K = 27, ..., 37)$.

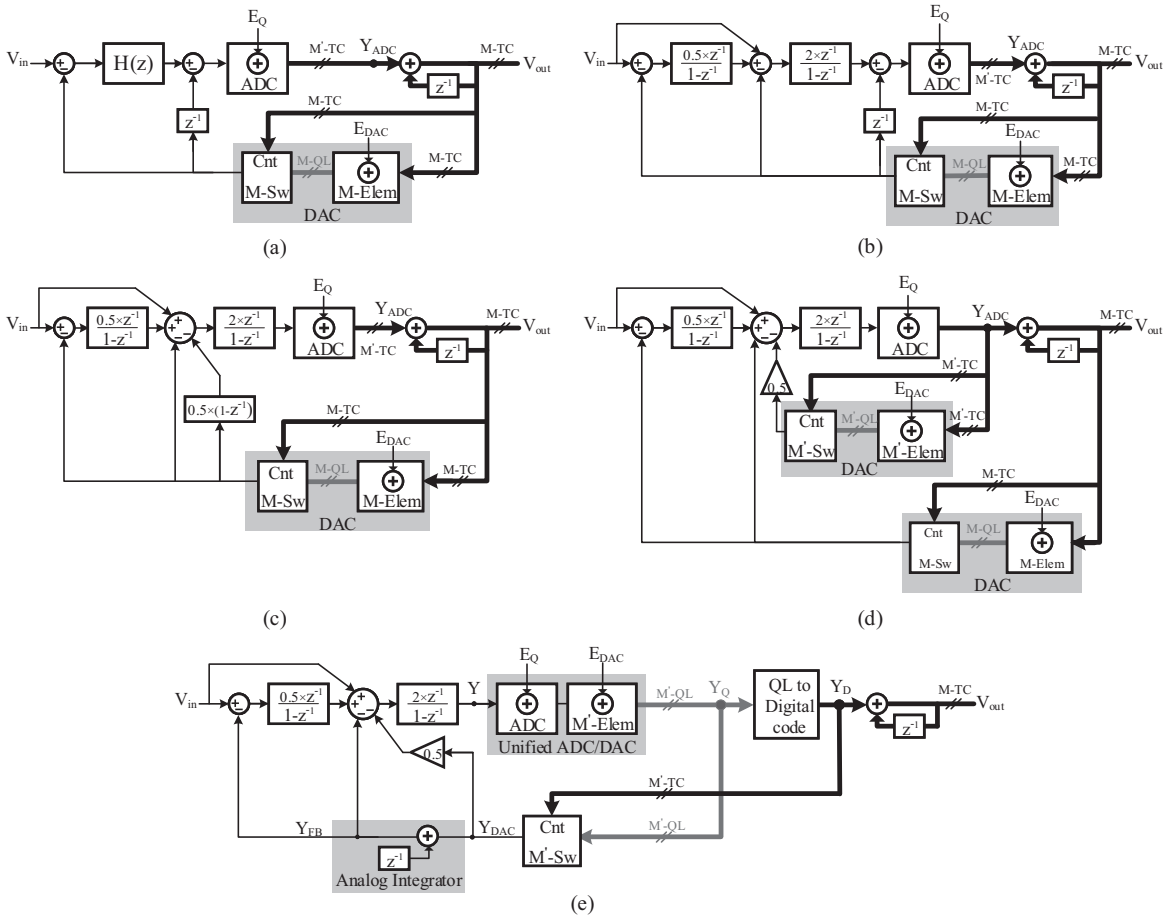

Figure 3. (a) The technique introduced in [16] to reduce the input swing of the comparators. (b) Second order $\Delta\Sigma$ modulator including the mentioned technique. (c) Transferring the path at the input of the comparators back to the input of the second integrator. (d) Utilizing the output of the internal ADC instead of V_{out}. (e) Second order $\Delta\Sigma$ modulator using the unified ADC/DAC and the technique to reduce the input swing of the comparators.

4.1. Unified ADC/DAC

The unified ADC/DAC contains 11 comparators as shown in Figure 4a. Each comparator is a four-input fully differential preamplifier followed by a regenerative latch which is an energy efficient dynamic structure as depicted in Figure 4b. The comparator compares the differential input voltages with the differential threshold voltages, $V_{th}(i)$, made by a resistive string [18, 19].

A resistive string generates the required quantized voltages, $V_Q(i)$ where $i = 1, ..., 11$. The regenerative latches are supplied by $V_Q(i)$. The differential outputs of the comparators are the quantized voltages. An array

of switches selects the target quantized voltage to feed back to the input of the loop filters. Digital thermometer codes control the array of switches.

4.2. Digital circuit

As shown in Figure 3e, a digital block produces output digital codes from the quantized voltages. The first stage in the digital block has to change the quantized voltages to full scale voltages. For this purpose, a brand new inverter is presented as shown in Figure 4c. Since quantized levels are not full swing, a CMOS inverter supplied by a full scale power supply, V_{FS}, is not able to fully scale the quantized levels. To solve this problem, the brand new inverter utilizes a diode connected PMOS transistor, M_{P_L}, as a load in the CMOS inverter, as shown in Figure 4c. The diode connected transistor drops the source voltage of $M_{P_{inv}}$. Thus, the proposed inverter is able to invert the quantized levels and turn them to the full scale voltages.

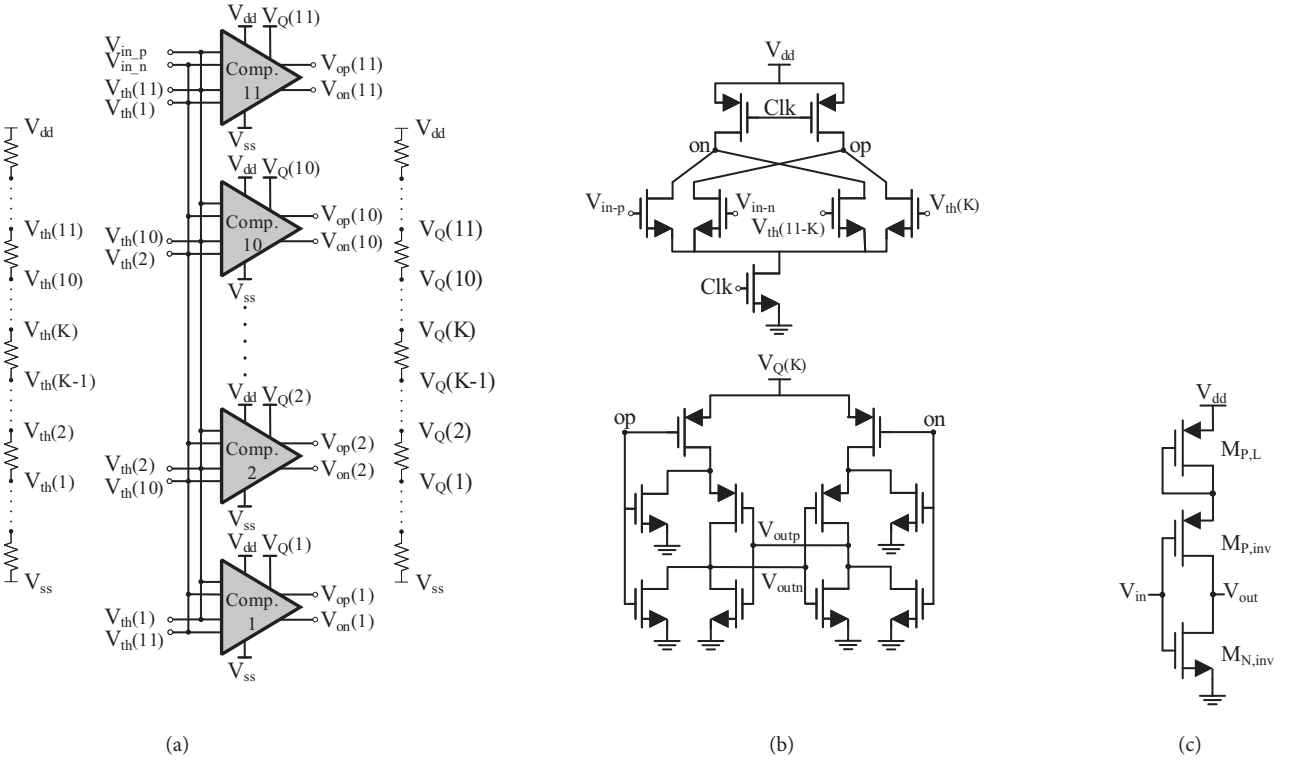

Figure 4. (a) 11 comparators constructing the unified ADC/DAC along with two resistive strings generating the threshold, and quantized voltages. (b) A comparator consists of a preamplifier and a latch. (c) A brand new inverter.

Besides, there is an encoder in the digital block. It corrects bubble errors and generates one-out-of-M codes to control the switches in the feedback path.

4.3. Loop filters

Switched-capacitors (SC) integrators are employed as the first and second loop filters along with the analog integrator in the feedback path, as shown in Figure 3e.

kT/C noise, caused by sampling, determines the minimum amount of capacitors in an SC integrator.

Since the digital filter removes the out of band noise, Eq. 3 determines the kT/C noise power.

$$v_{n,kT/C}^2 = \frac{kT}{OSR \times C_s} \tag{3}$$

For a given ENOB and full scale power supply, V_{FS}, the total noise power must meet the condition of Eq. 4 [20].

$$v_n^2 < \frac{V_{FS}^2}{8 \times 2^{2\times ENOB}} \tag{4}$$

In this design kT/C noise is considered as the fundamental limitation of the total noise. Substituting Eq. 3 to Eq. 4, leading to Eq. 5, determines the minimum sampling capacitance $C_{s,min} = 1.8$ pF. To assign a noise budget to other noise sources, a 3-pF sampling capacitor is employed in this design.

$$v_{n,kT/C}^2 = \frac{kT}{OSR \times C_s} < \frac{V_{FS}^2}{8 \times 2^{2\times ENOB}} \tag{5}$$

The timing diagram is shown in Figure 5a. Both SC integrators sample the data in phase one, Φ_1, and integrate it in phase two, Φ_2. Figure 5b shows the status of the SC integrators in each phase. Thanks to the feed-forward path to the input of the second integrator, input signal V_{in} is sampled into both C_{s1} and C_{s2} in the sampling phase, where C_{s1} and C_{s2} are sampling capacitors of the first and second integrators, respectively. Thus, the total sampling capacitor is $C_s = C_{s1} + C_{s2}$. By choosing $C_{s1} = C_{s2}$, each sampling capacitor equals 1.5 pF, relaxing the OTAs requirements.

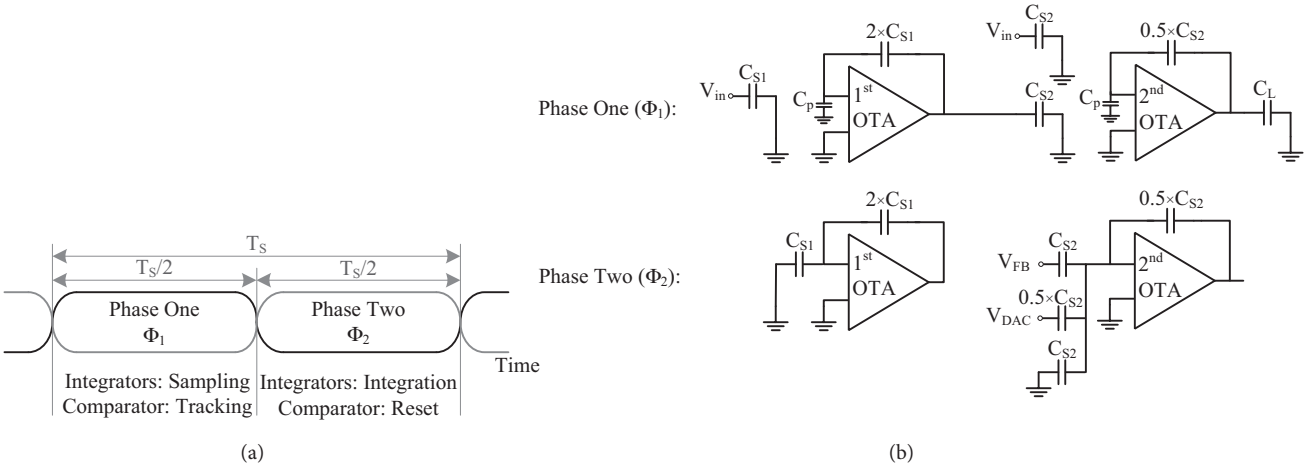

Figure 5. (a) Timing diagram of the SC integrators and the comparator. (b) The status of the SC integrators in each phase.

The operational transconductance amplifier (OTA) is a simple single-stage folded cascade amplifier shown in Figure 6a together with its frequency response demonstrated in Figure 6b. The OTA is designed to reach a 60-dB DC gain consuming 40 μW power. For $C_s = 1.5$ pF, the gain-bandwidth product (GBW) of the OTA is 17.2 MHz which is about 8.5 times larger than the sampling frequency.

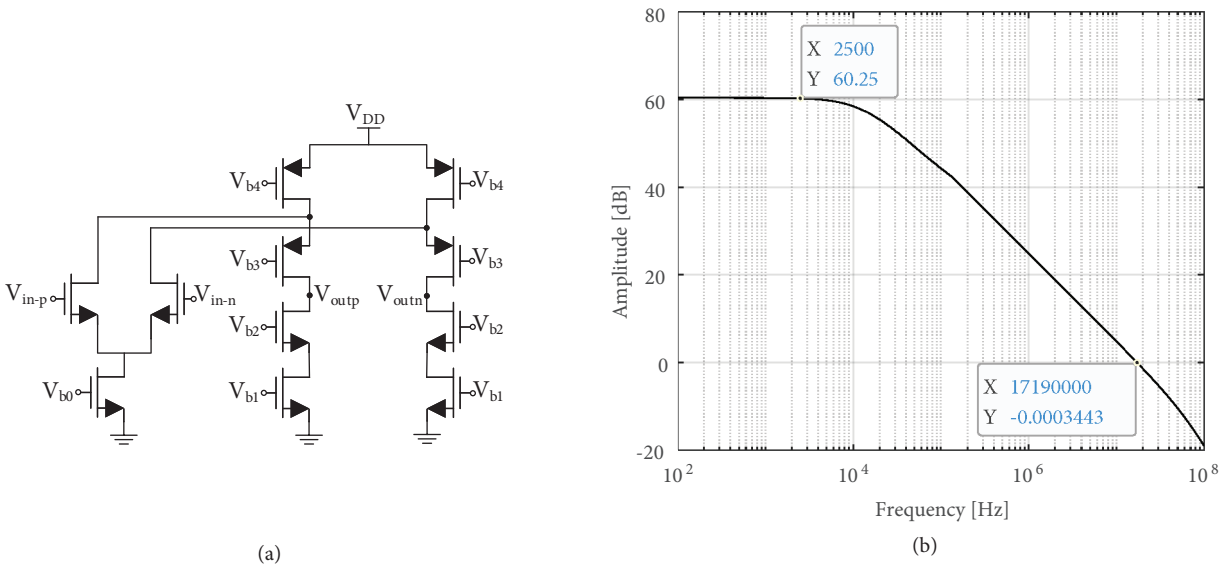

Figure 6. (a) A single-stage folded cascade amplifier and (b) its frequency response.

5. Simulation results

A conventional second order $\Delta\Sigma$ ADC shown in Figure 7a and its equivalent proposed modulator shown in Figure 7b are simulated in MATLAB Simulink with a 6-bit internal quantizer and OSR=40. To study the mismatch error shaping of the DAC unit elements, performances of the conventional and proposed modulators are compared.

The loop filters and internal ADC are ideal in Figure 7. Assuming there are no mismatches between DAC unit elements, both architectures achieve a 101-dB SNDR. The output power spectrum densities (PSD) are shown in Figure 8a.

To investigate the effect of a mismatch error between DAC unit elements, an error is introduced to the output of the feedback DAC in the conventional modulator. The error is a Gaussian distribution with a zero mean and a 1% standard deviation. The solid curve in Figure 8b shows the output PSD of the conventional modulator with a 1-kHz input signal representing a 91.3-dB SNDR. Figure 9a shows the simulated SNDR for 100 iterations resulting in a mean SNDR of 91 dB. The simulations show that the mismatch error is not shaped and degrades the SNDR about 10 dB.

The same error is introduced to the output of the unified ADC/DAC in the proposed modulator. The output PSD of the proposed modulator is depicted in the dotted curve of Figure 8b displaying a 98.1-dB SNDR. The simulated SNDR for 100 iterations results in a mean SNDR of 97.9 dB as shown in Figure 9b. The SNDR is reduced only 3 dB which represents about a 7-dB SNDR improvement in comparison to the conventional one. Thus, utilizing the unified ADC/DAC as a quantizer shapes the mismatch error between DAC unit elements, while DEM or digital calibration is not required.

To extract the performance of the proposed structure, the second order $\Delta\Sigma$ ADC shown in Figure 3e is designed and simulated fully differentially in 65-nm CMOS technology using CADENCE VIRTUOSO in schematic level. The resolution of the unified ADC/DAC and ENOB are 6 and 16.15 bits, respectively. Thanks to the use of the technique introduced in [17] to reduce the input swing of the comparators, only 11 comparators are required to design the 6-bit unified ADC/DAC.

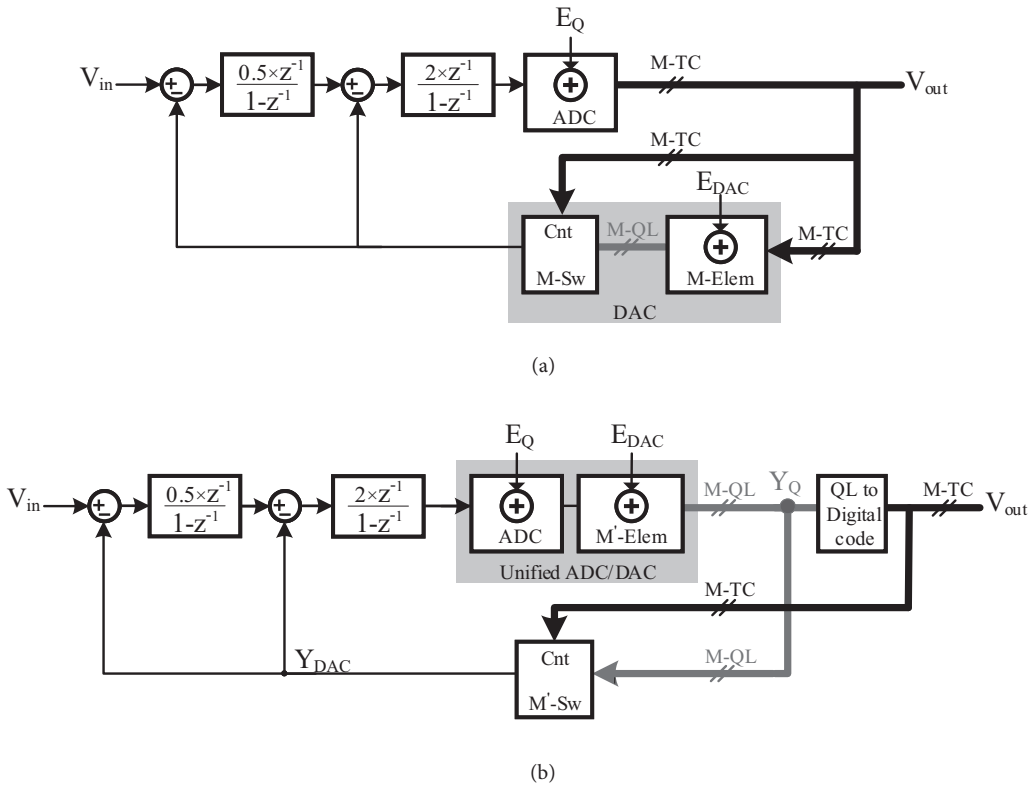

Figure 7. (a) A conventional second order $\Delta\Sigma$ modulator and (b) its equivalent proposed modulator.

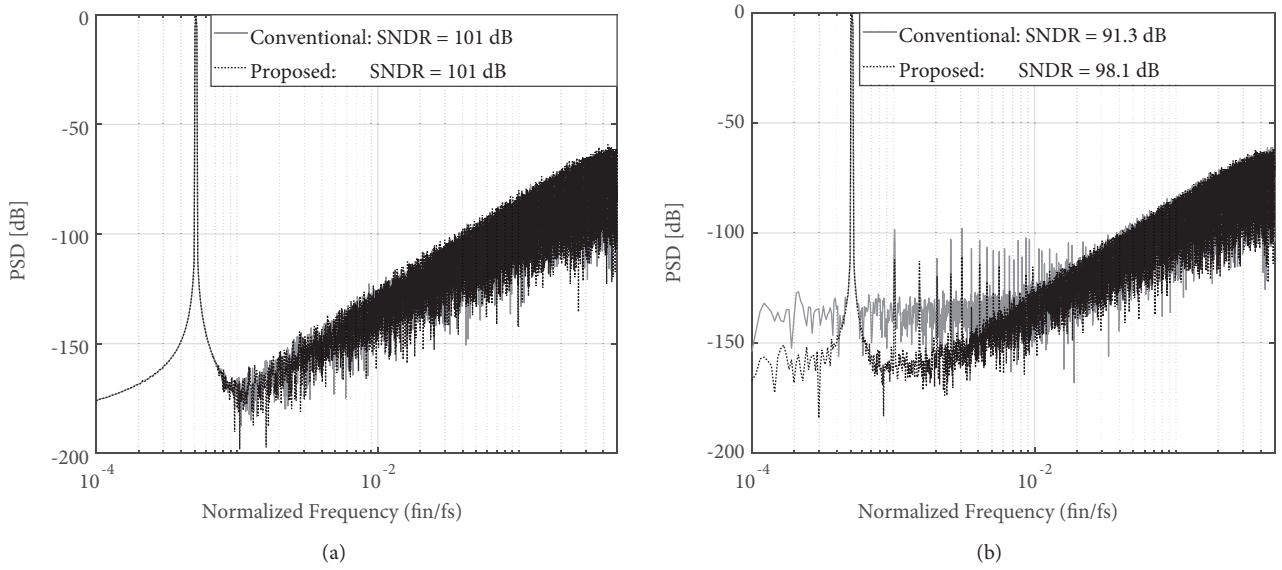

Figure 8. The output PSD of the conventional (solid curves) and the proposed (dotted curves) modulators. (a) Including an ideal DAC. (b) Introducing a mismatch error between DAC unit elements.

Figure 10a shows the simulated 16384-point windowed FFT spectrum of the proposed modulator with a 4.5-kHz input signal sampled at 2 MS/s. Utilizing the second order loop filter, the output spectrum illustrates

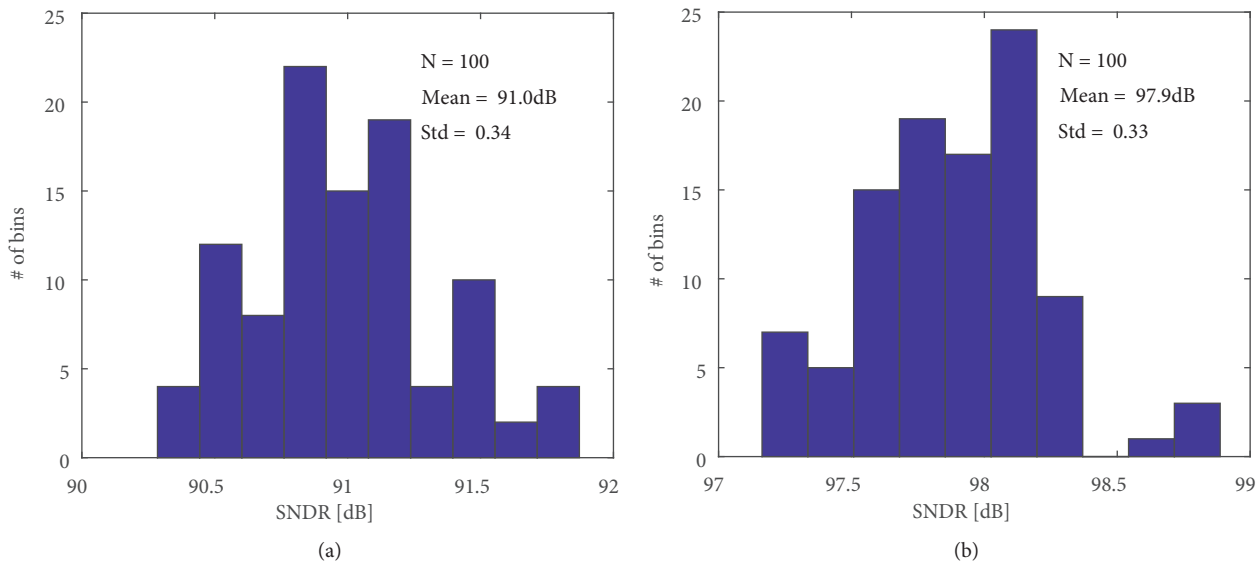

Figure 9. The simulated SNDR for 100 iterations in the presence of a Gaussian distributed error in (a) conventional modulator and (b) proposed modulator.

a 40-dB/dec noise shaping characteristic. An OSR of 40 gives a 98.7-dB SNDR corresponding to an ENOB equal 16.15.

Figure 10b plots the modulator SNDR versus the input signal amplitude. With a 4.5-kHz input signal, the modulator achieves a 99-dB peak SNDR and a 102-dB dynamic range.

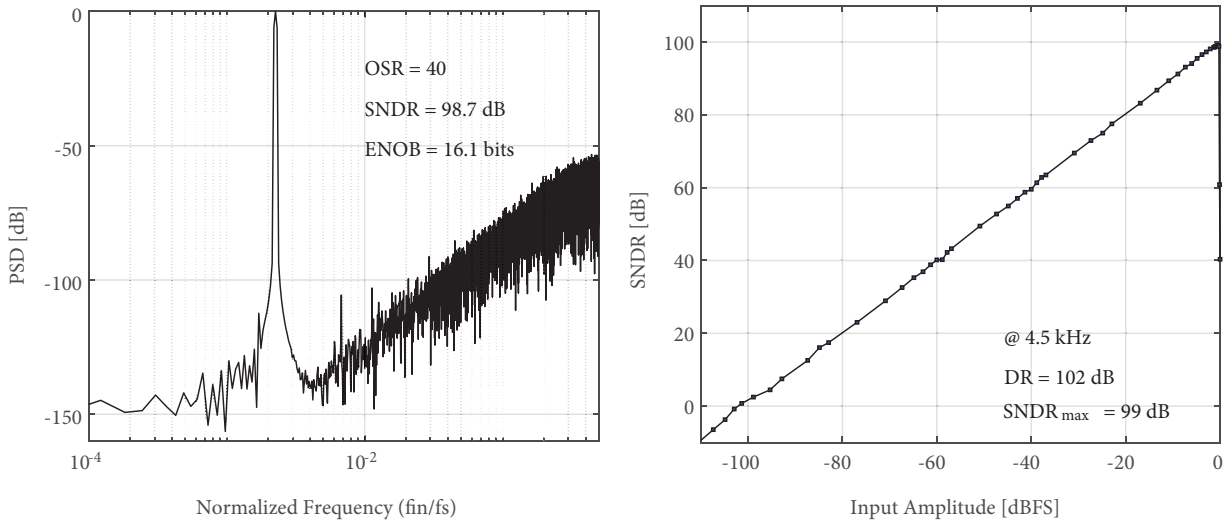

Figure 10. (a) The output PSD of the proposed modulator with a 4.5-kHz input signal. (b) SNDR versus the input signal amplitude with a 4.5-kHz input signal.

The proposed modulator draws 107 μA from a 1.4-V power supply, with the digital circuitry consuming 2% of the power. Three integrators dominate the analog power consumption with their 81.5% contribution. The unified ADC/DAC, composed of 11 comparators and two resistive strings, draws 16.5% of the total power.

Since DEM circuit and digital calibration are not required, power consumption of the digital circuitry is reduced significantly.

Table 1 presents a performance summary of the presented $\Delta\Sigma$ modulator designed and simulated in schematic level using CADENCE VIRTUOSO. Moreover, the performance of the proposed structure is compared to the state-of-the-art $\Delta\Sigma$ ADCs with similar bandwidth designed for audio applications. A key observation is that the proposed modulator achieves a higher resolution than previous designs with a relatively lower OSR. Three different figures-of-merit (FOM) are utilized to assist comparison as defined in Table 2. Presented $\Delta\Sigma$ modulator achieves better FOMs due to the higher resolution obtained from the ability to use a multibit internal quantizer.

Table 1. Performance summary and comparison to state-of-the-art publications.

Parameters	[21]	[22]	[23]	[24]	This work
Simulation level	Schematic	Chip	Postlayout	Schematic	Schematic
Process (nm)	180	130	180	140	65
Supply voltage (V)	1.2	0.6	1.8	1.5	1.4
Power (μW)	44	19.5	28.2	142	149.8
Sampling frequency (MHz)	2.56	0.8	3.2	5.12	2
OSR	128	16	64	128	40
Bandwidth (kHz)	10	25	25	20	25
DR (dB)	—	80	—	98	102
$SNDR_{max}$ (dB)	95.98	77.4	81.3	—	99
ENOB (bit)	15.65	12.56	13.21	16	16.15
FOM (dB)	179.5	168.5	170.8	—	181.2
FOM_{Sch} (dB)	—	171.1	—	179.5	184.2
FOM_{Wa} (fJ/conv.)	43	67	59	54	41

Table 2. The definitions of the figures of merit (FOM).

FOM	Formula
FOM (dB)	$SNDR_{max}$ + 10 $\times$ $\log_{10}$(Bandwidth/Power)
FOM_{Sch} (dB)	DR + 10 $\times$ $\log_{10}$(Bandwidth/Power)
FOM_{Wa} (fJ/conv.)	Power/(2 $\times$ Bandwidth $\times$ 2^{ENOB})

6. Conclusion

A multibit $\Delta\Sigma$ modulator using a novel unified ADC/DAC is presented. The outputs of the unified ADC/DAC are quantized levels instead of digital codes. Thanks to the unified ADC/DAC, the mismatch error between DAC unit elements is shaped with the same order of the quantization error shaping, while DEM circuit or digital calibration is not employed. Eliminating digital circuitry in the feedback path reduces the digital power consumption and saves the area occupation. The presented second order $\Delta\Sigma$ modulator, incorporating a 6-bit unified ADC/DAC, achieves a 16.15-bit resolution with a low OSR of 40 benefiting the mismatch error shaping.

It achieves a 7-dB SNDR improvement in comparison to the conventional one, when a Gaussian distribution error with a 1% standard deviation is introduced as a mismatch error between DAC unit elements.

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