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Efficient modelling of random access memory cell: an approach using QCA nanocomputing

Ali Newaz BAHAR[1], **Angshuman KHAN**[2,*]
[1]Department of Electrical and Computer Engineering (ECE), University of Saskatchewan, Saskatoon, Canada
[2]Department of Electronics and Communication Engineering, University of Engineering and Management, Jaipur, India

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Abstract: Quantum-dot cellular automata (QCA) is innovative and potentially fruitful nanotechnology that provides a solution for transistor-based circuits with enhanced switching frequency, large-scale integration, and low power consumption. The random-access memory (RAM) cell is a fundamental component that is designed to operate quickly and effectively since memory is a core part of the semiconductor industry, thus the QCA family. The RAM cell design in this work is based on a multiplexer structure and is implemented without using coplanar crossovers of QCA technology. QCADesigner-2.0.3, a standard QCA layout design and verification tool, is used in the simulation and validation processes for the proposed circuit. The QCAPro tool is used in order to ascertain the level of energy that is lost. In terms of latency, area, and the total number of cells used, the suggested QCA RAM design achieves better results than its predecessors. Compared to the best design currently available, the suggested layout reduces latency by approximately 50%, the area needs by approximately 43%, and the number of cells by approximately 40%.

Key words: Nanocomputing, QCA, quantum-dot cellular automata, RAM, random access memory

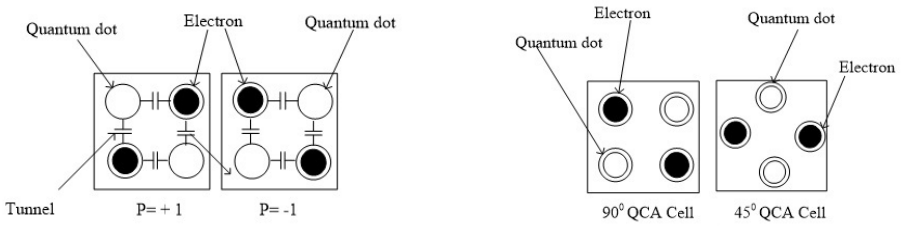
1. Introduction

Complementary metal oxide semiconductor (CMOS) technology, in particular, has advanced quickly during the past ten years [1, 2]. Researchers are trying desperately to find a solution and look for an alternative to traditional technology since some applications call for low power consumption and quick speed [3]. Since quantum-dot cellular automata (QCA) is revolutionary, durable nanotechnology with incredibly low power requirements and a very fast framework for creating an arbitrary function at the nanoscale, it is an excellent candidate technology [4]. There are two distinct kinds of QCA cells, both of which are seen in Figure 1, where Figure 1a shows regular QCA cells and Figure 1b displays 45-degree rotated cells. Four quantum dots comprise a single QCA cell, which may be found in each of the square's four corners. It has two travelling electrons that are diagonally positioned in the corners of the QCA cell. A binary representation may be made using the two stable configurations of two electrons, denoted by the polarisation (P) of -1 (logic 0) and +1 (logic 1), and both stable states are distinguished by it [4, 5].

QCA circuits are made up of three-input majority gates, wire and inverter [4, 5]. It is simple to create a QCA wire using a QCA cell array. Another fundamental block of QCA technology is an inverter. Figure 2 depicts the structure of these essential building pieces. The diagram in Figure 2a represents a QCA wire.

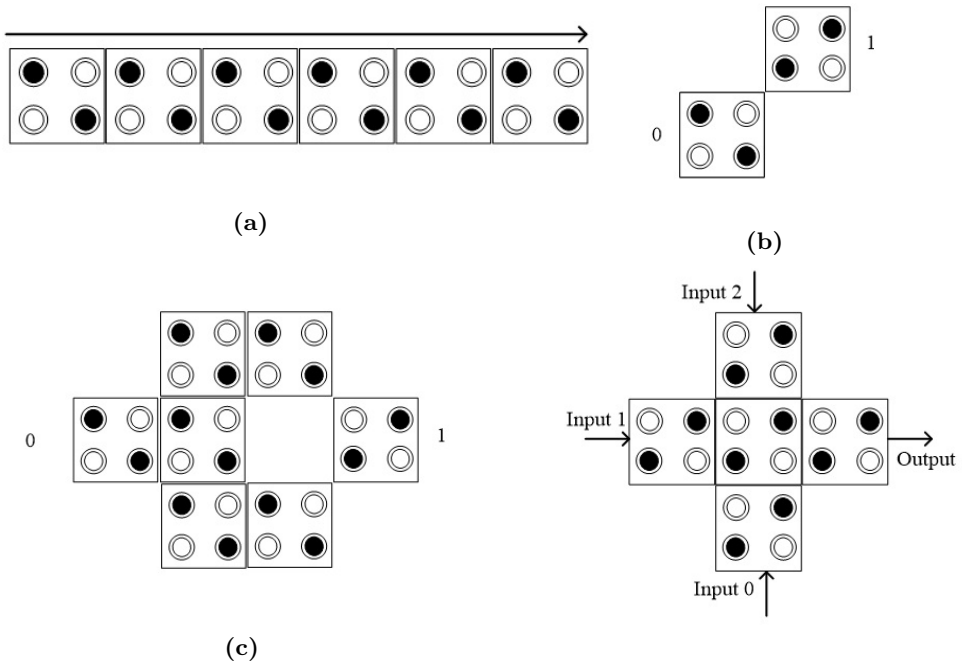
*Correspondence: angshumankhan2910@gmail.com

Figures 2b and 2c show the structure of two distinct inverters using QCA cells. A majority gate with three inputs is shown in Figure 2d. The information is input on the first three sides of this kind of gate, and the outcome is shown on the fourth side.



(a) (b)

Figure 1. (a) Two distinct polarisations of QCA cells, (b) normal and rotated QCA cell.



(a) (b) (c) (d)

Figure 2. Various QCA logic units, (a) the wire, (b) the basic inverter, (c) the regular inverter, and (d) the majority gate/voter.

Another important design paradigm is called a QCA clocking zone, which refers to a cluster of QCA cells with the same QCA clock. The waveform of the four clocking zones are given in Figure 3 so that QCA circuits may be created using those waveforms. Each clocking cycle is comprised of four phases: the switch phase, the hold phase, the release phase, and the relax phase. The phase delay between each of these phases is 90 degrees [4, 5]. Because a single QCA cell would be very susceptible to noise [6], it is recommended that each clocking zone have a minimum of two QCA cells.

Researchers have previously focused on creating reliable QCA circuits. It has been investigated [6] whether sneak noise channels exist in QCA circuits. It was discovered that to build a reliable QCA coplanar crossover

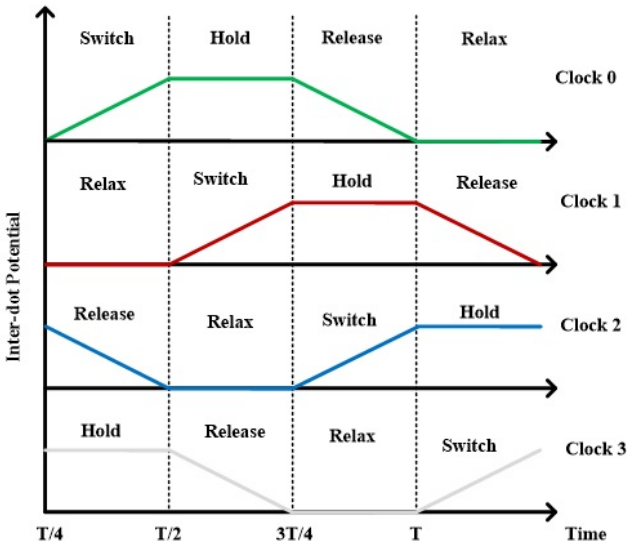


Figure 3. QCA clocking phases.

method, it is necessary to use two separate QCA clocking regions that are separated by a phase delay of ninety degrees. By utilising three separate clocking zones, it is feasible to design a consistent three-input majority gate [7, 8]. In a sophisticated majority gate with three inputs, the inputs are positioned during first clocking region, the QCA cells in the middle of the gate that are responsible for producing the outputs are located in the second clocking zone, and the clocking region in which the output wire is located in the third one [7, 8]. It is essential to be aware that there is a phase mismatch of 90 degrees between the clocking zones.

The QCA timing concept may be applied by utilising four-step monitoring over the four clock zones (switch, hold, release, and relax). A 90-degree phase shift is used to synchronise a QCA system's phases. During the transition phase, electrons are able to move across sites. According to the bias, a cell can only polarise its neighbour cell. Cell polarity is lost throughout the launch and relaxation stages. A QCA circuit can operate better by following a few rules for applying clock signals [9].

The purpose of this research is to come up with an efficient layout for a QCA memory cell that has set/reset capabilities. The proposed design is based on the criteria for creating a reliable QCA circuit using the QCA clocking requirements. It also features a simple and durable construction that eliminates the necessity for a crossover wire and has these other characteristics.
In a nutshell, the following are the paper's significant contributions:

- Design a 2:1 multiplexer and connect identical building pieces utilised in RAM cell modules.
- Optimized single-layered RAM cell design with set/reset capacity.
- Using the QCADesigner tool, verify the operation of the suggested design.
- Compare the suggested designs with state-of-the-art designs, and assess the parameters like cell count, delay, and area covered.
- Using the QCAPro tool to analyse and figure out the dissipated energy of the circuit.

The remaining parts of the paper are organized in the following way: The memory cells that are proposed earlier, i.e. the existing QCA RAM designs are highlighted in Section 2. Section 3 involves the newly suggested RAM layout using a simple multiplexer. This multiplexer has been recommended in the past, and it is now being considered to design the proposed RAM structure. In Section 4, the outcomes of the simulations as well as the assessments of the suggested structure have been discussed. The investigation of the power dissipation of the multiplexer that is based on the QCA RAM architecture is discussed in Section 5. The conclusion is included in Section 6 of this article.

2. Study of related work on RAM cell

Memory stores data and instructions in the same way that a human brain does. Memory is a quick access place for data in a computer, where data processing and essential instructions are located. Cells in memory are made up of unique addresses ranging from 0 to M_{S-1}, where M_{S-1} refers to memory size minus one. A machine with 64k words, for example, has $64 \times 1024 = 65{,}536$ memory locations. The address for these places ranges from 0 to 65,535.

The architecture of RAM cells is among the greatest interesting topics that may be researched in QCA. In the literature of QCA, there have already been a few publications that make use of a range of methodologies. In [10–14], these methodological approaches are discussed. The mode of operation of the QCA circuits that RAM cells are a part of determines whether those cells are considered to be loop-based [10–14] or line-based [15–17] in the RAM cell classification system. A line-based structure aims to provide a bidirectional signal transmission, which is accomplished by transporting data in both directions across a line. The need for additional clock zones makes deploying line-based memory cells more difficult. Loop-based memory cells store QCA-system data bits and do not need additional clock regions [11].

Since there will be a detailed discussion on the earlier works suggested in [12–14] across the coming few paragraphs, it is important here to also provide a discussion on [15–17], albeit in a more brief fashion. The authors in [15] proposed to use a line-based parallel RAM circuit. It is a two-dimensional design that uses three clocking zones and a total of nine gates, two of which are majority gates. In [16], a new and enhanced architecture of line-based memory that makes use of QCA is created. The RAM that is recommended made use of two parallel clock zones for each memory cell, and it is composed of a total of six gates. In [17], a basic memory cell is constructed with 158 cells and a loop. It is a two-dimensional construction that makes use of eight gates, and it is anticipated that it will have a capacity of $1.6 Gbit/cm^2$.

Let us take a look at a few other recent studies [18–22] as example. An implementation of a RAM cell using a D-latch and a loop is described in 2019 [18]. It used a total of eight gates without using a coplanar wire crossing. To facilitate the design of effective single-layer QCA-based circuits, the authors in [19] propose a novel D-latch-based nano-scale RAM cell in the same year (2019). In this case, seven gates have been used. As a note, D-latch is among the leading possibilities for the creation of loop-based structures in RAM cell designs such as [18] and [19]. The method for storing information involves continuously sending a set of information around a QCA cell that uses a closed-loop configuration. In 2020, it was projected that random access memory cells might be modularized using QCA-multilayer structures [20]. In this work, stacked basic modules that allow for reading, writing, setting, and resetting the contents of a random access memory cell are available. These include the XOR gate, 2:1 multiplexer, and D latch. In 2022, a novel random access memory cell that included both set and reset capabilities is suggested [21]. It used two 2:1 multiplexers and loops altogether. The 'Select' signal

governs how the proposed RAM operates, allowing either a 'Set/ Reset' action or a 'Read/Write operation to be carried out, by activating any one of them. Very recently (2022), an efficient loop-based memory with a 2:1 multiplexer and a three-input majority gate was constructed [22]. Data, read/write, and enable are the three input types. The input read/write is employed as a multiplexer selector line, and a majority gate with three inputs is responsible for producing the final output.

Here, a few significant designs, including the QCA layouts, are illustrated in detail to provide the reader with a thorough understanding. In [12], a QCA RAM that did not include a set/reset feature was suggested as shown in Figure 4. An SR-latch provides the foundation for the loop-based technique that is depicted in Figure 4a. The input, read/write, and select cells all serve as input cells inside this method. If select = '1' and read/write = '0' are both true when a read operation is started, the contents of the RAM cells will not get damaged even if the RAM cells are read many times. The process of writing is kicked off when select = '1' and read/write = '1,' and the newly added item is the one that gets written to the output. Figure 4b provides an illustration of the QCA configuration of the internal structure of the RAM cell. Another second arrangement of RAM layout presented in [12] is described in Figure 5; Figure 5a is the schematic and Figure 5b is the QCA layout.

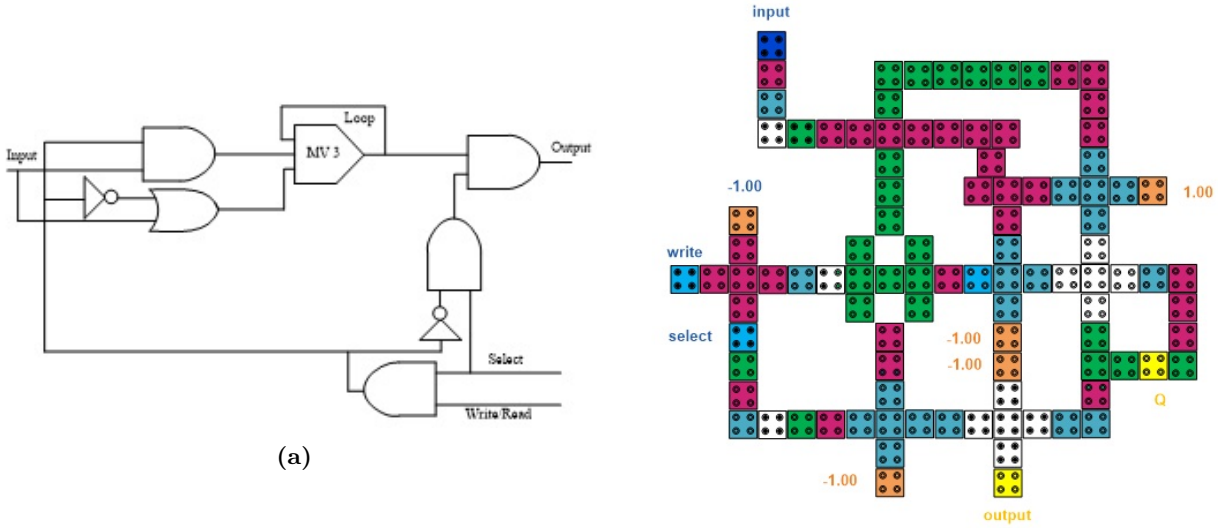
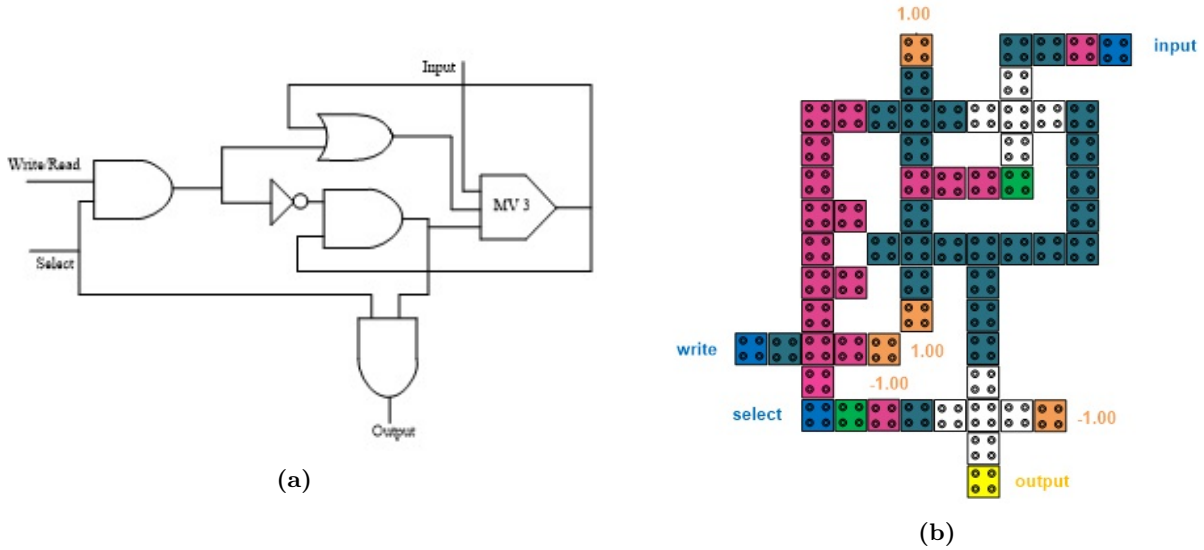


Figure 4. The RAM cell structure-1 as suggested in [12]: (a) Schematic, (b) QCA layout.

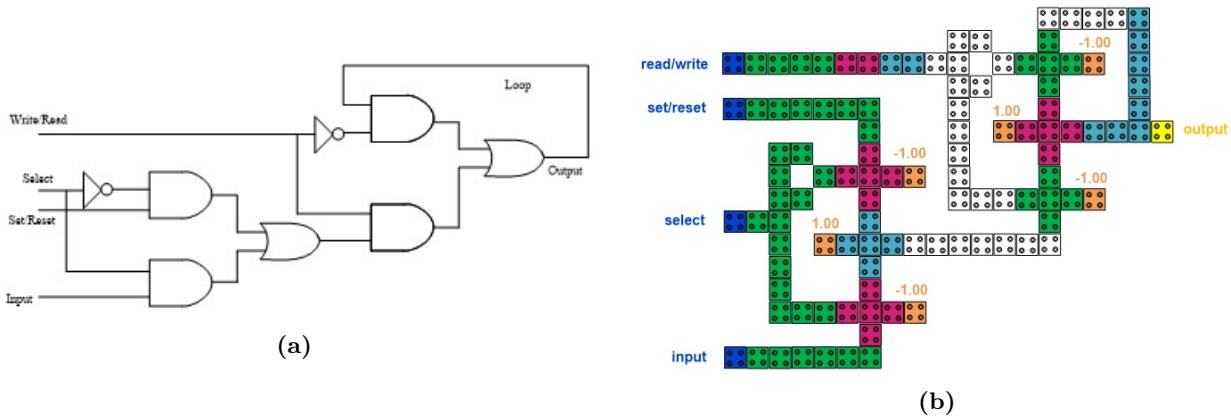
As shown in Figure 6, a loop-based configuration with two 2:1 multiplexers has been presented [13]. These multiplexers combined the output signal at the input of the first multiplexer, acting as a D flip-flop, depicted in Figure 6a. D flip-flop output stays fixed whether read/write = 0 or 1, but it may be altered with fresh input or set/reset instructions. If select is equal to '0,' then the set/reset signal will be transmitted to the output. The newly generated input signal is sent to the output whenever selections = '1.' The QCA architecture of the RAM cell structure is shown in Figure 6b.

According to the information presented in [14], a QCA RAM that is managed by the independent signals 'Set' and 'Reset' is recommended. Based on the loop structure, the suggested design comprises three majority gates with three inputs each and one majority gate with five inputs. Select(SL) = 1 starts the write operation



(a) (b)

Figure 5. The RAM cell structure-2 as suggested in [12]: (a) Schematic, (b) QCA layout.



(a) (b)

Figure 6. The RAM cell structure as suggested in [13]: (a) Schematic, (b) QCA layout.

by the information being sent from input to output, and the read/write mode has been set to 1. It also sets the mode to 1. Read/write (RD/WR) should be set to '0' and select to '1' to start reading. Regardless of the status of SL and RD/WR signals, the contents of the RAM will be set to either '1' or '0' based on the exact set/reset signals that are sent to the RAM. Figure 7 (Figure 7a is the schematic and Figure 7b is the QCA layout) depicts one potential architecture for a QCA RAM cell, which would allow the contents of the cell to be 1 or 0 from memory.

3. Proposed layout of RAM cell

As illustrated in Figure 8, the suggested RAM cell is built using the previously reported 2:1 multiplexer (MUX) [23] layout, where the schematic is depicted in Figure 8a and the QCA layout is displayed in Figure 8b. Figure 9 provides a visual representation of the design that has been proposed. The schematic design of a QCA memory cell may be seen in Figure 9a. The proposed RAM cell comprises two two-input multiplexers, with

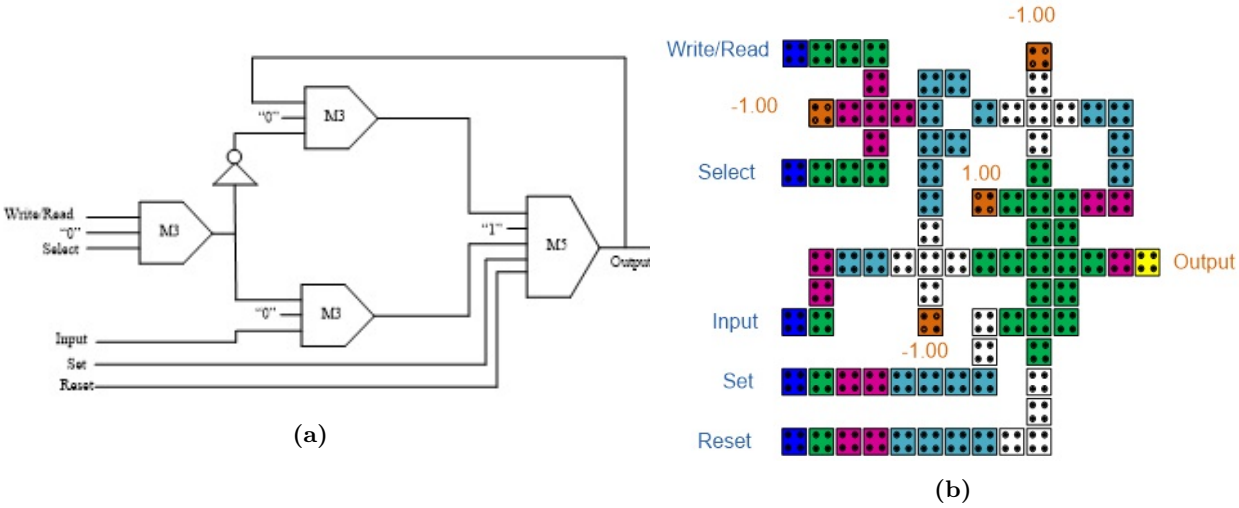


Figure 7. The suggested RAM cell in [14]: (a) Schematic, (b) QCA layout.

the set/reset and input signals serving as MUX-1's two inputs and MUX-2's output, combining with the circuit feedback to the input serving as MUX-2's two inputs. The chosen signal serves as the design's select line, while the read/write signal is utilised to send data to a MUX-2, which controls its functioning.The configuration of the improved QCA cell that has been suggested may be seen in Figure 9b. Table 1 is an illustration of the functionality of the newly proposed QCA memory cell, which includes the ability to set and reset. In the table, values that are not significant are represented by the symbol '×,' while the value 'out(t-1)' is used to denote the value that the circuit had before.

Figure 8. The 2:1 multiplexer as suggested in [14]: (a) Schematic, (b) QCA layout.

When RD/WR is equal to zero, the value of the circuit does not alter in any way. However, the circuit's value does change when read/write = '1'. When this occurs, the set/reset signal is communicated either as the new input or output. The value of the circuit does not shift in any form when RD/WR is equal to zero. When 'read' and 'write' both equal '0,' as they always do, the value of the circuit does not alter in any manner. The output is the one that takes in the set/reset signal if the 'select' variable is equal to '0.' On the other hand, the output is the one that gets the new input if 'select' is equal to '1.' In this particular scenario, the outcome is the one that receives it. In order for QCA circuits to work correctly, it is absolutely necessary for the input signals to be precisely synchronised with one another. The suggested RAM cell included additional clocking zones with the read/write to obtain the input signals, taking into account the synchronisation needs. As a result, mux-1's

output and read/write signals have the same latency when they arrive at mux-2.

Table 1. Logic table of the proposed memory cell.

Write/Read	Select	Set/Reset	Out(t)
0	×	×	Out(t-1)
1	0	0	0
1	0	1	1
1	1	×	Input

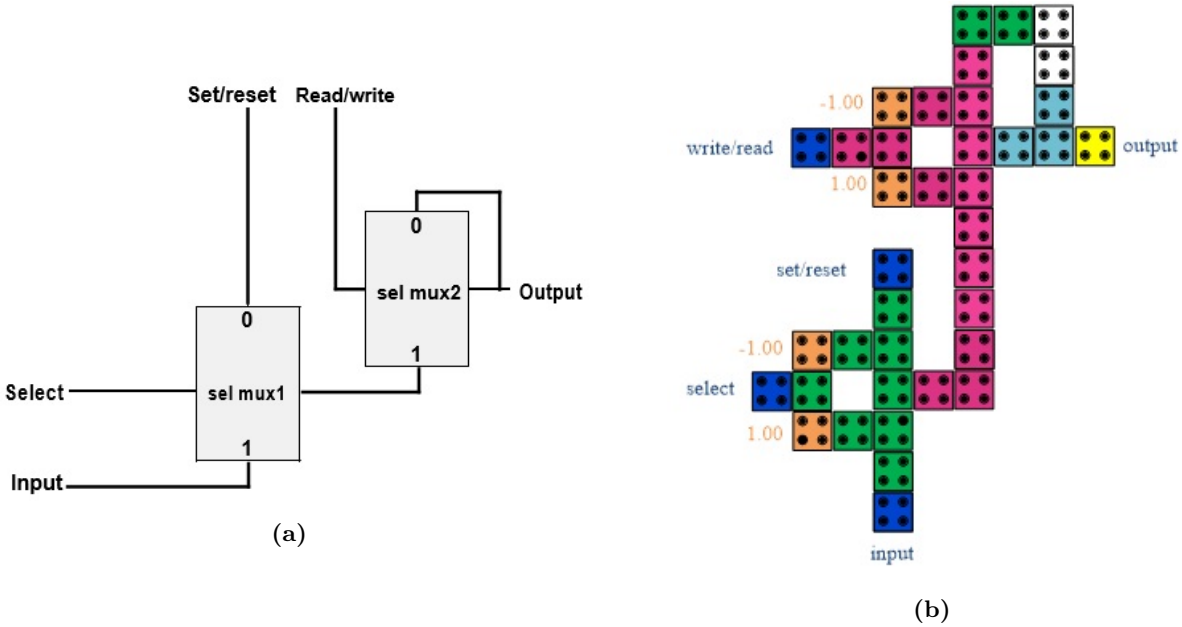


Figure 9. The newly proposed QCA memory cell of this work: (a) Schematic diagram, (b) QCA design.

4. Simulation results

To simulate of the proposed QCA RAM cell, version 2.0.3 of QCADesigner is used. The simulation output of the proposed layout is depicted in Figure 10. This output may be used to verify the occurrence of the desired outcome at any given moment in time. After the passage of one clock cycle, the set/reset value is then sent to the output when the signal being monitored is '0.' This occurs after the clock cycle is complete. This demonstrates that the procedures of setting up and resetting have been completed, and that the proposed circuit has a lag time that is equivalent to one CLK cycle. This also shows that the lag time is equivalent to one CLK cycle. When both the select signal and the read/write signal are enabled ('1') at the same time, the beginning of the write operation occurs whenever the input signal is transferred to the output after a clock cycle has passed following the simultaneous enabling of the select signal and the read/write signal. This occurs after one clock cycle has passed after the two signals have been enabled simultaneously. This occurrence takes place anytime both the select signal and the RD/WR signal have their respective enable bits set. This may take place whenever both signals have their enable bits set. The read operation may start after the selected signal

has been set to '1,' and the RD/WR signal has been assigned to '0'. After completing one CLK, the output is present instantly before it is sent to the output, which is considered a result. After the select signal is '1' and RD/WR is '0,' the read operation may commence. This kicks off the reading process in its proper manner.

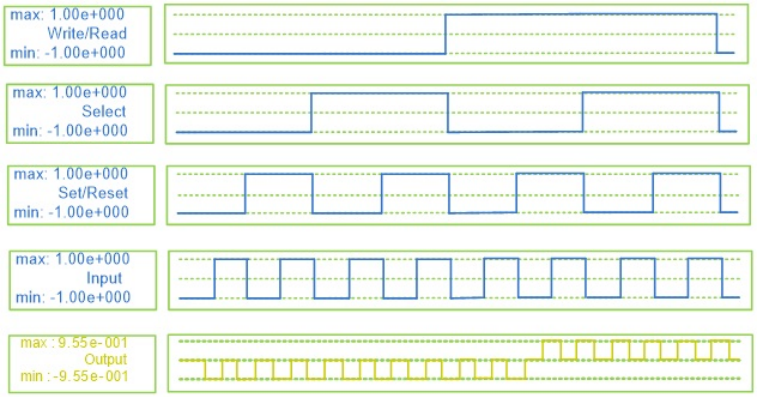


Figure 10. Simulation output of the proposed RAM cell.

Table 2 presents the findings of a comparison between the RAM cell layout that has been shown and more conventional designs. The cell count, area, latency, and kind of wire-crossing are all included in this table, along with a number of fixed variables. The results of the research show that the suggested layout is superior to the previous designs presented in [12–14, 17–20] regarding cell count, occupied space, and clock delay .

Table 2. Design parameters comparison of the proposed design and existing designs.

Year	Work	Cell count	Occupation space (μm^2)	Latency (CLK cycle)	Coplanar wire crossing	Number of constants values ('+1' and '–1')
2011	Design-1 [12]	100	0.11	3	Yes	5
2011	Design-2 [12]]	63	0.07	2	No	4
2012	[13]	109	0.13	1.75	No	6
2015	[14]	88	0.08	1.5	No	4
2003	[17]	158	0.16	2	Yes	6
2019	[18]	55	0.06	2.25	Yes	5
2019	[19]	87	0.12	1.5	No	7
2020	Design-1 [20]	73	0.07	1.75	Yes	6
2020	Design-2 [20]	60	0.056	1.75	Yes	6
2023	Proposed	38	0.04	1	No	4

5. Analysis

5.1. Power dissipation

During an input switching operation, a QCA circuit is analysed using QCAPro in order to determine the greatest amount of power loss, the average amount of power loss, and the smallest amount of power loss. Users of QCAPro are given the ability to choose their preferred temperature settings and calculate the maximum

power that can be utilised in QCA circuits as a function of the cell polarisation and clock energy levels. For each input vector, QCAPro may create a polarisation map of the QCA circuit. To construct a map for different input vectors, repeat this method several times. Some researchers used the QCAPro tool to determine the power waste [24, 25]. This paper used QCAPro to assess the proposed structure's energy usage. The QCAPro tool presently uses the QCADesigner [26] generated drawing file. QCAPro can do a rapid project check using this design file to determine the output value for all possible input combinations. A Hamiltonian matrix is applied to determine the total energy and power of a QCA cell. Using Hartree-Fock and assuming Coulomb interaction using a mean-field technique, the Hamiltonian matrix ($\widehat{H_i}$) for QCA matrix cells is obtained as (1) [25, 27, 28].

$$\begin{aligned}\widehat{H_i} &= \begin{bmatrix} -\frac{E_K}{2}\sum\limits_{j\neq i} C_j f_{i,j} & -\gamma \\ -\gamma & +\frac{E_K}{2}\sum\limits_{j\neq i} C_j f_{i,j} \end{bmatrix} \\ &= \begin{bmatrix} -\frac{E_K}{2}(C_{i-1}+C_{i+1}) & -\gamma \\ -\gamma & +\frac{E_K}{2}(C_{i-1}+C_{i+1}) \end{bmatrix}\end{aligned} \tag{1}$$

Here $\sum\limits_{j}$ is the summation over the total cell numbers, H_i denotes the Hamiltonian of the i^{th} cell, $f_{i,j}$ denotes the geometric component that determines the electrostatic interaction between i^{th} cell and j^{th} cell depending on geometric distance, C_j is the polarisation of the j^{th} cell and, γ=the tunnelling energy between two states of a cell, and it is managed by the clocking process. $(C_{i-1}+C_{i+1})$ is the summation of neighbouring polarisations. E_K is known as kink energy of cells. Kink energy can be expressed as (2):

$$E_{i,j} = \frac{1}{4\pi\varepsilon_0\varepsilon_r}\sum_n\sum_m \frac{q_{i,n}q_{j,m}}{|r_{i,n}-r_{i,j}|} \tag{2}$$

For every clock cycle, the expectation value of QCA energy is expressed as (3):

$$E = \langle\widehat{H}\rangle = \frac{\hbar}{2}.\vec{\Gamma}.\vec{\lambda} \tag{3}$$

Here, the average of any observable of interest in this QCA system is the Hamiltonian $\langle\widehat{H}\rangle$, $\hbar$ is the reduced Planck constant, $\vec{\lambda}$ is the coherence vector, and $\vec{\Gamma}$ is the energy environment vector. In quantum-dot cellular automata (QCA) systems, the quantum state of the system is described by coherence vectors. The coherence vector ($\vec{\lambda}$) represents the superposition of QCA cells' charge states and phase interactions. Precisely, the components of the coherence vector for a QCA device with N cells indicate the amplitudes of the various polarization configurations that the QCA system is capable of adopting. The energy of the QCA system may be computed using the coherence vector and the Hamiltonian matrix ($\widehat{H_i}$). As a note, the QCA system's energy levels and cell-cell interactions are described by the Hamiltonian, depicted in (1). Another representation of the Hamiltonian vector corresponding to Hamiltonian (1) is shown in (4).

$$\vec{\Gamma} = \frac{1}{\hbar}[-2\gamma, 0, E_K\overline{C}] \tag{4}$$

Here $\overline{C} = C_{i-1} + C_{i+1}$ = addition of the polarisations of neighbouring cells.
The expression of the instantaneous power is shown in (5) below:

$$\begin{aligned} P_t &= \frac{dE(t)}{dt} \\ &= \frac{\hbar}{2}[\frac{d\vec{\Gamma}}{dt}.\vec{\lambda}] + \frac{\hbar}{2}[\vec{\Gamma}.\frac{d\vec{\lambda}}{dt}] \\ &= P_1 + P_2 \end{aligned} \tag{5}$$

The quantity P_1 is derived from (5) and has two primary parts: the first part, P_{in-out}, which is the power gain resulting from the difference between the intensities of the input and output signals, and the second part, P_{lock}, which is the synchronisation power supplied to the cell. Additionally, the term P_2 denotes the power that has been lost, i.e. P_{diss}. The power dissipation model of the upper limit (P_{diss}) is described in [24, 29]. Note that P_{diss} depends on temperature, T, and is related to k_B which stands for the Boltzmann constant.

Even though the model provided for each QCA cell is the same, the overall power consumption can be determined by adding up the power lost by all of the cells contained within similar QCA matrix cells. Three distinct amounts of tunnel energy ($0.5E_K$, $1.0E_K$, and $1.5E_K$) at a temperature of $2K$ have been used to compare the new design to the earlier constructions. Darker thermal connection paint colours indicate high-power dissipation cells. The suggested structure and the existing designs are contrasted with regard to the overall amount of energy lost in Table 3, where it is further broken down into the energies spent during switching and dispersion. It is quite clear that the proposed layout significantly cut down on the amount of electricity that was lost. The energy dissipation map of the QCA RAM cells at $2K$ temperature with $0.5E_K$ is shown in Figure 11. The darker cells in this diagram dissipate the most energy. The inputs are represented by the white cell. By simulating the suggested RAM cell in QCADesigner 1.0.1 platform, this thermal layout was obtained in the QCAPro tool. It should be noted that QCAPro is only compatible with older versions of the QCADesigner tool.

Table 3. Energy loss comparison of the proposed and existing designs.

Works	Leakage energy loss (meV)			Switching energy loss (meV)			Total energy loss (meV)		
	$0.5E_K$	$1.0E_K$	$1.5E_K$	$0.5E_K$	$1.0E_K$	$1.5E_K$	$0.5E_K$	$1.0E_K$	$1.5E_K$
Design-2[12]	20.00	60.00	100.0	90.00	80.00	70.00	110.0	140.0	170.0
[12]	20.00	70.00	130.0	100.0	90.00	80.00	120.0	160.0	210.0
Proposed	11.00	33.00	55.00	23.00	21.00	18.00	34.00	54.00	73.00

5.2. Practicality and fault tolerance

Estimating the actual speed performance of the suggested architecture is challenging because the physical implementation of QCA is still in the early stages of development. However, it is anticipated that the suggested RAM may reach a speed of 1 THz in accordance with the potential capability of QCA technology. The number of clocks required to write and read the identical data bit at the output can be used to evaluate performance. The suggested RAM cell sends data from the input to the loop throughout the course of one complete clock

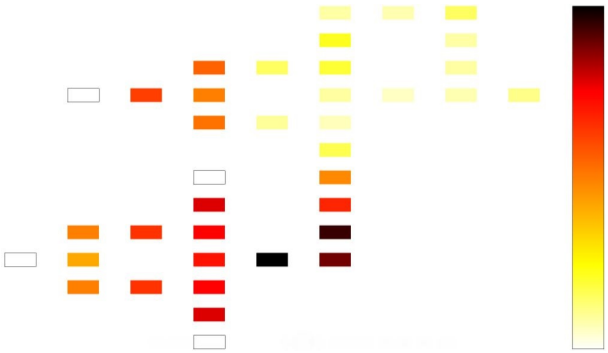


Figure 11. Energy hotspots for the proposed structure with $0.5E_K$.

cycle. The information exits the loop on the following clock cycle. As a result, information transmission uses two full clocks. For higher-order RAM configurations, more clocks are needed. As a result, for each QCA circuit, the delay grows as a function of the employed clock number along its longest path. Due to the varying timings at which the signals arrive at the output, it creates another simulation issue. To fix this problem, a designer should include duplicate clocking zones on shorter pathways in the scheme. The information could be delivered to the output concurrently if this is done.

A fault might be the cause of the asymmetry in the size and placement of the dots inside a QCA cell. The reaction between cells cannot repair the defect if the asymmetry is large. There is a probability to obtain a valid signal if the asymmetricity of two subsequent cells is positive and negative with the same magnitude. Numerous related faults may appear concurrently at interconnects during manufacture. Even when the tolerance for defects decreases, it still has an impact on the result. Unfortunately, there is currently no clear understanding of the final QCA implementation process, and as a result, the allowable tolerance range is likewise unknown. Algorithmic level thinking may raise the fault tolerance level of QCA designs as a higher-level solution technique.

6. Conclusion

This study suggests a novel resilient random-access memory (RAM) cell design. This architecture is based on two 2:1 multiplexers built without coplanar crossover, and it is capable of both production and recovery of data. Using the QCADesigner tool, the simulations of the recommended memory cell are carried out. The power dissipation induced by the recommended design is evaluated using an effective power approximation tool provided by the QCAPro simulator environment. The simulation results revealed that the anticipated outputs are successfully produced. The proposed QCA RAM cell design showed an effective and efficient structure when evaluated according to the criteria of needed area, latency, complexity (i.e. the number of cells), and energy consumption. The suggested approach decreases cell count by 40%, area requirements by 43%, and latency by 50% compared to the best existing design. These proposed blocks and methodologies might be useful in constructing future nanoprocessors and other higher-order circuits. The suggested memory circuit based on QCA can be expanded upon in the future to include other features, such as fault analysis. This straightforward RAM cell has the potential to be utilised in the construction of higher-order memory cells as well as content-addressable memory cells in the future, which will ultimately contribute to the development of a central processing unit. In addition, future studies may examine memory circuit designs based on magnetic QCA, which can reduce the number of gates used.

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