Analysis and implementation of a new high-buck DC-DC converter with interleaved output inductors and soft switching capability

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Abstract: This paper proposes an innovative structure for DC-DC converters with high buck gain by using a lower number of elements. The converter provides highly efficient output power and an extended output voltage range. In addition, the distribution of output current between two inductors and the soft-switching capability of the power switches have made the converter suitable for applications that require high output current. All power switches accomplish the ZVZCS (zero-voltage and zero-current switching) condition with the aid of a small auxiliary inductor (Lx), which charges and discharges parallel capacitors of main switches to provide soft-switching conditions. Thus, the switching losses associated with power switches are considerably reduced. Additionally, the output voltage ratio of the proposed converter can be changed by varying the switching frequency and duty cycle. In addition, the variation range of output voltage has been expanded compared to other topologies, allowing for a wider output voltage range. A coupled inductor is utilized to establish a relationship between the output gain and the turn ratios, resulting in a wider output voltage gain range. Eventually, a theoretical analysis is conducted and a 200-watt experimental prototype has been implemented to illustrate the proposed converter's efficacy. It converts a voltage input (300 V) to a voltage output (10 V).

Key words: Buck, DC-DC converter, nonisolated, dual switches, voltage stress

1. Introduction

Recent applications have employed DC/DC buck converters with a high exchange ratio of voltage, a low output voltage, and a high output current. Voltage regulator modules on computer CPU boards, LED lights, uninterruptible power supplies (UPS), hybrid electric vehicles (HEVs), and even low-voltage output battery chargers are the most common applications for these converters [1–3]. Buck converters are afflicted by conduction and switching losses, excessive voltages on semiconductor components, massive contemporary ripples, and a lower efficiency than the regular performance of the converter. Researchers are working on a range of low-voltage DC-DC converters that can handle high-current DC loads [4]-[15]. In order to recover the lost energy in the tapped inductor converters, the TI step-down converter possesses a no-loss clamp circuit that passes it to the output [4]. Additionally, using a tapped inductor (TI) and the new architecture described in reference [5]. It is possible to increase the duty cycle while decreasing the voltage gain. This structure's primary flaw is the stored energy in the coupled windings' leakage inductance, which causes large voltage spikes on the power switches and a decrease in efficiency. However, these converters are not suitable for high buck voltage usage.

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In reference [6], a novel high step-down DC-DC converter without a transformer is presented. The converter has interleaved output and low-voltage stress on the semiconductors, but it has hard switching and a large number of components. In addition to this, the ground for the input and the output are not the same. There are a reasonable amount of components in the converter, and soft switching is applied for power switches. Nevertheless, it uses a coupled inductor at the input and a transformer at the output, and the gain is not suitably reduced. The converter has four power switches with a total standing voltage of 2.66 Vin and needs four gate driver circuits. The authors in [7] and [8] propose two buck converters that take advantage of the series clamp capacitor and the TI method. The extended duty cycle and the spikeless switches are the advantages of these converters, but these topologies undergo the high stress of voltage on the key switch and discontinuous output current. A new semiquadratic buck converter, presented in [9], provides a high buck ratio without a transformer. This converter has a simple topology and a lower gain than the traditional buck converter. Because of the high voltage stress on the switches, hard switching, and a single inductor at the output, it is not suitable for applications requiring significant output current. In reference [10], an innovative, few-component, DC-DC converter with a high-step-down feature is given. Even if the number of elements is reduced, the increased stress on the semiconductors, the larger output voltage ripple, and the restricted range of output voltage variations are downsides of this converter. An alternative solution to the problem of voltage stress has been given in [11] by using a quadratic buck converter. This converter utilizes only one active switch and can step up or down the input voltage, while the existing single-switch quadratic buck/boost converters can only work in step-up or step-down mode. In addition, buck converters with switched capacitors are another way to provide high buck ratios [12]. Some strategies for limiting the maximum switching voltage of nonisolated 3-level buck converter structures are being investigated [13,14]. These topologies also benefit from lowering the size of the output filter and current ripple. The voltage gain of these converters, on the other hand, is the same as that of regular buck converters, so they cannot be used for high-buck applications. The authors in [15] propose a series-capacitor buck converter. The series-capacitor buck converter increases the duty ratio and equalizes the current. Adding a resonant tank to Cs creates a series resonator buck converter. Low-side switches are deactivated with zero voltage, whereas high-side switches are activated. Moreover, the increase in voltage stress on low-side switches occurs due to the resonant tank. Interleaved buck converters can reduce current ripples, and the modified version is proposed in [16]. The number of elements is also another parameter which affects DC-DC converter efficiency, reliability, volume, and implementation. A new DC-DC topology with a significant buck ratio is proposed in [17]. It has six power switches, and accordingly, six gate drivers will be needed, and also it makes the control of the converter complex. In addition, the converter's input and output are no longer connected. The converter gain is equal to D/6, so to obtain very low voltage gains such as 0.03, the duty cycle should be about 18%, resulting in lower efficiency. In comparison, the proposed converter in this paper works with D = 50% at every load condition. The authors in [18] propose another new DC-DC converter with a high step-down output ratio. The voltage gain of the converter at the duty cycle D=0.5 and with a turn ratio of 1/2 is about 0.16. The high step-down converters should have a very low output voltage ratio with suitable efficiency. The low output voltage can be used to power a low voltage DC motor or to power CPUs or electronic devices. Therefore, even though this converter has a suitable efficiency and a low number of components, its output voltage gain is unsuitable for applications requiring a high input voltage. The 300V input voltage can be changed to 48 VDC with this converter, but the proposed converter in this paper can reduce that to very low voltage ranges to be used as a voltage regulator module. Another structure for a high-buck DC-DC converter is proposed in [19]. The minimal number of components and high voltage gain of D^2 with two power switches

make this converter a suitable choice. However, similar to ref [18], this converter should work at a very low duty cycle (about 17%) to obtain 0.03 of output voltage gain. The critical disadvantage of this converter is the output current quality and the lower amount of current delivery to the output. This converter has a diode and a switch at the output, so the output capacitor size should be large enough to have a suitable DC current at the output. Moreover, the lack of interleaved structure in the output current delivery results in lower current handling capability. Thus, it is important to design and propose a converter that can better solve the problems listed above. This research proposes a new high-buck, nonisolated DC-DC converter that uses a two-stage buck converter with an interleaved output to share current between the output inductances and reduce output current ripple. The presented converter has only one auxiliary inductor to achieve soft switching for all semiconductor elements. Moreover, the converter has very low switching losses because of the ZVS and ZCS conditions for semiconductor elements obtained with the combination of leakage inductance and an auxiliary series inductor (Lx). Furthermore, switching frequency or duty-cycle variations could control the output voltage gain. Using the turn ratio (n), a two-winding coupled inductor is used to provide an appropriate output voltage gain variation range. However, the output voltage variation area is enlarged with the switching frequency control, turn ratio (n), and the small coupled inductor. Using a phase shift between the output inductor's currents, the voltage and current ripples are reduced at the output. However, the converter's maximum gain is D/n, where n equals N1/N2. In addition, a lower gain can be attained by adjusting the switching frequency, resulting in a broader output voltage control range. This article has five sections: introduction, converter operation principle, steady state analysis, design and theoretical comparison, and experimental results and conclusions.

2. The fundamental working principle of the proposed converter

Figure 1a depicts the proposed high step-down soft-switching DC-DC topology. The converter consisted of two main switches (S_1 & S_2) that receive complementary signals including a short delay (t_d). (L_x) is employed to achieve the ZVS state for power switches, while C_{x1} & C_{x2} serve as blocking capacitors. Three power diodes (D_1, D_2 & D_3) provide the output power of the converter. In addition, a two-winding coupled inductor containing a magnetized inductance (L_m) and the turn ratio (n) is utilized to have a wide range of output ratio and to reduce the output voltage gain. Besides that, the leakage inductance and L_x are combined. In this case, the inductors L_{o1} and L_{o2} act as output current filters, while C_o is defined as the output voltage filter capacitor.

The converter essential waveforms are depicted in Figure 1b, which gives an overview of the operating modes of the converter. The following assumptions are considered in this article for the analysis of the converter: 1- Ideal for all semiconductor components, 2- The output current I_o, output voltage V_o, and input voltage V_{in} remain constant throughout the switching cycle, 3- The inductance value of L_{o1} and L_{o2} are the same, 4- the capacitors have been selected sufficiently large to be considered a fixed voltage source. The magnetization inductance of the coupling inductance is so big that the magnetization current can be disregarded. Modes (1 to 8) of the converter for operation in continuous conduction mode (CCM) are shown in Figure 2.

Mode1- (t_0 to t_1) [Figure 2a]: At the start of this mode, the flowing current through the body diode of S_1 reaches zero, and the power switch S_1 is turned on. Furthermore, the voltage (V_{in}-C_{x1}) is supplied to the auxiliary inductor L_x, and its current flow is raised linearly. The capacitor C_{x2} is fully charged in this mode. The output diode D_1 is turned off and the current through diodes D_2 (I_{D2}) and the diode D_3 are linearly increased and decreased respectively. The current through the diode D_3 reaches zero at the end of this mode and then it is turned off. In addition, output inductors L_{o1} and L_{o2} demagnetize and supply the output load.
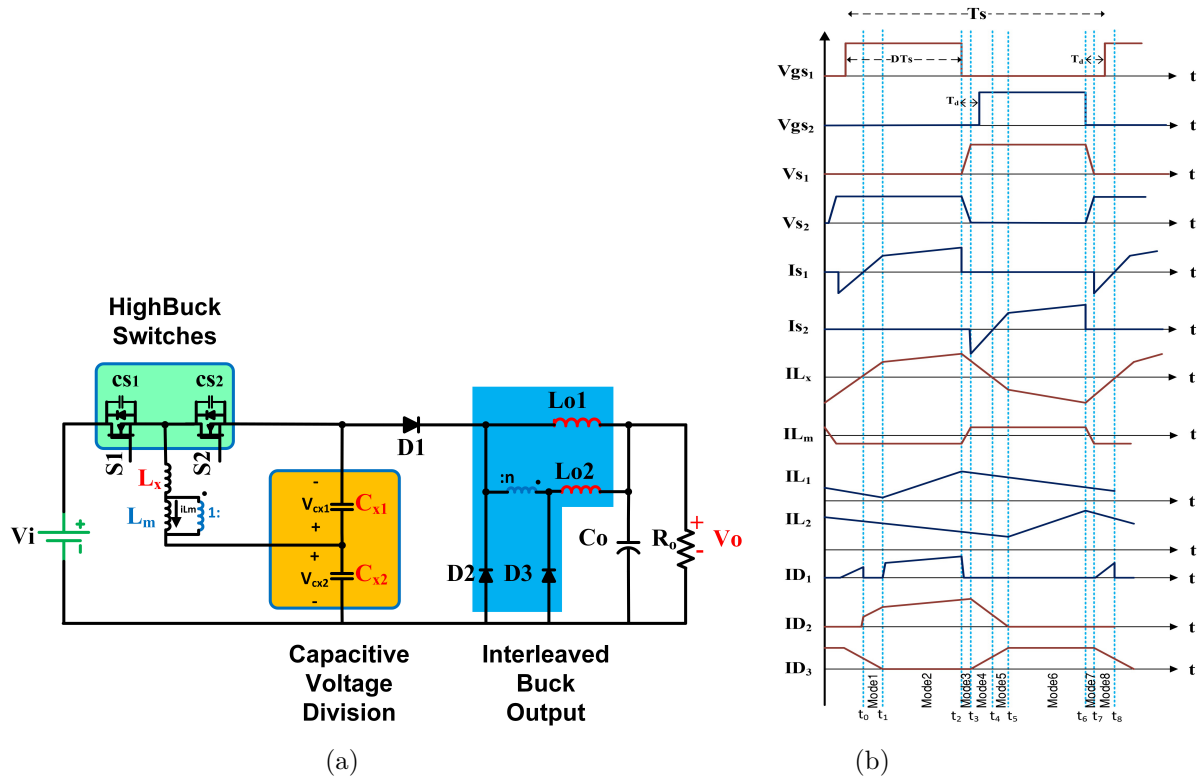
Figure 1. (a) Equivalent circuit diagram of the proposed converter, (b) Fundamental operating waveforms of the proposed converter.

For this mode, the following equation can be written as follows, where Δt_0 is (t-t_0):

$$i_{Lx} = \frac{(V_{in} - V_{cx1})}{L_x}\Delta t_0. \tag{1}$$

Mode2- (t_1 to t_2) [Figure 2b]: In this state, the power switch S_1 is kept switched on. The diode D_1 is once again turned on till the conclusion of this mode. The diode D_2 is still active with an increasing current flow. The diode D_3, which is switched off at t_1 in response under the ZCS condition, remains off. In the meanwhile, the output is supplied by the D_1 and coupled inductor through the D_2 diode. In addition, L_{o1} and L_{o2} are magnetizing and demagnetizing, correspondingly. Additionally, the magnetizing current passing through L_m is negative. However, the equation below can also be expressed in this mode:

$$i_{Lx} = i_{Lx,t1} + \frac{(V_{in} - V_{Cx} - V_{Lm})}{L_x}(t - t_1). \tag{2}$$

$$ni_{Lx} = i_{Lo2} \tag{3}$$

Mode3- (t_2 to t_3) [Figure 2c]: During this time, the magnetizing current direction of the coupled inductor changes from negative to positive. Also, the current through the power switch S_1 falls to zero, and then the voltage across it rises with a positive slope. It occurs due to the charge of the parallel snubber capacitor C_{s1}, which provides ZVS turn off for power switch S_1. In details, the parallel capacitors of the power switches S_1

and S_2 (C_{s1} and C_{s2}) voltages are started to be charged and discharged, respectively. The discharge of the snubber capacitor(C_{s2}) provides the necessary preparations for the power switch S_1 to be turned on at ZVS condition. Here is how the duration of this mode can be calculated:

$$t_3 - t_2 = \frac{V_{in}}{I_3}C_{s1} = \frac{V_{in}}{I_3'}C_{s2}, \tag{4}$$

where I_3 and I_3' are the average current values of L_x and L_{o2} at t_2, correspondingly. This mode finishes when $V_{s1} = V_{in}$ and $V_{s2} = 0$.

Mode4- (t_3 to t_4) [Figure 2d]: The power switch S_1 is turned off throughout this mode. The antiparallel body diode of the power switch S_2 is turned on. As it is known in the previous mode, the voltage across switch S_2 was zero and the conducting of the diode S_{s2} provides zero current state for the switch. Consequently, the power switch S_2 can be turned on at the ZVZCS condition at the start of the next working mode (mode5). Additionally, for circuit inductors, the currents flowing through the output inductors (L_{o1} and L_{o2}) as well as the input auxiliary inductor (L_x) are linearly demagnetizing. In addition, the current through the magnetizing inductor is still flowing in a positive direction; however, since diodes D_2 and D_3 are conducting, the voltage across the magnetizing inductor reaches zero. The following equation can be obtained from this state:

$$i_{Lx} = i_{Lx,t4} + \frac{(V_{Cx1})}{L_x}(t - t_4). \tag{5}$$

Mode5- (t_4 to t_5) [Figure 2e]: This mode starts at t_4. In this mode, the S_2 switch is turned on under the ZVZCS condition. The state of the current passing through the auxiliary inductance is altered to negative. Additionally, the voltage across the magnetizing inductance is still zero due to the conduction of diodes D_2 and D_3. At the end of this interval, the current through the diode D_2 decreases to zero and the current through the diode D_3 achieves its maximum value. In addition, the output inductors L_{o1} and L_{o2} are still demagnetizing. However, this mode finishes when the current via the output inductor I_{Lo2} reaches nI_{Lx}.

Mode6- (t_5 to t_6) [Figure 2f]: Within this mode, the diodes D_1 and D_2 are turned off, while the diode D_3 is turned on. The flowing current through the output inductors (L_{o1} and L_{o2}) is decreased and increased, respectively. Also, at the time t_6, the demagnetization of the inductor Lx current is finished. For this mode, we have:

$$i_{Lx} = i_{Lx,t5} - \frac{V_{Cx1}}{L_x}(t - t_5). \tag{6}$$

Mode7- (t_6 to t_7) [Figure 2g]: At the start of this mode, the power switch S_2 is turned off at the ZVS condition. After that, the parallel snubber capacitors of the power switches S_1 and S_2 (C_{s1} and C_{s2}) are discharged and charged, respectively. Moreover, the discharge of C_{s2} to the voltage zero provides the condition for switch S_1 to be turned on at ZVS condition at mode 1. Furthermore, during this time, the magnetizing current direction of the coupled inductor changes from positive to negative. Finally, the duration of this period is described as follows:

$$\Delta t_6 = t_7 - t_6 = \frac{V_{in}}{I_1}C_{s1} = \frac{V_{in}}{I_1'}C_{s2}, \tag{7}$$

where I_1 and I_1' are the currents of the inductors L_x and L_{o2} at t_6, respectively. However, this mode finishes when $V_{s2} = V_{in}$ and $V_{s1} = 0$.

Mode8- (t_7 to t_8) [Figure 2h]: Diode D_1 is turned on at this interval, and the current through diode D_3 is linearly decreased. The antiparallel diode of the switch S_1 is turned on and provides the ZCS condition for power switch S_1. Therefore, at the end of this interval and the start of mode 1, the power switch S_1 is turned on at ZVZCS. Consequently, the following equation is deducted for this mode:

$$i_{Lx} = i_{Lx,t7} + \frac{(-V_{Cx1} - V_{Lm})}{L_x}(t - t_7). \tag{8}$$
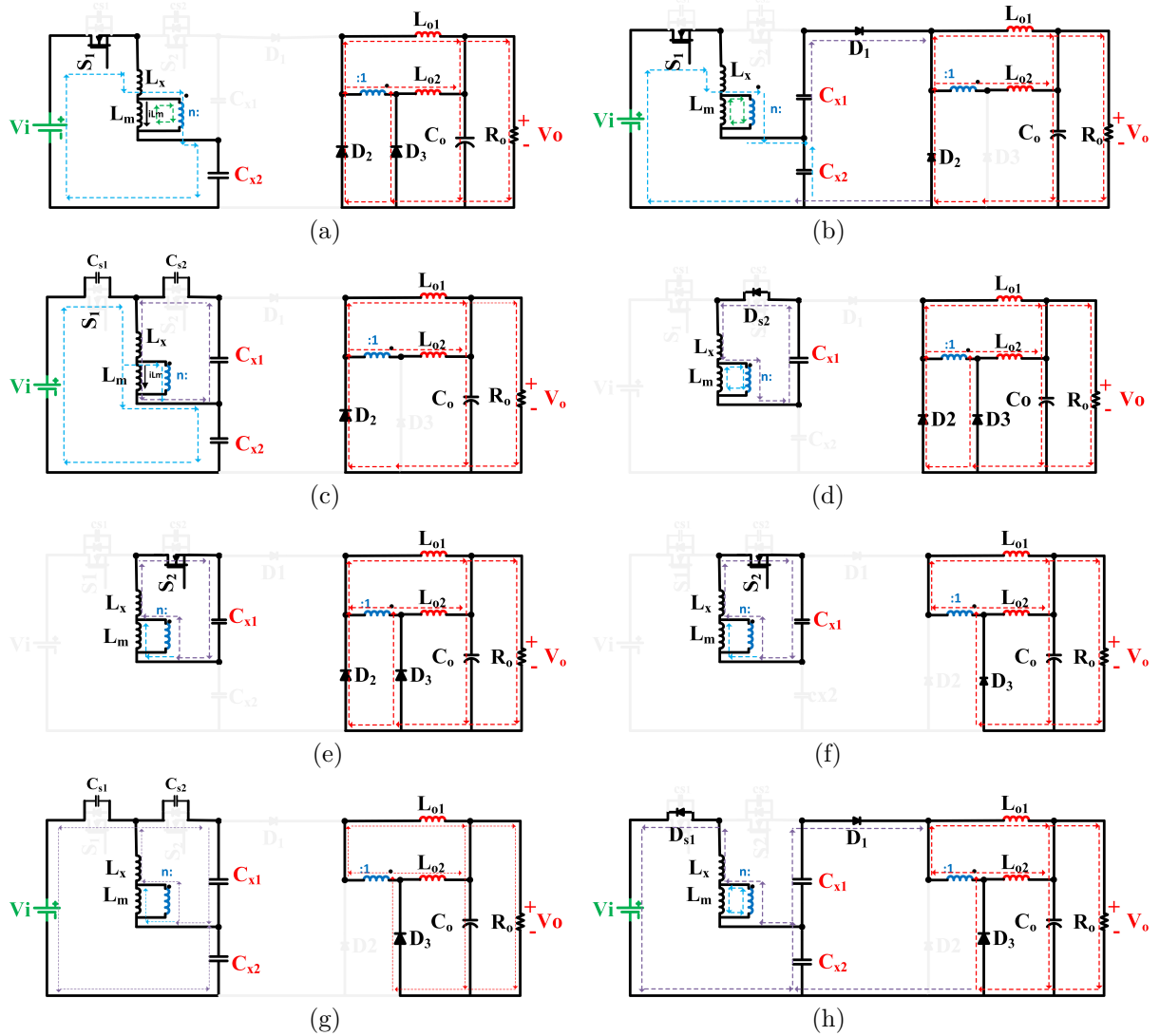
Figure 2. Equivalent circuit of operational modes. (a) mode1, (b) mode2, (c) mode3, (d) mode4, (e) mode5, (f) mode6, (g) mode7, (h) mode8.

## 3. Analysis of the proposed converter in steady-state

The steady-state analysis of the proposed converter is discussed in this section. In addition, it is assumed that the duty cycle is set as 50% with a 2-μs delay duration among pulses. Furthermore, frequency value

variation is utilized for solving the equations. Also, the relationship between voltage gain and duty-cycle change is calculated. To further simplify the description of the converter analysis, the following considerations are supposed: 1) It is considered that the converter is ideal, and losses are neglected; 2) Modes III and VII have short periods and are thus disregarded in the analysis.

3.1. Voltage gain

In this part, the output voltage gain is calculated individually based on switching frequency and duty cycle. The topological voltage conversion ratio is achieved using the principle of conservation of energy. The converter has a maximum voltage gain at a specific duty cycle; hence, to obtain lower voltage gains, the switching frequency variation could be used. According to the inductor L_x current waveform in Figure 3 and by considering the shaded input current lower areas S_1 and S_2, the following equation for input power can be written as:

$$P_{in} = \int_{t_0}^{t_0+T_s} V_{in}.I_{in}dt = (S_1 - S_2)V_{in}. \tag{9}$$
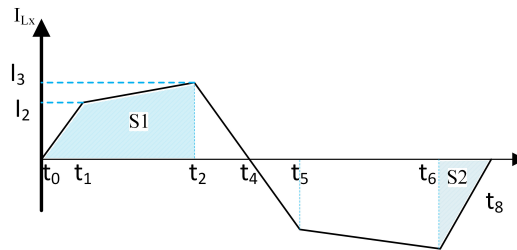
Figure 3. I_{Lx} (black line), Input current (shaded area).

The following equations can be derived using the voltage-second principle applied to auxiliary inductance L_x at modes 2&6.

$$V_{Cx1} = -DV_{in}, (D = 0.5) => V_{Cx1} = -V_{in}/2, \tag{10}$$

$$V_{Cx2} = DV_{in}, (D = 0.5) => V_{Cx2} = V_{in}/2. \tag{11}$$

However, it is necessary to calculate the time intervals for essential working modes to obtain the voltage gain versus switching frequency. The time intervals $\Delta t1 = t0 - t1$ and $\Delta t8 = t6 - t8$ summation are defined as Δt_a where it can be obtained as below:

$$\Delta t_a = \Delta t_1 + \Delta t_8 = {}^{T_s}/_2 - \Delta t_2 \ Where \quad \Delta t_2 = t_2 - t_1, \tag{12}$$

$$\Delta t_a = 2L_x \frac{I_2 + I_3}{V_{in}}. \tag{13}$$

And for the time interval in the mode2, it can be written:

$$\Delta t_2 = t_2 - t_1 = L_x \frac{I_3 - I_2}{V_{in} - V_{Cx} - V_{Lm}} = 2L_x \frac{I_3 - I_2}{V_{in} - 2V_{Lm}}. \tag{14}$$

By using the KCL on the coupled inductor windings at mode 2, it can be deduced that:

$$nI_{Lx} = I_{L2}. \tag{15}$$

By assuming $i_{L2|t_1} = I'_2, i_{L2,|t_2} = I'_3$, $i_{Lx|t_1} = I_2 \& i_{Lx|t_2} = I_3$ and using eq. (15), it can be written:

$$I'_3 - I'_2 = n(I_3 - I_2). \tag{16}$$

Another equation for Δt_2 using the L_{o2} can be found as follows:

$$\Delta t_2 = \frac{L_{o2}(I'_2 - I'_3)}{V_O - V_{Lm}/n} = \frac{nL_{o2}(I_2 - I_3)}{V_O - V_{Lm}/n}. \tag{17}$$

From eqs. (14) and (17) we have:

$$\frac{2L_x(I_2 - I_3)}{2V_{Lm} - V_{in}} = \frac{nL_{o2}(I_2 - I_3)}{V_O - V_{Lm}/n}. \tag{18}$$

So, from eq. (18), the V_{Lm} formula can be calculated as below:

$$V_{Lm} = \frac{L_{o2}nV_{in} + 2V_O L_x}{2n(L_{o2} + L_x)}. \tag{19}$$

By using the voltage balance equation on the inductor L_{o2}, the following can be obtained:

$$V_{Lm} = \frac{nV_O.T_s}{\Delta t_2}. \tag{20}$$

And by using equations (19) and (20), the amount of Δt_2 can be simplified as:

$$\Delta t_2 = \frac{2n^2 V_O T_s (L_{o2} + L_x)}{(L_{o2}nV_{in} + 2V_O L_x)}. \tag{21}$$

The amount of $I_3 - I_2$ can be solved by eqs. (14) and (21) as follows:

$$I_3 - I_2 = \frac{nV_O(V_{in} - 2V_{Lm})}{2L_x f_s V_{Lm}} = \frac{nV_O(nV_{in} - 2V_O)}{f_s(12nV_{in} + 2L_x V_O)}. \tag{22}$$

From eqs. (12) and (13), the sum $I_3 + I_2$ can be obtained as:

$$I_3 + I_2 = \frac{V_{in}(T_s/2 - 2n^2 V_o(L_{o2} + L_x))}{2L_x f_s(2L_x V_o + 12nV_{in})}. \tag{23}$$

So, the amount of I_2 and I_3 can be written as follows:

$$I_3 = \frac{Vin - 4nV_o}{8L_x f_s}. \tag{24}$$

$$I_2 = \frac{V_{in}(T_s/2 - 2n^2 V_o(L_{o2} + L_x))}{2L_x f_s(2V_o L_x + 12nV_{in})} - \frac{V_{in} - 4nV_o}{8L_x f_s}. \tag{25}$$

And the time intervals Δt_1 and Δt_8 are calculated as below:

$$\Delta t_1 = t_1 - t_0 = L_x \frac{I_2}{V_{in} - V_{Cx}} = L_x \frac{2I_2}{V_{in}}, \tag{26}$$

$$\Delta t_8 = t_8 - t_7 = L_x \frac{I_3}{V_{in} - V_{Cx}} = L_x \frac{2I_3}{V_{in}}. \tag{27}$$

The voltage gain calculation for the proposed converter is based on the input and output power equality. So, by considering the input current waveform depicted in Figure 3, the following equation can be regarded:

$$(S1 - S2)V_{in} = V_o I_o T_s. \tag{28}$$

For S1 and S2, we have:

$$S1 = \frac{I_2 \Delta t_1 + (I_2 + I_3)\Delta t_2}{2}, \tag{29}$$

$$S2 = \frac{I_3 \Delta t_6}{2} = \frac{L_x}{V_{in}} I_3^2. \tag{30}$$

It is possible to determine the output voltage gain versus the switching frequency variations by using equation 9, Figure 3, and by solving the equation $(S_1 - S_2)Vin.fs = Vo^2/R$. By assuming the parameter M1 as below:

$$\begin{aligned} M_1 = 4R^2 L_{o2}^2 n^4 + 8R^2 L_{o2} L_x n^4 - 4R^2 L_{o2} L_x n^2 + ... \\ 4R^2 L_x^2 n^4 - 4R^2 L_x^2 n^2 + R^2 L_x^2 + 8R f_s L_{o2}^2 L_x n^2 + ... \\ 8R f_s L_{o2} L_x^2 n^2 + 4R f_s L_{o2} L_x^2 + 4 f_s^2 L_x^2 L_2^2 \end{aligned} \tag{31}$$

Eventually, the relationship between switching frequency changes and output voltage ratio can be expressed as:

$$M = \frac{V_O}{V_{in}} = \frac{n(\sqrt{M_1} - 2f_s L_{o2} L_x + RL_x - 2RL_{o2}n^2 - 2RL_x n^2)}{8 f_s L_x^2}. \tag{32}$$

On the other hand, the maximum voltage ratio of the converter in relation to the duty cycle can be determined as follows:

$$M_{\max} = D/2n. \tag{33}$$

The voltage stress across two power switches can be derived as:

$$V_{S1,\max} = V_{S2,\max} = V_{in} \tag{34}$$

And the voltage stress across Schottky diodes is low and can be found as follows:

$$V_{d1,2,3\,\max} = V_{Lm} = \frac{nV_O.T_s}{\Delta t_2} = \frac{(L_{o2}nV_{in} + 2V_O L_x)}{2n(L_{o2} + L_x)}. \tag{35}$$

3.2. Condition of ZVS for power switches

The converter has two power switches. These power switches are turned on under the zero voltage-zero current switching (ZVZCS) situation and turned off under zero voltage switching (ZVS). To mount ZVS on the switches, the inductance L_x desires sufficient energy to the snubber capacitors C_{s1} and C_{s2} for charging and discharging. In addition, to use ZVS for circuit breakers, the following formula applies:

$$\frac{1}{2}L_x I_3^2 \geq C_s(V_{in})^2, \tag{36}$$

where $C_{s1} = C_{s2} = C_s$. In addition, the snubber capacitor charge time (t_d) should be considerably greater than the switch's current fall time (t_f) to decrease the losses. Consequently, the capacitor's charging time can be determined as follows:

$$t_d \geq 3t_f. \tag{37}$$

3.3. Mode of boundary conduction

The proposed converter will work with CCM and DCM if the following conditions are met:

$$2I_{L_{o1},L_{o2}} \geq \Delta i_{L_{o1},L_{o2}} \quad \rightarrow \quad CCM \quad Operation, \tag{38}$$

$$2I_{L_{o1},L_{o2}} < \Delta i_{L_{o1},L_{o2}} \quad \rightarrow \quad DCM \quad Operation. \tag{39}$$

By using the ampere second law to capacitors C_{x1} and C_{x2}, it can be deduced that the current going through each output choke is 50% of the average output current; hence, in the CCM state $I_o \geq \Delta i_{L_{o1,2}}$. Besides, by supposing $L_{o1} = L_{o2}$, the equation of the output chokes current ripple is as follows:

$$\Delta i_{L1,2} = \frac{(V_{Lm}/n - V_O)\Delta t_2}{L_{o2}}. \tag{40}$$

Substituting (20) into (40) and considering eq. (38), yields:

$$\Delta i_{L_{o1,2}} = \frac{V_o(T_s - \Delta t_2)}{L_{o2}} \rightarrow I_o \geq \frac{V_O(T_s - \Delta t_2)}{L_{o2}}. \tag{41}$$

Thus, the following equation can be used to obtain the voltage gain in DCM mode:

$$(DCM), \frac{V_o}{V_{in}} = \frac{D^2}{2n} \times \frac{1}{D^2 + 0.25 \times (I_o/I_{oB\max})}. \tag{42}$$

The boundary between discontinuous conduction mode (DCM) and continuous conduction mode (CCM) states can also be formulated as follows:

$$V_o/V_{in} = \frac{1 \pm \sqrt{1 - I_o/I_{oB,\max}}}{4n}. \tag{43}$$

However, Figure 4a shows the relationship between the boundary condition characteristics and the duty cycle (D). Also, Using equations (41) through (43), the CCM and DCM regions of operation are illustrated.
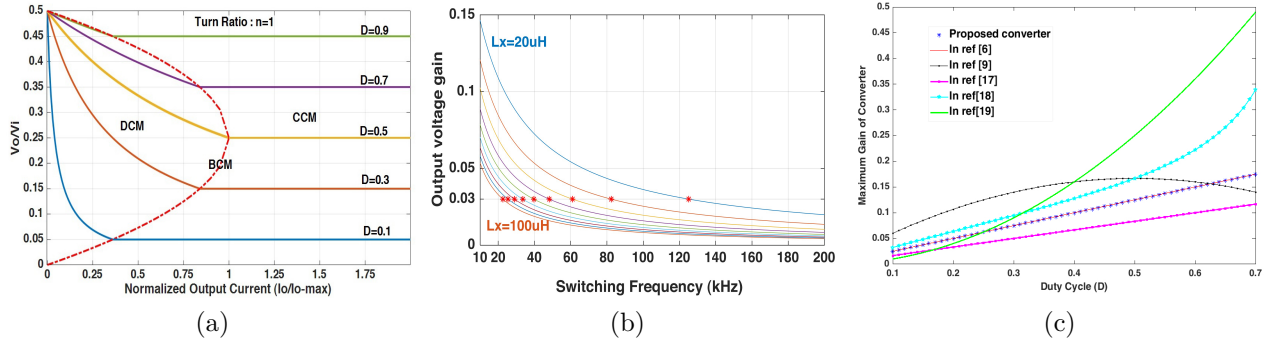
Figure 4. (a) The boundary conduction characteristic curve, (b) the curve representing the output voltage gain of the proposed converter, and (c) comparison of converters' maximum achievable voltage gain curves in references [6,9,17-19] versus the proposed converter.

3.4. Design techniques and analytical comparison

The proposed converter has a wider output voltage range, making it perfect for various low-voltage applications. Figure 4b depicts the output voltage gain curve of the proposed converter, which is obtained by adjusting L_x from 20 μH to 100 μH and switching frequency from 10 kHz to 200 kHz with a constant 50% duty-cycle (D).

Figure 4c depicts the maximum voltage gain vs duty cycle for the proposed converter and the converters in references [6,9,17-19]. Consideration should be given to the fact that the voltage gain of the proposed converter can be adjusted via switching frequency, resulting in an expanded voltage gain range.

For amounts of capacitors C_{x1} and C_{x2}, we have:

$$C_{x1,2} \geq \frac{nI_O D T_s}{2\Delta V_C}. \tag{44}$$

It is possible to calculate the maximum values of the snubber capacitors C_{s1} and C_{s2} to obtain the ZVS operation of power using the following formulas:

$$C_{s1,s2} \geq \frac{I_3 . t_{f,switch}}{V_{in,\min}}, \tag{45}$$

where t_f denotes the current falling time of main switches. Furthermore, the values of the output inductors L_{o1} and L_{o2} can be calculated as follows:

$$L_{o1} = L_{o2} = \frac{V_O(T_S - \Delta t_2)}{\Delta i_{L1,2}}. \tag{46}$$

Finally, the magnetizing inductor (L_m) for the coupled inductor is determined as follows:

$$L_m \geq \frac{\Delta t_2}{0.1 \times I_3} \times \frac{L_2 n V_{in} + 2V_O L_x}{2n(L_2 + L_x)}. \tag{47}$$

The current is less than ten percent of the transformer's maximum in either direction. The proposed converter benefits from the small magnetizing inductor, resulting in a more moderated size and volume.
In Table 1, key parameters and the number of components for the proposed converter, the other nonisolated

high step-down structures, and the isolated DC-DC converter are provided. According to Table 1, the proposed converter and the converters described in references [18] and [19] benefit from common ground. The common-ground characteristic allows the converter to have less electromagnetic interference (EMI) and to sense output voltage directly, resulting in rapid and precise adjustment of output voltage. However, the converter in ref [19] suffers from hard-switching, whereas the converter in ref [18] should operate with a duty-cycle of D = 5% to get a gain of 10V/300V = 0.033. As is well known, when the duty cycle is extremely low, such as D = 5%, the efficiency of the step-down converter decreases to extremely low levels. Additionally, the soft switching working region may be lost.

The suggested converter, on the other hand, works with D = 50% at every output voltage gain, and the output voltage gain will be changed by switching frequency or auxiliary inductance value, as shown in Figure 4b. In addition, the other converters are simulated by MATLAB simulink software with similar condition to the proposed converter and the efficiencies have been obtained and added to Table 1 to show the advantage of the proposed converter.

Table 1. Examination of the proposed converter in contrast with different designs.

Case	Proposed	Ref [6]	Ref [9]	Ref [17]	Ref [18]	Ref [19]	Ref [20]
Switches count	2	4	4	6	2	2	2
Diodes count	3	2	0	2	1	2	2
Capacitors count	3	5	1	5	1	2	2
No. of the mag. cores /coupled inductors	4/1	2/0	0/2	2/0	0/1	2/0	4/1
Winding of coupled inductors	2	0	2	-	2	-	1:1 Transformer
Total device count	12	13	7	15	5	8	10
Maximum voltage gain	$D/2n$	$D/4$	$\frac{nD(1-D)}{n+1}$	$D/6$	$\frac{D-D^2}{1+n-nD-nD^2}$	D^2	$D/2n$
Output voltage range, Extended(E), Not extended (NE)	E	NE	NE	NE	NE	NE	E
Switch voltage stress	Vi	Vi	Vi	Vi/3	Vi	$V_i, \sqrt{D}V_i$	Vi
Voltage stress on diodes	Vi/3	-	-	Vi/6	Vi	$V_i, \sqrt{D}V_i$	Vi/3
Total standing voltage on switches	2Vi	4Vi	4Vi	2Vi	2Vi	$(1+\sqrt{D})V_i$	2Vi
Total standing voltage on diodes	Vi	-	-	Vi/3	Vi	$(1+\sqrt{D})V_i$	2/3Vi
Output current ripple	Very-low	Low	Low	Very-low	Low	High	Very-low
Common ground	Yes	No	No	No	Yes	Yes	No
Implementation cost	Medium-low	Low	Low	Medium-high	Low	Low	Medium-low
Isolation type N-I (Nonisolated) I (Isolated)	N-I	N-I	N-I	N-I	N-I	N-I	I
Efficiency at 200 W (300 V input, 10 V output at duty cycle (D), turn ratio n = 0.5	91.5% D: 50%	81.6% D: 13%	87% D: 12%	81.8% D: 19	45% D: 5%	66.2% D: 5%	89% D: 50%
Switching condition	ZVS - ZVZCS	Hard - switching	ZVS	Hard - switching	ZVS - ZVZCS	Hard - switching	ZVS - ZVZCS

4. Experimental results

The proposed 200-W output converter case study is implemented herein. Table 2 lists parameter and element quantities. Table 2 compares component counts, semiconductor voltage stress, and other critical factors. Table 2 shows the converter's benefits. Common ground reduces EMI across the circuit. The converter's nonisolated structure also complements extended low-voltage applications. Comprehensive output voltage gain allows a wide output voltage range. The converter's direct output voltage allows precise control. Three diodes share output current, reducing semiconductor current stress.

For implemented circuit, the amount of duty cycle is fixed at D = 50%. Therefore, the pulse widths of the main switches are equal, and the operational switching frequency is 40 kHz.

Table 2. Proposed specifications for converter elements and input voltage under test conditions.

Input voltage	300 V	Inductors (L_{o1},L_{o2})	100 μH (3*0.8 mm litz-wire, EE42-21,N = 23)
output voltage	10 V	Inductor (L_x)	60 μH
Load	0.5 Ω	Magnetizing inductor (L_m)	250 μH
Switches S_1 and S_2	20n50	Turn ratio	(15/30 turns)
Snubber capacitors ($C_{s1,2}$)	10nF	Switching frequency	40 kHz
Schottky diodes ($D_{1,2,3}$)	TSF30H200C, Vf = 0.8v	Capacitors (C_{x1},C_{x2})	22μf -200 V
Capacitors(C_o)	470μf -50 V	PID controller coefficients	$K_p = 21.2, K_i = 7.6e4, K_d = 6.1e-5$

An ATMEGA-AVR-based PI controller feeds an SG3525-based frequency-oscillated MOSFET driver for pulse generating. Complementary pulses are applied to the power switches. Figure 5a shows the converter's control system. Figure 5b illustrates the implemented converter. Some of the main waveforms obtained from the converter are collected and are shown in Figure 6. It is shown that the converter switches are working in soft-switching conditions, and also the output voltage is fixed at 10 V. Figure 6 shows the voltage and current waveforms for the switches S_1 and S_2. Figures 6a, 7a, 6b, and 7b demonstrate the zero voltage and zero current at the turning-on transition. Also, the ZVS is performed when the switches are turned off. However, a small overlap exists for the ZVS-OFF condition. Because of the small overlap time interval and lower voltage and current values at that condition, the resulting losses are not of a significant magnitude. The switches are subjected to a voltage stress of 300 V, which is the same as the input voltage and agrees with eq. (34). Figures 6c and 7c illustrate the gate pulses corresponding to the switches S_1 and S_2 at 10 V and 8 V of output voltage, respectively. The pulses are complementary and are generated with SG3525 with two microseconds of dead time, and also the negative voltage for the switches at the turn-off process is provided. Figures 6d, 7d, 6e, and 7e show the voltage waveforms of the diodes D_1, D_2 and D_3, respectively. Here, there is a 100-V stress on the power diodes, which can be theoretically resolved using equation (35) below:

$$V_{D1,2,3,\max} = \frac{nV_O.T_s}{\Delta t_2} = \frac{0.5 \times 10 \times 1/40000}{1.23 \times 10^{-6}} = 100V. \tag{48}$$

Moreover, according to equation (34), the theoretical voltage stress across the power switches is equal to the input voltage, and it is 300 volts. Furthermore, the amount of current stress (peak current) across the power

switches S_1, S_2 (equal to I_3 in figure 3) and the diodes $D_{1,2,3}$ can be calculated as:

$$I_{S1,S2\,max} = I_3 = \frac{V_{in} - 4nV_o}{8L_x f_s} = \frac{300 - 4 \times 0.5 \times 10}{8 \times 60\mu H \times 40kHz} \simeq 14.5A \tag{49}$$

Besides, the peak current across the body diode D_1 is equal to half of the output current ($I_{D1,max} = DI_o$), and the maximum current stress of two other diodes (D_2 and D_3) is limited to the output current average. So, the maximum current that can flow through D_1 is 10 A, and it is 20 A for D_2 and D_3. Furthermore, the amount of Δt_2 by using eq. (21) can be calculated as:

$$\Delta t_2 = \frac{2n^2 V_O T_s (L_{o2} + L_x)}{(L_{o2} n V_{in} + 2V_O L_x)} = \frac{2 \times 0.5^2 \times 10 \times (1/40000) \times (100 + 60)}{(100 \times 0.5 \times 300 + 2 \times 10 \times 60)} = 1.23\mu s. \tag{50}$$

The voltages through the capacitors C_{x1} and C_{x2} are about –150 V and 150 V in Figure 7a, which agree with eqs. (10) and (11). Finally, Figures 6g and 7g show the output current through the inductors L_{o1} and L_{o1} for 10 V and 8 V of output voltages, in which 10 A and 8 A are carried through each output inductor, respectively. In addition, according to equation (41), calculating the current ripple of each output inductor is as follows:

$$\Delta I_{L_{o1,2}} = \frac{V_O(T_s - \Delta t_2)}{L_{o2}} \simeq 2.3A. \tag{51}$$

Additionally, switching frequency variation controlled the proposed converter. Figure 6a shows the converter step response after an 8 V to 10 V output voltage step adjustment. The output voltage step change takes 500 microseconds. At 200 W output power, the proposed converter has 91.5% efficiency. Higher output power increases efficiency, but the slope has decreased. Figure 8 shows the proposed converter efficiency diagram. Figure 8 includes the efficiency curve with switching losses to demonstrate soft switching's benefits. Without soft switching, efficiency drops to 85.6% at 200 W output power, according to theoretical estimates. The converter's 5.9% efficiency loss increases power switch and converter losses.
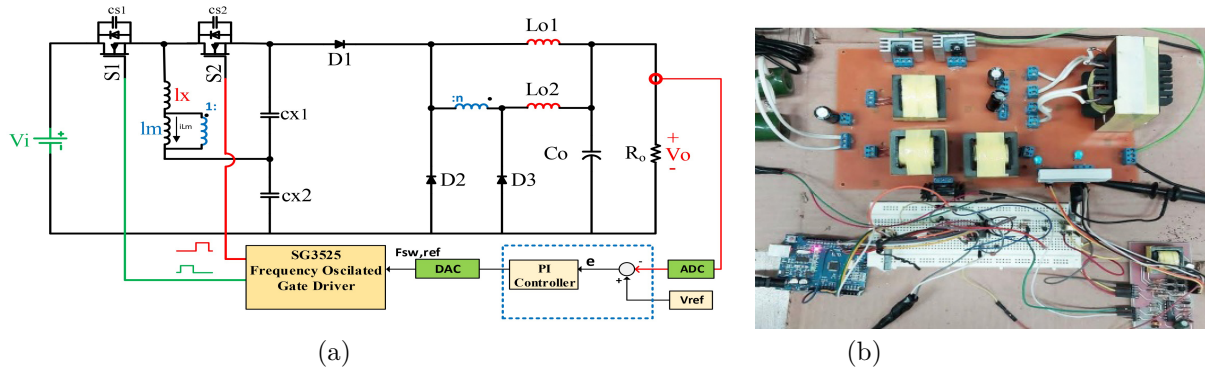

(a)   (b)

Figure 5. (a) Proposed converter control method, (b) proposed converter graphic representation.

5. Conclusion

In the current work, a new topology for a DC-DC converter with high step-down capability, high efficiency, and a low number of elements has been proposed. A coupled inductor has also been used to have a lower output gain. Also, soft switching for power switches has been achieved using an auxiliary inductor (L_x) in
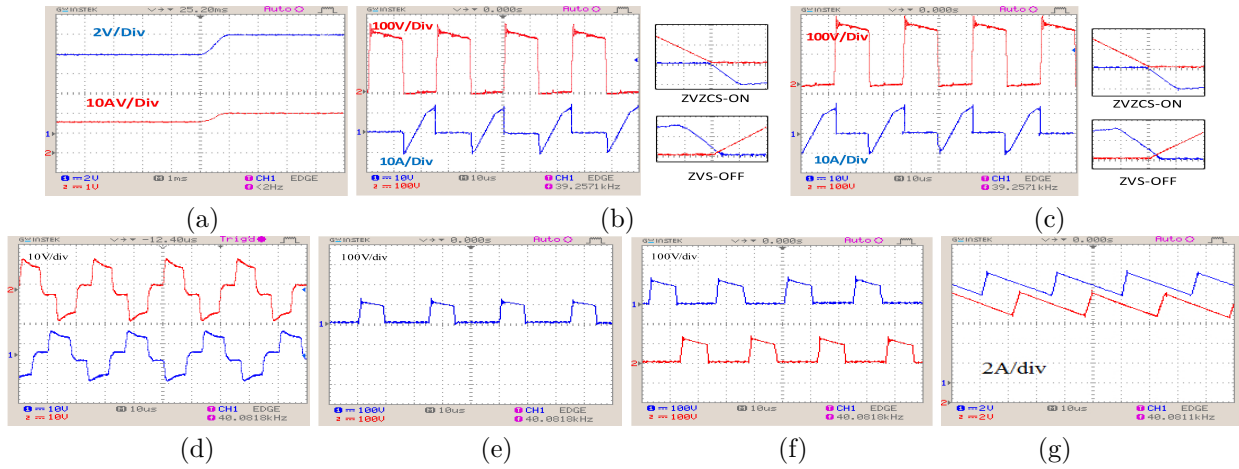
Figure 6. The proposed converter's main experimental waveforms, (a) The step change of the output voltage-current by variyng from 8 V to 10 V, and for 10 V output voltage: (b) power switch S_1 $V_{ds} - I_C$, (c) power switch S_2 $V_{ds} - I_C$, (d) gate pulses of S_1 and S_2, (e) V_{D1},(f) $V_{D2,3}$, (g) output inductor currents.
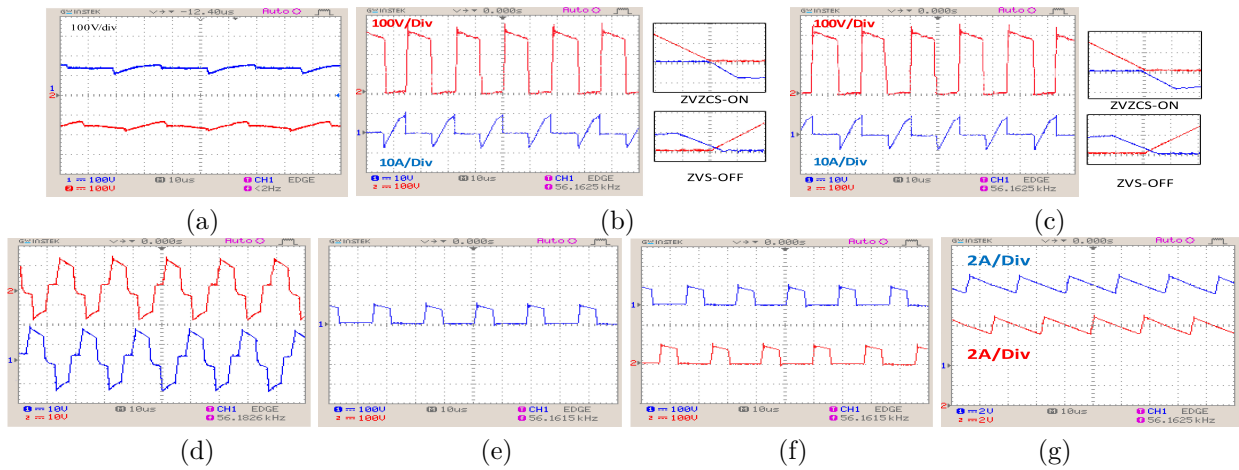
Figure 7. The proposed converter's main experimental waveforms at 8 V output voltage, (a) converter capacitors voltages V_{Cx1}-V_{Cx2}, (b) power switch S_1 $V_{ds} - I_C$, (c) power switch S_2 $V_{ds} - I_C$, (d) gate pulses of S_1 and S_2, (e) V_{D1},(f) $V_{D2,3}$, and (g) output inductor currents.
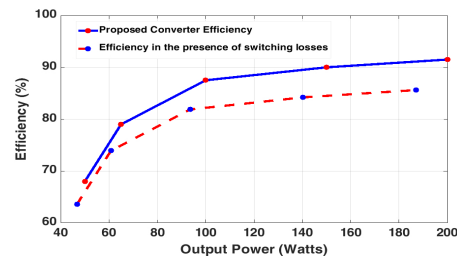
Figure 8. A comparison of the proposed converter's efficiency with and without switching losses.

series. In order to obtain a higher output current, an interleaved combination has been used for inductors at the output, which results in a current division between output Schottky diodes to handle more current at

the output. Moreover, the proposed converter has been designed to have an extensive range of output voltage ratios, which can be achieved by changing the converter switching frequency. In addition, the converter's working principles and mathematical analysis have been discussed. Finally, a 200-W prototype has been built. Experimental results have been presented, compared, and agreed with theoretical calculations. The proposed converter output efficiency is about 91.5% at the duty-cycle D = 50%, fsw = 40 kHz, and 10 V output voltage with the output load $R_L = 0.5\Omega$.

References

[1] Taghizadegan Kalantari N, Ghabeli Sani S, Sarsabahi Y. Implementation and design of an interleaved Cuk converter with selective input current ripple elimination capability. International Journal of Circuit Theory and Applications. 2021;49 (6):1743-56.

[2] Köse H, Aydemir MT. A step-down isolated three-phase IGBT boost PFC rectifier using a novel controlalgorithm with a novel start-up method. Turkish Journal of Electrical Engineering and Computer Sciences. 2021;29 (2):978-93.

[3] Ghabeli Sani S, Mohammadi F, Banaei MR, Farhadi-Kangarlu M. Design and implementation of a new high step-up DC-DC converter for renewable applications. International Journal of Circuit Theory and Applications. 2019 ;47 (3):464-82.

[4] Yao K, Qiu Y, Xu M, Lee FC. A novel winding-coupled buck converter for high-frequency, high-step-down DC-DC conversion. IEEE transactions on power electronics. 2005;20 (5):1017-24.

[5] Modeer T, Norrga S, Nee HP. High-voltage tapped-inductor buck converter utilizing an autonomous high-side switch. IEEE Transactions on Industrial Electronics. 2014;62 (5):2868-78.

[6] Pan CT, Chuang CF, Chu CC. A novel transformerless interleaved high step-down conversion ratio DC–DC converter with low switch voltage stress. IEEE transactions on industrial electronics. 2014 Jan 21;61 (10):5290-9.

[7] Hwu KI, Jiang WZ, Yau YT. Nonisolated coupled-inductor-based high step-down converter with zero DC magnetizing inductance current and nonpulsating output current. IEEE Transactions on Power Electronics. 2015;31 (6):4362-77.

[8] Kirshenboim O, Peretz MM. High-efficiency nonisolated converter with very high step-down conversion ratio. IEEE Transactions on Power Electronics. 2016;32 (5):3683-90.

[9] Marvi F, Adib E, Farzanehfard H. Efficient ZVS synchronous buck converter with extended duty cycle and low-current ripple. IEEE Transactions on Industrial Electronics. 2016 27;63 (9):5403-9.

[10] Kumar MA, Bhakthavatchalu R. FPGA based delay PUF implementation for security applications. In2017 International Conference on Technological Advancements in Power and Energy (TAP Energy) 2017(pp. 1-6). IEEE.

[11] Mostaan A, Gorji SA, Soltani MN, Ektesabi M. A novel single switch transformerless quadratic DC/DC buck-boost converter. In2017 19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe) 2017 (pp. P-1). IEEE.

[12] Uno M, Kukita A. PWM switched capacitor converter with switched-capacitor-inductor cell for adjustable high step-down voltage conversion. IEEE Transactions on Power Electronics. 2018;34 (1):425-37.

[13] Ganjavi A, Ghoreishy H, Ahmad AA. A novel single-input dual-output three-level DC–DC converter. IEEE Transactions on Industrial Electronics. 2018 ;65 (10):8101-11.

[14] Köse H, Aydemir MT. A step-down isolated three-phase IGBT boost PFC rectifier using a novel controlalgorithm with a novel start-up method. Turkish Journal of Electrical Engineering and Computer Sciences. 2021;29 (2):978-93.

[15] Tu C, Chen R, Ngo KD. Series-Resonator Buck Converter—Viability Demonstration. IEEE Transactions on Power Electronics. 2021;36 (9):9693-7.

[16] Khalili S, Molavi N, Farzanehfard H. Soft-switched asymmetric interleaved WCCI high step-down converter with low-voltage stress. IEEE Journal of Emerging and Selected Topics in Power Electronics. 2021;9 (6):6692-9.

[17] Syrigos SP, Christidis GC, Mouselinos TP, Tatakis EC. A non-isolated DC-DC converter with low voltage stress and high step-down voltage conversion ratio. IET Power Electronics. 2021;14 (6):1219-35.

[18] Vesali M, Ranjbar H, Ghafoorian F. A new soft-switching high step-down DC-DC converter for voltage regular module application. IET Circuits, Devices and Systems. 2022;16 (2):136-46.

[19] Nejad ML, Esteki M, Heidari R, Adib E. An Improved Cascade Buck Converter for High Step-Down DC-DC Applications. IEEE Journal of Emerging and Selected Topics in Industrial Electronics. 2022;3 (3):626-34.

[20] Sani SG, Banaei MR, Hosseini SH. Analysis and implementation of an isolated high step-down converter with interleaved output for low voltage applications. International Journal of Circuit Theory and Applications. 2022.