Turk J Phys
35 (2011) , 1 – 12.

doi:10.3906/fiz-1012-71

Effects of SILAR cycle on the electrical characteristics of Cd/CdSe/n-Si/Au-Sb structure

Betül GÜZELDİR, Mustafa SAĞLAM and Aytunç ATEŞ
Department of Physics, Faculty of Sciences, Atatürk University, 25240, Erzurum-TURKEY
e-mail: bguzeldir84@gmail.com

Received: 23.12.2010

Abstract

Cd/CdSe/n-Si/Au-Sb structures have been fabricated by Successive Ionic Layer Adsorption and Reaction (SILAR) method under various SILAR cycles. The characteristics parameters of these structures such as barrier height, ideality factor, series resistance are calculated from the current-voltage (I-V) measurements and the barrier height, carrier concentration are calculated from reverse bias capacitance-voltage (C-V) measurements at 300 kHz frequency and room temperature. Furthermore, the density distribution and rectifying ratio of these structure have been calculated from the I-V measurements as a function of SILAR cycle. It has been seen that the changes of characteristic parameters such as barrier height, ideality factor and series resistance of the Cd/CdSe/n-Si/Au-Sb structures have lightly changed with increasing SILAR cycle.

Key Words: CdSe, SILAR method, sandwich structure

1. Introduction

Metal-Semiconductor (MS) contacts have been the focus of extensive theoretical and experimental studies for several decades [1–4]. Due to the technological importance of MS contact devices, a full understanding of the nature of their electrical characteristics is of greater interest [5–10]. Control of the barrier height is critical to the successful operation of devices based on MS contacts. Unstable contacts result in barrier height changes, increased leakage current, and other undesirable effects that degrade the electrical performance of the device. Therefore, research on mechanisms which influence barrier heights at metal-semiconductor contacts is of high interest from a basic and a practical point of view [11].

The SILAR method involves an alternative immersion of the substrate in a solution containing a soluble salt of the cation and anion of the compounds to be grown. The substrate supporting the growing film is rinsed in high purity deionized water after each immersion in order to avoid homogeneous precipitation. The immersion and rinsing time periods can be experimentally determined. In principle, SILAR is a deposition method in

which thickness of the layer has determined by the number of deposition cycles. The SILAR method has been employed for the deposition of CdS, ZnS, CdZnS, PbS, CuS, CdSe, etc. thin films on different substrates [12–16].

Chemically deposited CdSe thin films have received increasing interest due to it is use in semiconductor devices. The effects of bath parameters and nature of substrate on the rate of deposition of CdSe thin film by CBD method have been reported by Kainthala et al. [17]. Baudreau and Rauh [18] have modified Kainthala's method to deposit CdSe and concluded that the ammonia was critical in getting good quality reproducible CdSe thin films. Mondal et al. [19] have deposited CdSe thin films at room temperature using triethanolamine (TEA) as a complexing agent. Dhumure and Lokhande [20] have chemically deposited CdSe films and reported the effect of some of the preparative parameters on the deposition process. Jodgudri and Lokhande [21] have reported photoelectrochemical cell based on CdSe and SnS electrodes. Garacia et al. [22] have prepared highly photosensitive CdSe thin films by CBD method.

II-VI binary semiconducting compounds belonging to the cadmium chalcogenide family (CdS, CdSe, CdTe) are considered very important materials for photovoltaic applications. CdSe is a promising photovoltaic material because of its high absorption coefficient and nearly optimum band gap energy for the efficient absorption of light and conversion into electrical power. CdSe is an important material for the development of various modern technologies of solid state devices such as high efficiency thin film transistors and light emitting diodes. Other areas of successful applications include photo-detectors, light amplifiers, lasers, gas sensors, large-screen liquid crystal display and photoluminescence response. Several physical and chemical techniques are available for the growth of CdSe thin films. CdSe thin films have been deposited using different techniques such as electrodeposition, molecular beam epitaxy, spray pyrolysis, SILAR method, vacuum deposition and chemical bath deposition. Among these methods SILAR has several overriding advantages over other techniques such as uniform film deposition, control of thickness, precise maintenance of deposition temperature and low cost. In SILAR method, thin films are obtained by immersing a substrate into separately placed cationic and anionic precursors and thus, precipitate in-solution formation, whereby wastage of material is avoided. SILAR is an attractive and less expensive method for film preparation. Preparative parameters such as concentration, pH, nature of the complexion agent, temperature, etc., are easily controllable. In the present work, studies were carried out on properties of Cd/CdSe/n-Si/Au-Sb structure with aim for their possible use in optoelectronic devices [23].

Electronic energy levels in the semiconductor bandgap play a key role in the determination of solid state device characteristics. When these levels, or states, are localized in the semiconductor bulk, they can be easily characterized and somewhat controlled to alter device behavior. However, such states at the semiconductor-metal interface can neither be routinely determined nor controlled. In particular, the measurement of interface charge in these levels at the metal-semiconductor junction has eluded researchers due to problems in handling the currents flowing in the contacts. It is well-known that interface properties have a dominant influence on the device performance, reliability and stability. Barrier height is one of the most important characteristic parameters in metal-semiconductor contacts. Barrier height generally forms different from expected due to undesired effects between the metal-semiconductor interface. Barrier height stability can be enhanced via methods such as formation of a thin layer in the metal-semiconductor interface and by annealing the metal-semiconductor contact. In this study, we use CdSe thin film for just such an aim to enhance the Cd/n-Si structure.

In this study, Cd/CdSe/n-Si/Au-Sb structures have been fabricated directly on n-Si semiconductors by the SILAR method. The purpose of this paper is to characterize how the I-V and C-V characteristics parameters,

such as barrier height, ideality factor, series resistance, density distribution, and so, in the Cd/CdSe/n-Si/Au-Sb structure change with increasing SILAR cycle. The I-V and C-V measurements of the structure have been carried out under laboratory conditions in dark at room temperature.

2. Experimental

The cleanness and hydrophilicity of substrates play an important role in the deposition of films. Contaminated substrates result in nonuniform film formation [24]. The deposition of thin films or multilayer systems is always accompanied by stress generation both in substrate and growing film. Stress and adhesion determine the stability of a thin film substrate composite and thus the lifetime of a component, since the composite may fail by cracking, delamination or buckling. Stresses exist even though films are not externally loaded. Film stresses that tend to increase with thickness of the growing film are a prime limitation to the growth of very thick films, because they promote film peeling. In addition, film stresses affect band gap shifts in semiconductors, transition temperatures in superconductors and magnetic anisotropy. Substrate deformations and distortion may also arise from stresses in overlying films [25, 26]. So we can say that, substrate is very important parameter. The adoption of suitable substrates might play key roles in constructing semiconductor nano-heterostructures for achieving enhanced physical properties.

Samples were prepared using mirror cleaned and polished n-type Si wafers with (100) orientation and 1 – 10 Ω – cm resistivity. The wafer was chemically cleaned using the RCA cleaning prodecure (i.e., 10 min boil in NH_3+H_2O_2+6 H_2O followed by $HCl + H_2O_2$+6H_2O at 60 °C). The native oxide on the front surface of the n-Si substrate was removed in $HF + 10H_2O$ solution and finally the wafer rinsed in de-iosined water for 30 s. Ohmic contacts of low resistance on the backside of the samples were formed by evaporating of Au-Sb alloy followed by a temperature treatment at 420 °C for 3 min in nitrogen atmosphere. After ohmic contact was made, the ohmic contacat side and the edges of the n-Si semiconductor substrate were covered by wax so that the polished and cleaned front side of the semiconductor sample was exposed to the cationic precursor solution employed for SILAR method. Cadmium selenide thin films were deposited by using $CdCl_2$ and freshly prepared sodium selenosulphate (Na_2SeSO_3) solitions. The Na_2SeSO_3 solution was prepared by mixing 10 g selenium powder (99% purity) with 100 gr anhydrous sodium sulfite in 500 ml of distilled water with constant stirring for 8–10 h at 80 °C. It was sealed and kept overnight, since on cooling, a little selenium separated out from the solution. It was then filtered to obtain a clear solution.

$CdCl_2$ solution was used for cationic precursor. Sodium selenosulphite was used as a source of selenium ions. The adsorption time, reaction time and rinsing time to control the growth of CdSe thin film were selected as 20 s, 30 s and 50 s, respectively. A single SILAR deposition cycle consisted of 20 s adsorption of Cd^{+2} ions, 50 s rinse with double distilled water, 30 s adsorption and reaction of Se^{2-} ions with preadsorbed Cd^{2+} ions on the substrate, followed by 50 s rinse with double distilled water. By repeating such deposition cycles 20, 25 and 30 times, we obtained CdSe thin films on Si substrates, respectively.

In order to carry out electrical measurement, the cadmium contacts were formed by evaporation of Cd dots with diameter corresponding to a diode area of 7.85×10^{-3} cm^2 onto the CdSe thin films, in a vacuum-coating unit at 10^{-7} mbar. The processing stage was outlined in Figure 1 and a schematic cross-section of the sample is shown in Figure 2.

The I-V and C-V characteristics of these structures were measured using a HP 4140B picoampermeter and a HP model 4192A LF impedance analyser, respectively, at room temperature in the dark.

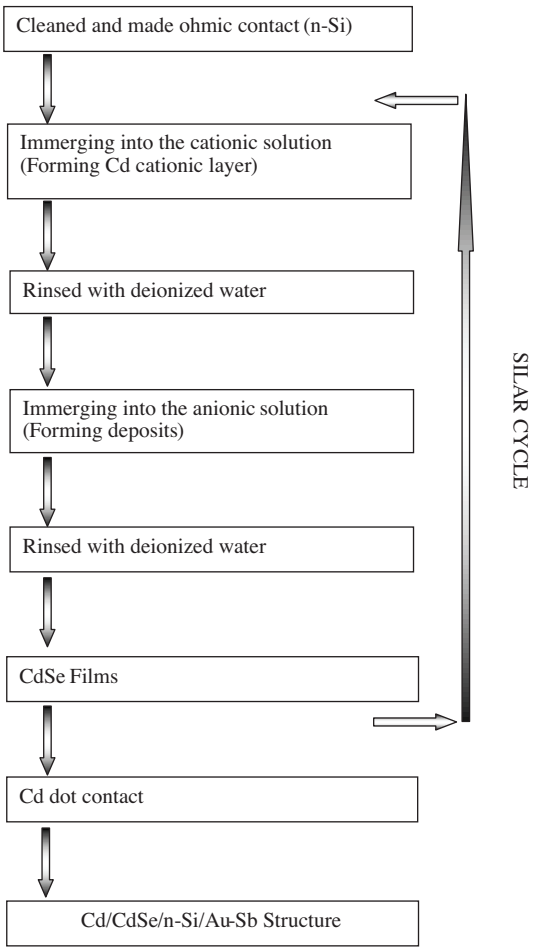

Figure 1. The processing stage of Cd/CdSe/n-Si/Au-Sb structure.

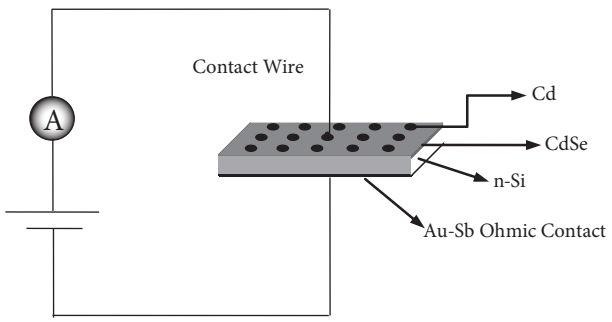

Figure 2. The structure diagram of the fabricated device.

3. Results and discussion

3.1. Surface properties

Surface morphology of deposited CdSe thin films were studied using SEM. SEM is a convenient and versatile method to study the microstructure of thin film. The surface morphology of CdSe thin film prepared

at room temperature is shown in Figure 3. From the micrograph it was speculated that the agglomeration of spherical grains led to the formation of relatively big islands of spherical shape but of different size. There are no macroscopic defects like void, pinhole, peeling or cracks. From the featureless surface morphology of the deposited CdSe thin films, we can anticipate that these films will exhibit very low optical scattering losses and should therefore be suitable for optoelectronic applications.

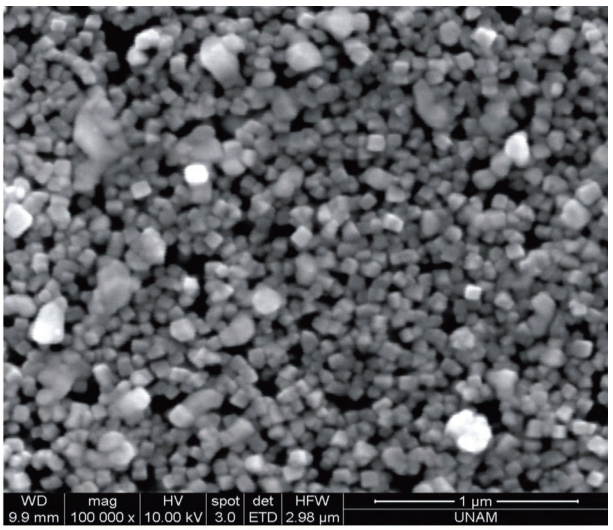

Figure 3. SEM image of the CdSe thin film grown on n-Si substrate.

3.2. Current-voltage characteristics

When a MS structure with the R_s is considered, the I-V equation in respect to the thermoionic emission (TE) theory is given by [1]

$$I = I_0 \exp\left(\frac{eV}{nk_BT}\right)\left[1 - \exp\left(-\frac{e(V - IR_s)}{kT}\right)\right], \tag{1}$$

where n is the ideality factor, k_B is the Boltzmann constant, e is the electron charge, V is the forward bias voltage, T is the temperature, R_s the series resistance and I_0 is the saturation current and is given by

$$I_0 = AA^*\ T^2 \exp\left(-\frac{e\Phi_b}{k_BT}\right) \tag{2}$$

$A*, A, \Phi_b$ are the effective Richardson constant of 112 A/cm^2K^2 for n-type Si, the area of the rectifier contact, and the experimental zero bias barrier height, respectively. The value of ideality factor n is can be obtained from equation (1) as

$$n = \frac{e}{k_BT}\frac{dV}{d\left(\ln I\right)}. \tag{3}$$

Figure 4 shows the forward and reverse bias I-V curves of the Cd/CdSe/n-Si/Au-Sb structures as a function of SILAR cycle. The values of the parameters obtained from these characteristics are given in Table 1. The barrier height value of Cd/CdSe/n-Si/Au-Sb structure was calculated with the help of equation (2) from the y-axis intercepts of the semilog-forward bias I-V plots, and the value of the ideality factor n was obtained using

equation (3) from the linear region of these plots. The ideality factor n is introduced to take into account the deviation of the experimental I-V data from the ideal TE model. This can be attributed to the interfacial layer of CdSe layer on the n-Si surface. If the Si surface is prepared by the usual polishing and chemical etching technique, and the evaporation of metal is carried out in a conventional vacuum system having a pressure of around 10^{-7} Torr, the Si surface is inevitably covered with a thin insulating film. This interfacial oxide layer can be formed by water or vapour adsorbed onto the surface of the n-type Si before adding the $CdCl_2$ and Na_2SeSO_3 solutions on the front surface of the n-Si substrate. It may form either during surface preparation and metal evaporation or post-deposition thermal annealing. For a sufficiently thick interface layer, the interface states are in equilibrium with the inorganic semiconductor and they cannot interact with the metal. For MS contacts it is known that the contact characteristics are controlled by Fermi level pinning due to the interface states. That is, it can be concluded that the barrier height determined from the I-V characteristic is controlled by the interface states in equilibrium with the semiconductor [4, 27].

Table 1. The experimental values of parameters obtained from I–V of Cd/CdSe/n-Si/Au-Sb structures with increasing SILAR cycle.

Cd/CdSe/	I-V			F(V)-V		dV/d(ln I)–I		H(I)-I	
n-Si/Au-Sb	n	Θ_b (eV)	I_0 (A)	Θ_b (eV)	R_s (kΩ)	n	R_s (kΩ)	Θ_b (eV)	R_s (kΩ)
20 Cycle	2.122	0.732	6.474E-009	0.783	36.310	2.994	45.890	0.756	42.772
25 Cycle	2.110	0.733	6.281E-009	0.786	38.021	2.881	43.766	0.761	40.884
30 Cycle	2.021	0.718	6.075E-009	0.779	39.223	2.574	47.330	0.759	49.359

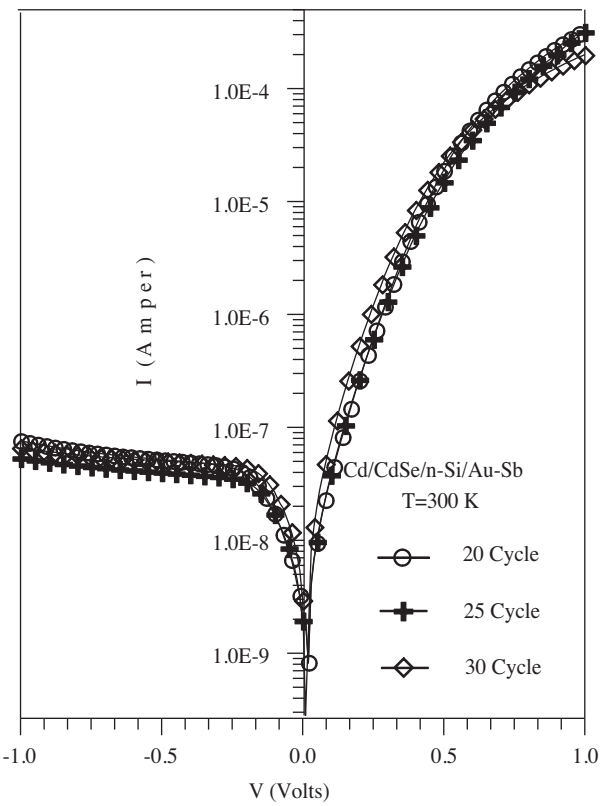

Figure 4. The forward and reverse bias current-voltage characteristics of Cd/CdSe/n-Si/Au-Sb structure as a function of SILAR cycle.

On a semi-log scale and at low forward bias voltage, the I-V characteristics of the metal-semiconductor contacts are linear but deviate considerably from linearity due to the some factors at large voltages. One of the factors is series resistance (R_s). The barrier height, as well as the other diode parameters as the ideality factor n and the series resistance R_s can be calculated by means of a method developed by Cheung in the high current range where the I-V characteristics is not linear [28, 29]. Cheung's functions can be written as [29]

$$\frac{dV_a}{d\left(\ln I\right)} = \frac{nk_BT}{e} + IR_s \tag{4}$$

$$H(I) = V - \left(\frac{nk_BT}{e}\right)\ln\left(\frac{I}{AA^*T^2}\right) \tag{5}$$

$$H(I) = n\Phi_{bn} + IR_s, \tag{6}$$

where Φ_{bn} is the barrier height obtained from data of downward curvature region in the forward bias I-V characteristics. equation (4) should give a straight line for the data of downward curvature region in the forward bias I-V characteristics. The slope of the linear part of the $\mathrm{d}V/\mathrm{d}(\ln I)$ versus I will give R_s and its y-axis intercept will give nq/k_BT. Using the n value determined from equation (4) and the data of downward curvature region in the forward bias I-V characteristics in equation (5), a plot of) $H(I)$ versus I according to equation (5) will also give a straight line with y-axis intercept equal to $n\Phi_b$. The slope of this plot also provides a second determination of R_s that can be used to check the consistency of Cheung's approach. These plots are shown in Figure 5 and Figure 6.

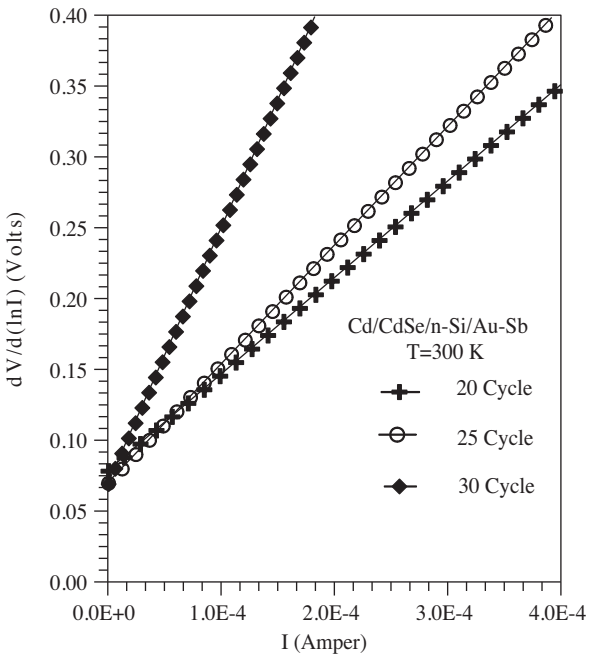

Figure 5. Experimental dV/d(ln I)-I curves of Cd/CdSe/n-Si/Au–Sb sandwich structure as a function of SILAR cycle.

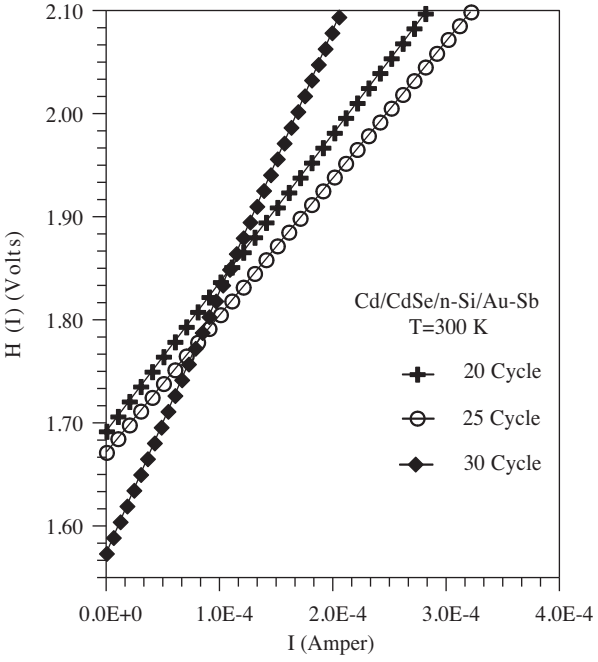

Figure 6. Experimental H(I)-I curves of Cd/CdSe/n-Si/Au–Sb sandwich structure as a function of SILAR cycle.

We can say that the series resistance values calculated from Cheung's functions are in good agreement with each other according to Table 1. However, it can be clearly seen that there is relatively a high difference

between the values of the ideality factor obtained from the downward curvature regions of forward bias I-V plots and from the linear regions of the same characteristics. The reason of this difference can be attributed to the existence of effects such as the series resistance and the bias dependence of the barrier height according to the voltage drop across the interfacial layer and change of the interface states with bias in this concave region of the I-V plot [1].

Norde proposed a method to determine value of the series resistance. The following function has been defined in the modified Norde's method [30, 31]:

$$F(V) = \frac{V}{\gamma} - \frac{k_B T}{e} ln\left(\frac{I(V)}{AA * T^2}\right), \tag{7}$$

where γ is the first integer (dimensionless) greater than n. factor, $I(V)$ is current obtained from the I-V curve and the other parameters are described above. From Norde's functions, the effective barrier height and R_s value can be determined as

$$\Phi_b = Fm + \left[\frac{(\gamma - n)}{n}\right]\left[\frac{V_m}{\gamma} - \frac{k_B T}{e}\right], \tag{8}$$

$$R_s = (\gamma - n)\left(\frac{k_B T}{e I_m}\right). \tag{9}$$

Figure 7 shows plots of $F(V)$ as a function of V of the Cd/CdSe/n-Si/Au-Sb structure as a function of SILAR cycle. From the F(V)-V plots, the some parameters of the Cd/CdSe/n-Si/Au-Sb sandwich structure, (Φ_b, R_s) have been determined. From these F(V)-V curves, the barrier height and series resistance values have been shown in Table 1. It is seen that the values of the series resistance have lightly changed with increased SILAR cycle.

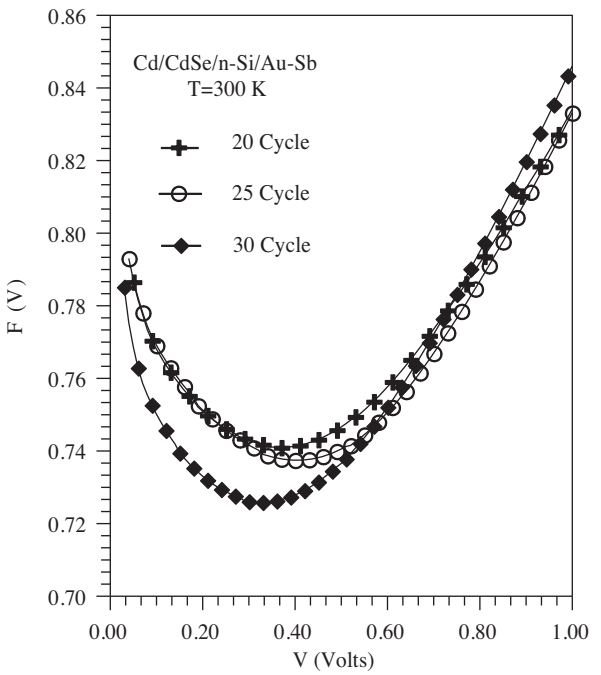

Figure 7. Experimental F(V)-V curves of Cd/CdSe/n-Si/Au-Sb sandwich structure as a function of SILAR cycle.

The interface states N_{ss} is given by [32]

$$N_{ss} = \frac{1}{e}\left[\frac{\varepsilon_i}{\delta}(n(V) - 1 - \frac{\varepsilon_s}{W_D}\right], \tag{10}$$

where ε_s and ε_i are the permittivity of the CdSe layer and the semiconductor, respectively, δ is the thickness of CdSe layer and W_D is the width of the space charge region. The CdSe layer thickness δ was obtained from high frequency (1 MHz) CV characteristics using the equation for insulator layer capacitance $C_{ox} = \frac{\varepsilon_s \varepsilon_i A}{\delta}$, where $\varepsilon_i = 3.8\varepsilon_0$. The W_D was also calculated CV characteristic at 1 MHz using the equation for the width of the space charge region, $W_D = \left(\frac{2\varepsilon_s \varepsilon_i V_d}{eN_D}\right)^{1/2}$ and V_d is the diffusion potential [4, 33]. Thus, the CdSe layer thickness were calculated as 342 nm, 364 nm and 391 nm, respectively.

Furthermore, in n-type semiconductors, the energy of the interface states E_{ss} with respect to the bottom of the conduction band at the surface of semiconductor is given as

$$E_c - E_{ss} = e(\Phi_b - V). \tag{11}$$

The dependence of N_{ss} values on the bias was obtained using equations (2) and (10), and then the dependence of N_{ss} on the bias was converted to a function of E_{ss} using Equation (11). That is, the curves obtained by taking into account the bias dependence of the ideality factor, barrier height and reverse bias of the saturation current are given in Table 1. The interface state energy distribution curves of the Cd/CdSe/n-Si/Au-Sb structure as a function of SILAR cycle are given in Figure 8. As can be seen from Figure 8, the interface state density N_{ss} has an exponential rise with bias from the midgap towards the top of the conduction band for each cycle. In the same time, the interface state density (N_{ss}) have lightly changed with increasing SILAR cycle.

According to Figure 9, the variation of the rectifying ratio with as a function of SILAR cycle can be given easily for Cd/CdSe/n-Si/Au-Sb structure. It can be seen from Figure 9 that the values of the rectifying ratio measurement of Cd/CdSe/n-Si/Au-Sb structure have lightly changed with increased SILAR cycle.

3.3. Capacitance-voltage characteristics

When a small ac voltage is superimposed on the dc bias, charges of one sign are induced on the metal surface and charges of the opposite sign in the semiconductor. Figure 10 and 11 show the plots of C-V and C^{-2}-V versus forward and reverse bias voltage applied to Cd/CdSe/n-Si/Au-Sb structure at 300 kHz as a function of SILAR cycle. At the MS contact, the depletion layer capacitance can be expressed as

$$C^{-2} = \frac{2\,(V_d + V)}{\varepsilon_s \varepsilon_0 e A^2 N_d}, \tag{12}$$

where A is the area of the diode, ε_s is the dielectric constant of the semiconductor, ε_0 is the permittivities of the free space, V_d is the diffusion potential at zero bias, N_d is the donor concentration. Using the Schottky barrier approximation and taking into consideration the assumption of a locally independent N_d one can determine V_d from C^{-2}-V curves as a function of applied voltage [1, 34, 35].

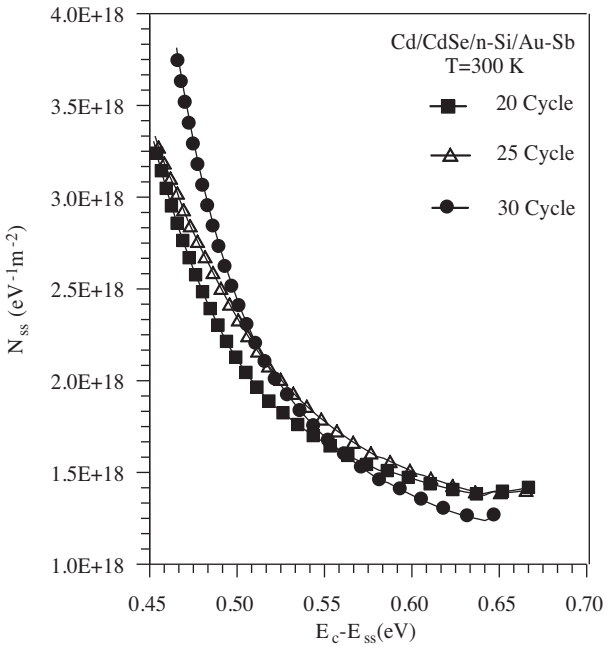

Figure 8. The energy distribution curves of the interface states obtained from the I-V characteristics as a function of SILAR cycle.

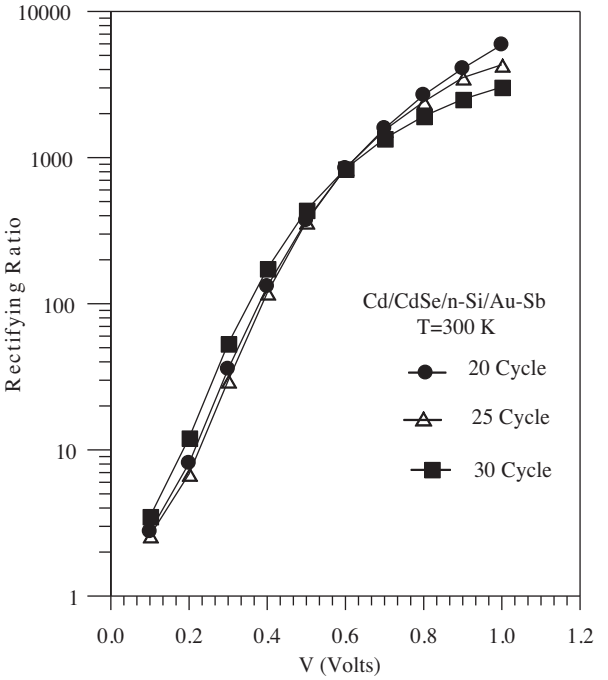

Figure 9. The rectifying ratio versus applied voltage for Cd/CdSe/n-Si/Au-Sb structure as a function of SILAR cycle.

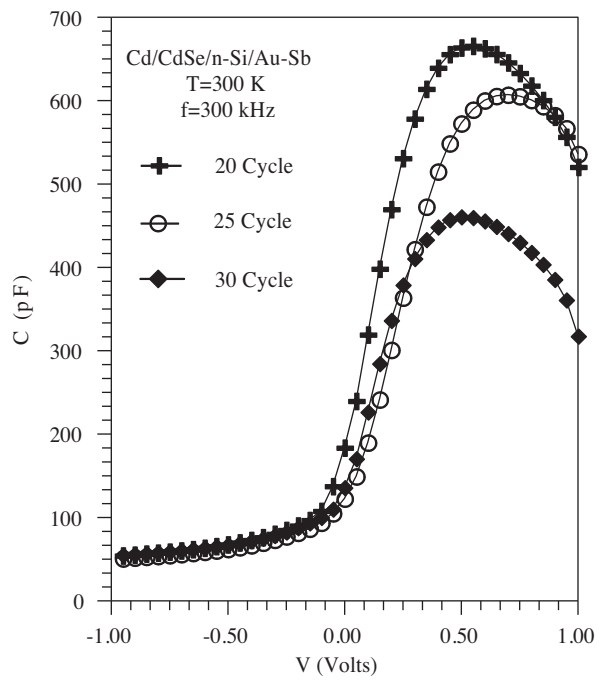

Figure 10. The forward and reverse bias C-V characteristics of the Cd/CdSe/n-Si/Au–Sb structure as a function of SILAR cycle.

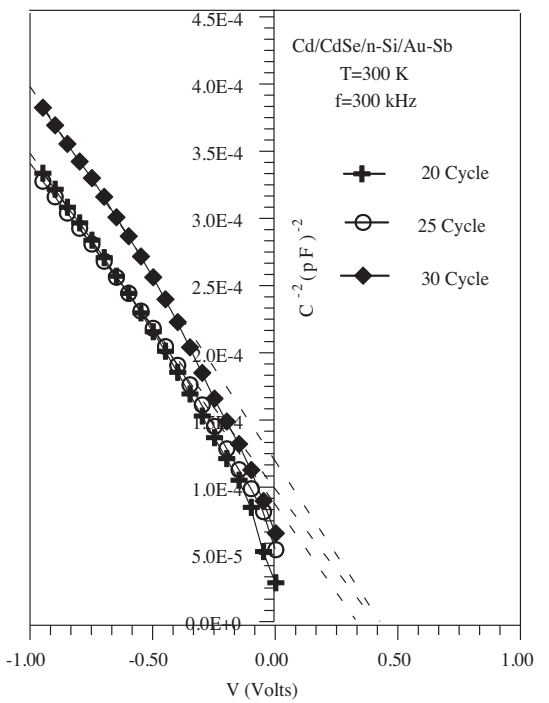

Figure 11. The reverse bias C^{-2}-V characteristics of the Cd/CdSe/n-Si/Au-Sb structure as a function of SILAR cycle.

The value of the barrier height can be calculated by the help of the relation $\Phi_b = V_d + V_n$ using $C-V$ measurements. Here, V_n is the potential difference between the Fermi energy level E_f and the bottom of the conduction band in the neutral region of n-Si, which is directly equal to E_f and can be calculated by knowing N_d and N_c, density of states in the conduction band ($N_d = N_c \exp\left(\frac{V_n}{k_B T}\right)$). The values of V_d, N_d, V_n and Φ_b are shown as a function of SILAR cycle in Table 2. It can be seen from Table 2 that the values of the barrier heights of Cd/CdSe/n-Si/Au-Sb structures have lightly increased with changed SILAR cycle.

Table 2. The experimental values of parameters obtained from C^{-2}–V characteristics of Cd/CdSe/n-Si/Au-Sb structure with increasing SILAR cycle.

Cd/CdSe/	C-V Method (300 kHz)			
n-Si/Au-Sb	V_d (eV)	N_d (cm^{-3})	V_n (eV)	Θ_b (eV)
20 Cycle	0.437	2.691E+14	0.235	0.672
25 Cycle	0.439	3.620E+14	0.235	0.674
30 Cycle	0.441	2.732E+14	0.234	0.675

As can be seen from the mean values, the barrier height calculated from the I-V characteristics is not equal to the barrier height extracted from C-V characteristics. Both techniques are differently sensitive to possible occurance of inhomogeneities and especially small patches with a lower Schottky barrier height at the contact, strongly influences the resulting appearent Schottky barrier height. On the other hand, barrier heights calculated from the C-V measurements has a tendency to be an average value of the Schottky barrier heights of patches present in the contact (barrier height inhomogeneities that are present in the CdS/n-Si interface), that is, average barrier height is the mean value of the barrier minima plus barrier maxima [36].

4. Conclusions

In this study, Cd/CdSe/n-Si/Au-Sb structures have been fabricated by the Successive Ionic Layer Adsorption and Reaction (SILAR) method. The I-V and C-V characteristics of Cd/CdSe/n-Si/Au-Sb structures have been investigated as a function of SILAR cycle. The characteristic parameters such as barrier height, ideality factor, series resistance, density distribution of structure are calculated from the I-V measurement, the barrier height, carrier concentration are calculated from reverse bias C^{-2}-V measurement have showed little changing effect with respect to increasing SILAR cycle.

Acknowledgment

This work was supported by The Turkish Scientific and Technological Research Council (TUBITAK) (Project Number: 108T500). The Authors wish to thank to TUBITAK for their support.

References

[1] E. H. Rhoderick and R. H. Williams, *Metal-Semiconductor Contacts*, 2nd ed.Oxford University Press, Oxford, (1988).

[2] R. F. Pierret, *Semiconductor Device Fundementals*, Purdue University Press, (1996).

[3] L. J. Brillson, *Handbook on Semiconductors*, edited by P. T. Landsberg, North Holland, (Amsterdam, 1992).

[4] S. M. Sze, *Physics of Semiconductor Devices*, 2nd ed., Wiley, (New York, 1981).

[5] De Vrieze, K. Strubbe, W. P. Gomes, S. Forment, R. L. Van Meirhaeghe, *Phys. Chem. Chem. Phys.*, **3**, (2001), 5397.

[6] A. Keffous, M. Siad, S. Mamma, Y. Belkacem, C.L. Chaouch, H. Menari, A. Dahmani, W. Chergui, *Appl. Surf. Sci.*, **218**, (2003), 336.

[7] S. Forment, R. L. Van Meirhaeghe, A. De. Vrieze, K. Strubbe, W. P. Gomes, *Semicond. Sci. Technol.*, **16**, (2001), 975.

[8] H. Bayhan, A. S. Kavasoglu, *Solid-State Electron.*, **49**, (2005), 991.

[9] M. Okutan, E. Basaran, F. Yakuphanoglu, *Appl. Surf. Sci.*, **252**, (2005), 1966.

[10] M. Lonergan, *Annu. Rev. Phys. Chem.*, **55**, (2004), 257

[11] T. Okumura and C. Kaneshiro, *Electron and Commun.*, **82**, (1999), 5.

[12] B. R. Sankapal, R. S. Mane, C. D. Lokhande, *Mater. Res. Bull.*, **35**, (2000), 177.

[13] M. P. Valkonen, T. Kalliainen, S. Lindross, M. Leskela, F. Rauhala, *Appl. Surf. Sci.*, **115**, (1997), 386.

[14] R. Resch, G. Friedbacher, M. Grasserbauer, T. Kanniainen, S. Lindross, M. Leskala, L. Niinisto, *Appl. Surf. Sci.*, **120**, (1997), 51.

[15] S. D. Sartale, C. D. Lokhande, *Mater. Chem. Phys.*, **65**, (2000), 63.

[16] S. D. Sartale, C. D. Lokhande, *Ind. J. Pure Appl. Phys.*, **38**, (2000), 48.

[17] R. C. Kainthala, D. K. Pandya, K. L. Chopra, *J. Electrochem. Soc.*, **127**, (1980), 277.

[18] R. A. Baudreau, R. D. Rauh, *J. Electrochem. Soc.*, **130**, (1983), 513.

[19] A. Mondal, T. K. Chaudhri, P. Pramanik, *Solar Energy Mater.*, **7**, (1983), 431.

[20] S. S. Dhumure, C. D. Lokhande, *Ind. J. Pure Appl. Phys.*, **31**, (1993), 512.

[21] S. A. Jodgudri, C. D. Lokhande, *Ind. J. Phys. A*, **70**, (1996), 477.

[22] V. M. Garacia, M. T. S. Nair, P. K. Nair, R. A. Zingaro, *Semicond. Sci. Technol.*, **10**, (1993), 427.

[23] K. Grija, S. Thirumalairajan, S. M. Mohan and J. Chandrasekaran, *Chalcogenide Letters*, **6**, (2009), 351.

[24] Daoli Zhang, Jianbing Zhang, Qiming Wu, and Xiangshui Miao, *J. Am. Ceram. Soc.*, **93**, (2010), 3284.

[25] L. Maissel, R. Glang Eds.., *Handbook of Thin Film Technology*, Mc Graw-Hill, (New York, 1970), p. 662.

[26] H. Tsai, D. B. Bogy, *J. Vac. Sci. Technol.*, **5**, (1987), 3287.

[27] A. F. Özdemir, A. Kökçe, A. Türüt, *Appl Surface Sci.*, **191**, (2002), 188.

[28] M. Sağlam, E. Ayyıldız, A. Gümüş, A. Türüt, H. Efeoğlu, S. Tüzemen, *Appl. Phys. A.*, **269**, (1996), 22.

[29] S. K. Cheung, N. W. Cheung, *Appl. Phys. Lett.*, **49**, (1986), 85.

[30] H. Norde, *J. Appl. Phys.*, **50**, (1979), 5052.

[31] K. E. Bohlin, *J. Appl. Phys.*, **60**, (1986), 1223.

[32] H. C. Card, E. H. Rhoderick, *J. Phys. D*, **4**, (1971), 1589.

[33] M. Saglam, A. Ates, M. A. Yıldırım, B. Güzeldir, A. Astam, *Current Appl. Phys.*, **10**, (2010), 513.

[34] V. Ziel, *Solid State Phys Elec.* 2nd ed, Englewood Cliffs, NJ: Prentice-Hall, (1968)

[35] Z. Horvath, *J Appl Phys.*, **63**, (1988), 976.

[36] J. Osvald, *J. Appl. Phys.*, **85**, (1999), 1935.