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Processing of germanium for integrated circuits

Ray DUFFY*, **Maryam SHAYESTEH**, **Ran YU**
Tyndall National Institute, University College Cork, Lee Maltings, Cork, Ireland

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Abstract: In this review paper the authors will focus on Ge processing for integrated circuits. The key areas that require the most attention are substrates and integration, gate dielectrics, and access resistance. We will discuss each of these topics in turn, while also reviewing the most scaled Ge field-effect-transistor devices, and consider how modelling activities have matured for Ge in recent years.

Key words: Semiconductors, Germanium, Processing, Substrates, Integration, Dielectrics, Resistance, Field-effect-transistors

1. Introduction

It is a well-established fact that silicon (Si) has had many good years as the main material in digital electronic technologies, but it is facing stiff competition from other semiconductor materials that may one day replace it in the channel of the field-effect-transistor (FET) device. High carrier mobility materials, such as germanium (Ge), III-V compounds like InGaAs, graphene, and transition metal dichalcogenides (TMDs), are current candidate materials to replace Si channels. In simple terms, higher electron and hole mobilities could lead to performance gain or power saving in digital applications. Considering how large and wide-spread the handheld portable consumer electronics market has become, the impact could be very far-reaching. Mobile phone and tablet device microprocessors are currently the fastest growing segments of the electronics market [1].

One key concern about using these alternate channel materials is whether they can be integrated into the Si manufacturing process without losing the intrinsic properties that make them attractive in the first place. Due to the massive investment in existing infrastructure and the mechanical strength of Si, it is likely that 300 and 450 mm wafers can only ever be produced from Si, and thus any alternate channel material must be integrated onto that.

In this review paper we will focus on Ge processing for integrated circuits. The key areas that require the most attention are :

- Substrates and integration,
- Gate dielectrics,
- Access resistance.

We will discuss each of these topics in turn, while also reviewing FET device state-of-the-art for Ge, and consider how modelling activities have matured for Ge channel FETs in recent years.

*Correspondence: ray.duffy@tyndall.ie

One might argue that, before comparing Ge device processing and performance with Si, we should first consider the body of research work behind both materials. Ge is definitely less mature than Si. Using the number of publications as a metric, Figure 1 shows the number of hits from the literature search tool Scopus, the abstract and citation database of peer-reviewed literature from Elsevier [2], using the search terms "Silicon devices", "Germanium devices", "InGaAs devices", "Graphene devices", and "TMD devices". First and foremost, Si has the largest volume of work, Ge has grown steadily since the 1960s, InGaAs had a growth spurt in the 1970s but plateaued in the 21st century, TMDs have emerged recently, and graphene has rocketed up since the mid-2000s. Figure 2 shows an alternate analysis of this data where the year-on-year percentage change in number of publications is plotted. This graph highlights where early work began for many of the materials, as that corresponds to a largely oscillating curve during that early era for each material. The exception is perhaps Ge, where the growth has been more steady year-on-year. The popularity in Ge research enjoyed growth in 2003 and 2004. Since then, publications have grown steadily. Many breakthrough papers have emerged across the world, as Ge technology and understanding has steadily matured. For all this excellent work, Ge is still well behind Si in terms of knowledge and experience, and a variety of methodologies applied to Si remain underdeveloped or unreported in Ge substrates and devices. This point will become obvious as we discuss the different aspects of processing and device optimisation in this paper.

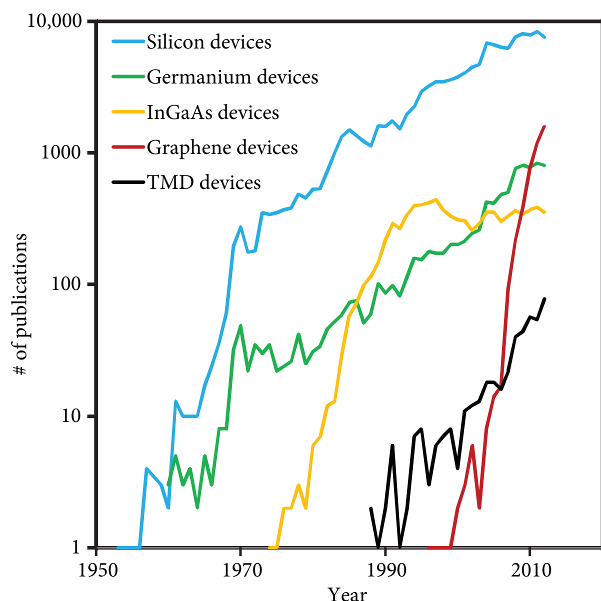

Figure 1. Number of publications on the topics of "Silicon devices", "Germanium devices", "InGaAs devices", "Graphene devices", and "TMD devices" according to the search results from www.scopus.com.

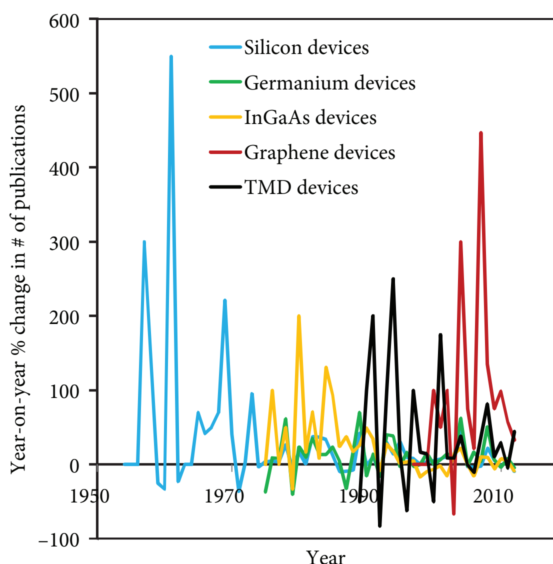

Figure 2. Year-on-year % change in number of publications on the topics of "Silicon devices", "Germanium devices", "InGaAs devices", "Graphene devices", and "TMD devices" according to the search results from www.scopus.com.

Integrating and optimising a new material or replacing Si at the heart of the transistor, the channel of a FET, is a substantial scientific challenge, but it is also a huge economic undertaking. Manufacturing processes are very costly to alter in any industry, especially in the semiconductor processing industry, and particularly in the high-end microprocessor market. Inertia invades the thinking of the manufacturing divisions of large companies when it comes to large shifts in technology. Process engineers would rather evolve the technology

than scrap one and start a new one. Thus, they would like to change as little as possible when transitioning from one technology generation to the next. The suggestion to replace one channel material (Si) with another (Ge) therefore takes a long time, in order to convince everyone of the economic merits of doing so. This does not come as a surprise when one counts the enormous investment in infrastructure the manufacturing companies have made.

Having said all that, most major microprocessor manufacturers take high mobility materials very seriously, and although no announcements have been made yet of an advanced complimentary-metal-oxide-semiconductor (CMOS) technology with pure Ge, InGaAs, or TMD channels, it is just a question of time.

2. Highly scaled GE FETs

Before we delve into the Ge processing modules, we should first take a step back to look at the most advanced and scaled Ge devices that have been published to date. Note that it is generally accepted that future semiconductor FET devices will progress toward ultrathin body channels. In other words, the device is essentially fabricated from a thin layer of material, perhaps sub-20 nm thick. The benefit is that small devices can be made that yield higher performance and greater energy efficiency. Thin-body device architectures include ultrathin semiconductor-on-insulator, double or tri-gate multi-gates, and nanowires. Over the last couple of years FinFETs have become mainstream but still comprise Si and SiGe channels. Thus, while there have been many very good Ge device papers using the planar CMOS architecture, we will focus on the thin-body devices here as that is the direction in which the industry is heading.

Ge FinFET devices have been limited to p-type channels, with ion implantation used for source/drain doping. Feng et al. fabricated Ge p-channel FinFETs with fin widths (W_{fin}) down to 130 nm [3]. Van Dal et al. recently described scaled p-channel Ge FinFET devices with W_{fin} of 40 nm, fabricated on a Si bulk wafer using the aspect-ratio-trapping technique, which will be discussed in the next section [4,5]. Liu et al. reported p-type Ge FinFET devices with W_{fin} = 60–100 nm and a summary of the best literature data for Ge FinFETs in terms of drive versus gate length [6]. Finally, Ikeda et al. fabricated p-type Ge nanowire FET devices with W_{fin} = 20 nm [7]. They also benchmarked recent devices in accordance with W_{fin}, device architecture, gate length, and drive current.

The question remains whether or not scaled Ge FETs can outperform the equivalent Si FET device. Although the answer to that might be unclear from an experimental standpoint at the moment, Eneman et al. performed a very insightful analysis comparing Ge with Si FinFETs in the presence of strain [8]. Their modelling analysis concluded that relaxed Ge p-FinFETs cannot outperform strained Si, but require a mobility boost to do so, possibly through embedded stressors. For Ge n-FinFETs, relaxed channels already outperform strained Si primarily due to favourable fin sidewall mobility. Adding stressors increases that benefit to more than double the Si performance in terms of mobility.

3. Substrates and integration

One of the first problems of integration involves the mechanical strength of Ge. Essentially, a Ge wafer on the scale of 300 or 450 mm would not be strong enough to survive the auto-feed handling involved in integrated circuit processing. Wafers of this size would simply shatter. In fact, having worked with 100 mm Ge wafers for many years, these authors are very aware of the mechanical strength limitations of working with Ge, as we have experienced many wafer breakages, even caused by the softest touch.

The solution to this is to put Ge onto a Si handle wafer, as Si is mechanically strong enough for 450 mm

wafer processing. The question is how to place the Ge on the Si substrate without compromising the inherent material properties that made us choose Ge in the first place. The main options can be listed as epitaxial growth of some sort, the condensation technique, and substrate transfer by localised bonding.

Much work involves forming strain-relaxed Ge on Si substrates. Epitaxial integration of Ge on Si is limited by the mismatch of approximately 4% between the crystal lattices, which leads to the formation of misfit dislocations when the growing layer surpasses a critical thickness in the order of 1 nm [9]. Kim et al. described an alternate guideline for critical thickness for high Ge content $Si_{1-x}Ge_x$ grown on Si, and they predicted a critical thickness of 2–3 nm 100% Ge on Si [10]. In general, this thickness is too small to be practical for today's technologies. Hence, we need to find techniques that can grow Ge on Si above the critical thickness.

The side effect of this epitaxial process above the critical thickness is the formation of defects, which can adversely affect electrical performance in terms of increased leakage and reduced carrier mobility. Nguyen et al. used reduced pressure chemical vapour deposition (CVD) of Ge on (110) and (111) Si substrates in combination with thermal treatments in the range of 400–830 °C, which showed some dramatic looking cross-sectional transmission electron microscopy (XTEM) images of nasty looking threading dislocations [11]. One conclusion from that work was that (110) orientations look more promising than (111) for that particular technique. Yamamoto et al. proposed a processing methodology to reduce the threading dislocation density in Ge layers grown on Si, namely reduced pressure CVD in combination with HCl etching [12]. Lieten et al. used a solid phase epitaxy (SPE) process of amorphous Ge on (111) Si to form Ge on Si substrates [13]. The Ge was deposited by plasma enhanced chemical vapour deposition, and a thermal anneal produced crystallisation using the Si wafer as a template. On the positive side, this is a very straight-forward and economical process; however, mobility was not as high as bulk Ge and may be linked to the strain-relaxation-induced defects. In a follow-up work the same authors determined that incorporation of H during deposition of amorphous Ge can improve the SPE quality [14]. Furthermore, in a device study Jin and Chang determined that a forming gas anneal (10% H_2) at 500–600 °C is beneficial for carrier mobilities in GeOI [15].

As a side note, a review paper by Claverie et al. discussed much of the SPE physics of Ge and included a very useful recrystallisation rate versus anneal temperature plot [16]. Johnson et al. experimentally determined that intrinsic Ge SPE rates have an activation energy of 2.15 eV [17].

An alternative technique to form Ge layers uses the condensation technique. In short, a SiGe layer is grown on a Si handle wafer and subsequent oxidation of the SiGe removes Si atoms, leaving behind only the Ge atoms. Thus, the SiGe layer is transformed into Ge. (110)-oriented compressively strained (1.1%) GeOI layers with Ge thickness of 12 nm have been demonstrated [18]. This is not as popular as other techniques for integrating Ge on Si, which is somewhat surprising as it is relatively straight-forward. There may be some concern about the ability to achieve 100% Ge.

One very promising approach that has been implemented by many groups is liquid phase epitaxy of Ge between nitride and oxide layers. Amorphous Ge is deposited and then raised above the melting temperature of 937 °C. Upon cool-down the liquid Ge crystallises, starting from the Si handle wafer seed, which is normally accessed by a window etched in the nitride layer prior to Ge deposition. Often no twin boundaries are seen in the bulk of the Ge layer, except only close to the Si substrate seed. The Si handle wafer determines the Ge orientation, as Ge (100) and (111) were experimentally demonstrated by Liu et al. [19]. Furthermore, Toko et al. comprehensively studied seeded rapid-melting-growth (RMG) of amorphous Ge to obtain GeOI stripes on SiO_2 using (100), (110), and (111) Si templates [20]. Hashimoto et al. fabricated Ge wires 44 μm long by growing

laterally on L_2O_3 rather than SiO_2 [21]. The authors explained the improvement based on a suppression of the random nucleation mechanism.

Cammilleri et al. experimentally demonstrated seeded growth of Ge on Si via ultrahigh-vacuum CVD using germane (GeH_4) diluted at 10% in H_2. The Ge layer was primarily clean of defects except near the Ge-Si interface, and faceted growth was observed in XTEM [22]. Terzieva et al. showed that high temperature annealing at 800 °C can reduce threading dislocation densities in CVD Ge layers grown on Si substrates [23]. Care must be taken at high temperatures as Si out-diffusion may occur along with SiGe formation. Balakumar et al. used sputtered Ge on a nitride mask, again with a window etched to reach a Si seed [24]. In that work, a high temperature anneal at 925 °C was used to stimulate lateral epitaxy. Finally, Huang et al. produced single-crystal Ge films on Si prepared by electrodeposition and crystallised by SPE during a forming gas annealing process [25].

A twist on the lateral epitaxy method is metal-induced lateral crystallisation (MILC), where Ni or Au is incorporated in the Ge to reduce the required processing temperature. Park et al. demonstrated this with anneals at 360 °C [26]. Furthermore, Pd-induced crystallisations at 350 °C were used for poly-Ge formation [27]. The uptake of this approach is open to question, however. These metal atoms could potentially diffuse into the active regions of the device, which may lead to leakage current. It is well known that impurities located in the depletion region of a junction, for example, can increase trap-assisted-tunnelling currents. The MILC approach would require careful integration to ensure that this event does not occur.

Another body of work surrounds the formation of poly-Ge for thin-film transistor applications [28,29]. Typically, the Ge layer is deposited by CVD or molecular-beam epitaxy. RMG forms a quasi-single-crystal Ge from a poly-Si seed or a quartz substrate. Better hole mobilities were achieved compared to SPE on a poly-Si seed, and compared to the condensation method on single-crystal Si seed [30].

An important variation on the theme of Ge epitaxial growth, particularly for multi-gate-field-effect-transistors (MugFETs) is Ge growth in trenches. The trenches are formed in SiO_2 by a shallow-trench-isolation process. Optimisation is required to avoid stacking fault defects, and high temperature anneals for melt and regrowth can cure the defects [31,32]. Alternatively, if narrow trenches are used, the defects can be captured by what is known as aspect-ratio-trapping (ART). As stated previously, van Dal et al. reported scaled p-channel Ge MugFET devices with fin widths of 40 nm, fabricated on a Si bulk wafer using the ART technique [4,5]. Earlier work developing this process was done by Loo et al. and Park et al. [33,34].

Finally, bonding of Ge exfoliated layers onto SOI wafers to form GeOI is another important technique. Much like the formation of SOI wafers, it relies on H-implantation, low-temperature annealing to form subsurface voids, exfoliation, bonding to a handle wafer, and chemical-mechanical-polishing to planarise the top surfaces. Ferain et al. characterised the Ge exfoliation process for substrate transfer [35]. David et al. characterised extended defects visible in Ge, related to the H implantation [36]. As a final note, GeOI wafers are now available for purchase from a well-known wafer supplier who specialises in exfoliation, substrate transfer, and bonding.

At this point in time, many of the microprocessor companies have different philosophies on the integration of Ge onto a Si handle wafer. The ultimate choice is not clear for now and may even depend on the FET device architecture in a particular technology. The ART technique may work well for FinFETs, while bonding may allow the technique to be used if planar GeOI is the desired platform.

4. Gate dielectrics

One of the most challenging issues in establishing Ge CMOS technologies is to realise good quality Ge dielectric interfaces with a low interface state density (D_{it}), which is critical to achieve low subthreshold slope, high carrier mobility, and associated high current drive. Unlike the Si system, the oxide of Ge (GeO_2) is an unpleasant and unhelpful material that has very poor properties for transistor manufacturing. One of the problems is that GeO_2 transforms into GeO, which desorbs at annealing temperatures of >420 °C [37]. Takahashi et al. did a systematic experiment showing GeO_2 desorption only when in contact with the Ge substrate. The conclusion is that Ge atoms need to be supplied by the substrate in order to drive the GeO_2 transformation into GeO [38]. One could extrapolate that the GeO desorption effect not only causes loss of GeO_2, but also causes loss of the underlying Ge substrate. Recently Oniki et al. did a Ge/GeO_2 desorption study with thermal desorption spectroscopy [39]. The authors found that oxide desorption occurs above 400 °C, but was pushed down to 300 °C in the presence of a metal catalyst.

Different attempts have been made to form a dielectric layer on Ge with low interface states. They include approaches with various types of interfacial layers such as Si [40,41], GeO_2 [42-45], oxynitrides [46–49], and different high-k dielectric materials [50–52]. Novel processes have been investigated, i.e. sulphur passivation [42], high pressure thermal oxidation [53,54], vacuum ultraviolet-assisted oxidation [55], plasma oxidation [56,57], radical oxidation [58,59], direct neutral beam oxidation [60], plasma postoxidation [61], and thermal molecular oxidation [62].

Among the different types of proposed MOS systems, GeO_2/Ge interfaces have recently been explored, both experimentally and theoretically, in order to provide low density interface defects and have been used to create high-performance MOSFETs [63,64]. Although GeO_2 is not as physically stable a material as SiO_2, GeO_2/Ge shows the similar bonding constraint as its counterpart SiO_2/Si system in terms of a large spread in bond angle and a random distribution of dihedral angles [65]. Moreover, similar to the high-k/Si system, which has an interfacial SiO_2 layer, a GeO_2 interfacial layer can be used to maintain a good interface condition for the high-k dielectric/Ge structure. Thus, GeO_2 has been recently reinvestigated as one of the promising candidates for Ge surface passivation. High quality GeO_2/Ge interfaces fabricated by conventional thermal furnaces have been reported for MOS structures and planar devices. On the other hand, rapid thermal oxidation, due to its small thermal budget, which results in a thin GeO_2 layer grown, shows promise and has been used for Ge nanowire devices [66].

A few other novel approaches have been reported recently that show potential and deserve special mention. Kita et al. reported that a combination of high-pressure oxidation and low-temperature oxygen annealing is the most suitable for Ge/GeO_2 stack formation [67]. This report was followed by several others by the same group where the processes were developed further [68,69] Toriumi et al wrote a review of their group's work, which is a useful reference guide to that topic [70].

Finally, among the scaled FET device community HfO_2 currently appears to be the high-k dielectric of choice. This is true of the scaled FETs discussed in Section 2. However, notable literature studies of alternative high-k dielectrics can also be found. Guo et al. reported work on $LaLuO_3$ high-k dielectric with a thermally grown GeO_2 interfacial layer. Wu et al. experimentally looked at ZrO_2, again in combination with a GeO_2 interfacial layer, to improve electrical performance. Finally, Bellenger et al. recently presented a GeO_2/AlO_3 gate stack for n-type MOS Ge devices [71].

In conclusion, a multitude of high-k dielectrics have been explored, and much like for Si, HfO_2 is popular

candidate material. Overall, the work on high-k dielectrics on Ge has followed many of the trends of Si technology. This is perhaps a good example of how Ge technology has benefited from the many years of work on Si and has reused the knowledge and insight built up in this area.

5. Access resistance

5.1. Doping optimisation

In terms of introducing dopant impurities into Ge substrates and into the source/drain regions of Ge MOSFETs, by far and away the most common approach is ion implantation, and many exciting techniques demonstrated in Si have yet to be developed in Ge. Almost all literature dopant studies describe ion implanted B, Ga, P, As, or Sb into bulk Ge substrates. For the n-type dopants, the shallowest profiles have been produced by 5 keV As implants [72]. For the p-type dopants, the shallowest profiles have been produced by 2 keV B implants [73]. From a technological point of view, the most commonly used dopants are P or As for n-type regions, while it appears that B or BF_2 implantation is favoured for p-type regions.

Overall, there has been just a single report of plasma doping of Ge by Heo et al. [74] Considering the popularity of plasma doping in Si devices over the past decade [75,76], it is certainly surprising that not more has been done in this area for Ge. Care has to be taken to avoid the known Ge surface voiding problem [77,78] and any attack of thin-body Ge by the plasma species. Other areas that are somewhat underdeveloped for Ge include cold implants, hot implants, co-implants, and vacancy engineering, which could be grouped under the heading of "point defect engineering". Essentially, interstitial and vacancy point defects may cause dopant diffusion or may hinder dopant activation and thus must be carefully controlled.

Colder wafer temperatures enhance the likelihood of amorphisation as dynamic annealing is reduced, and thus damage build-up is promoted [79,80]. At colder temperatures point defects are less mobile; thus, an interstitial defect has less energy to move and meet a vacancy point defect with which it can recombine. As a result, implants used at cryogenic temperatures are an alternative to traditional preamorphising implants. The opposite of this is heating the wafer during implantation, as a method to promote dynamic annealing and thus the suppression of amorphisation. There have been a number of publications in this field for Si recently [81,82]. The drawback is that a special hard mask must be used, as the temperatures required to stifle amorphisation are higher than what photoresist can tolerate.

Experimental reports of hot implants or cold implants applied to Ge substrates are difficult to find. While end-of-range (EOR) defects are less likely to be a problem in Ge compared to Si, amorphisation of Ge is more likely than Si, and in thin-body Ge hot implants may bring a performance benefit. Note that the EOR is an interstitial-type (i.e. nonsubstitutional atoms in the host substrate) defect band, just beyond the peak of the implanted profile. During any subsequent thermal step, EOR defects dissolve and emit interstitials, which subsequently diffuse and then may interact negatively with the active dopant profile. Thus, from this aspect, Ge is an easier material to work with than Si.

The concept for co-implantation can be described as the introduction of nondopant species in order to locally control the point-defect concentrations in the presence of dopants, in order to boost dopant activation and suppress dopant diffusion. For example, in Si at certain high concentrations, F will cluster with vacancy point-defects to form F_nV_m clusters. Alternatively, if C is favoured, a region of high concentration substitutional C can be formed using preamorphisation and rapid-thermal-anneal processing. Both the F_nV_m clusters and substitutional C are very effective in trapping interstitial point defects that may happen to come along. If correctly positioned, this interstitial barrier can protect dopant profiles from interstitial-driven deactivation or diffusion [83,84].

The premise is the same for Ge. Chroneos and Bracht's recent review describes the theory of point defect engineering in Ge in great detail [85], including the influence of co-implant impurities. Experimental studies have also demonstrated the value of co-implants in Ge under certain circumstances, although to date it appears that they are less effective in Ge than they have proven to be in Si. N implants have been shown experimentally to reduce P diffusion in Ge [86]. C also reduces P diffusion in Ge [87]. El Mubarek demonstrated the impact of F on P profiles in the 400–500 $^\circ$C temperature range [88]. Furthermore, it was shown experimentally that F co-implants can affect the diffusion of low-dose As implants [89].

Vacancy engineering typically relies on a high keV or MeV implant to create a region rich of vacancies close to the surface of the semiconductor. Strengths and limitations of the vacancy engineering approach for the control of dopant diffusion and activation in Si were reviewed recently by Claverie et al. [90] The enrichment with vacancies close to the Si surface can be obtained by inert impurity implantation at high energy [91]. Transient enhanced diffusion suppression of B in Si with high energy Si co-implants was demonstrated experimentally [92].

This technique is relatively unexplored in Ge. Perhaps it is considered unnecessary due to the relative abundance of vacancies in Ge. Conversely, perhaps the scientific community needs to focus on "interstitial engineering" in Ge in order to create an excess of interstitial point defects.

After the dopants are introduced to the Ge substrates, an annealing step is required to activate them and repair any damages that may have been caused to the semiconductor crystal. Much like the doping schemes discussed previously, many advanced techniques that have been well explored in Si substrates and devices are relatively immature in Ge substrates and devices. Most of the published data have been generated by furnace anneal or rapid thermal anneal (RTA).

Relatively recently, however, reports have emerged applying laser thermal anneal (LTA) to Ge, although to date this has only been applied to planar substrates and not yet to more topographical structures such as FinFETs and nanowires. It has been demonstrated that dopant activation and contact resistance can be dramatically improved by LTA in the melt regime [72,93–98]. Control of melt-depth is done by changing laser energy density. Another variable includes the number of laser pulses applied to the substrate. One of the highlights for dopant activation was the work of Bruno et al., which showed Sb solubility ($>10^{21}$ cm^{-3}) after LTA, extracted using Rutherford backscattering spectroscopy [94].

Furthermore, Theraja et al. [99] combined Sb with LTA producing active dopant concentrations of up to 10^{20} cm^{-3}, specific contact resistivity (ρ_c) of $7 \times 10^{-7}\Omega$ cm^2, and diode $I_{ON}/I_{OFF} > 10^5$. One of the issues with Sb in Ge is the control of diffusion while repairing the high implant damage from the heavy Sb ions. Sb is a faster diffuser than both P and As in Ge. Martens et al. used LTA in combination with As implants and NiGe to achieve $\rho_c = 8 \times 10^{-7}\Omega$ cm^2. When 600 $^\circ$C RTA was used for the As implant, ρ_c was $1 \times 10^{-6}\Omega$ cm^2 [100].

Flash lamp annealing (FLA), which has been advantageous for dopant activation in Si for many years, is only beginning to be explored in Ge substrates. Considering the encouraging results demonstrated experimentally using LTA, it should be expected that FLA will also produce positive results for dopant activation, contact resistance, and consequently device performance.

As the melting point of Ge is 937 $^\circ$C, a low-temperature process such as solid-phase-epitaxial-regrowth (SPER) appears to be another solution [101]. Furthermore, SPER can be done with standard furnace tools. Moreover, SPER techniques have generated low sheet resistance for both n-type and p-type doped layers

[102,103]. Dopant snowploughing has been observed for P during SPER at 350 °C [104], so care must be taken when optimising the dopant profile under those circumstances.

A word of caution is necessary with the LTA, FLA, and SPER approaches with respect to dopant activation. These techniques should generate above-equilibrium levels of activation, which will be metastable in nature. Unfortunately, with such conditions deactivation back to equilibrium levels will occur if an excessive thermal budget exists in the back-end of the process. Deactivation studies are beginning to emerge [105]; however, considering the importance and relevance of this topic, further work is needed in this area to understand the limitations of these techniques.

Finally, another annealing technique that is emerging is microwave annealing [106]. This has been applied to Si successfully, and also there has been a report for Ge [107]. Activation levels of 10^{19} cm^{-3} were shown for P implants into Ge substrates; hopefully this exciting technique can be optimised to beat that benchmark.

5.2. Contact optimisation

High contact resistance on n-type Ge is mainly attributed to Fermi-level pinning (FLP) close to the valence band [108,109], and subsequently to a large electron Schottky barrier height. Contact to p-type Ge is less of a challenge, as ohmic contacts can be formed more readily. Three of the most common n-type Ge contact solutions include:

- ultrathin amorphous insulating layers to terminate the free dangling bonds and eliminate FLP,
- surface passivation to bond other impurity species to the dangling Ge bonds at the surface, and
- optimisation of a metal-semiconductor alloy, such as NiGe, in combination with high active doping concentrations underneath to create stable low-resistive contacts.

Theoretical studies have shown that a thin insulating tunnel barrier can depin the Ge surface with optimum thicknesses of approximately 1 nm [110]. Selenium segregation was recently used to reduce the effective electron Schottky barrier heights for NiGe/n-Ge contacts [111], while CF_4 plasma treatment of the Ge surface was experimentally demonstrated to alleviate FLP [112]. Gallacher et al. extracted ρ_c of 2.3 × $10^{-7}\Omega$ cm^2 on n-type Ge that was doped during epitaxial growth [113]. The optimum NiGe formation temperature was a 340 °C RTA. However, the NiGe interface with the underlying substrate was not smooth.

LTA is of great interest in semiconductor processing as it enables ultrafast annealing with very limited thermal budgets. It can suppress dopant diffusion and generates high levels of dopant activation. Specifically in Ge, Mazzocchi et al. reported high activation levels of B and P dopants ($>1 \times 10^{20}$ cm^{-3}) as well as limited diffusion when they used LTA with energy densities in the range of 0.57–1.8 J/cm^2 [87]. Furthermore, Firrincieli et al. reported ρ_c of 8 × $10^{-7}\Omega$ cm^2 on n-type Ge where LTA was used for dopant activation, in combination with RTA for NiGe formation [114].

Finally, Shayesteh et al. used laser thermal annealing in the formation of the NiGe itself, on n-doped Ge [97], and compared it to results generated by conventional RTA. LTA can produce a uniform contact with a remarkably smooth substrate interface, with specific contact resistivity 2–3 orders of magnitude lower than the equivalent RTA case. ρ_c of 2.84 × $10^{-7}\Omega$ cm^2 was achieved for optimised LTA energy density conditions.

6. Modelling and projections

It is estimated by ITRS semiconductor industry experts that both development time and cost for FET technology utilising Ge-based channels can be reduced by as much as 40% from modelling activities, making it a key enabling methodology. Despite much innovative experimental work, modelling capabilities are underdeveloped for Ge, particularly in commercially available process and device simulation tools. Properly formulated physics-based models would give substantial input for time- and cost-effective development of Ge devices.

Zographos and Erlebach reviewed process simulation [115] for Ge focussing on point defects and extended defects; B, P, and As diffusion, activation, and dose loss; and C co-implantation and co-diffusion. From their perspective at Synopsys, more efforts are needed to improve the existing models and to develop currently missing models for N and F co-implantation, strain effects, and alloys such as SiGe with high Ge fraction and GeSn.

Even though the modelling landscape is less developed than the Si equivalent, a number of interesting simulation-based studies have been published. From a process modelling point of view, Koffel et al. demonstrated process modelling of P, As, and Sb profiles in Ge [116]. Tsouroutas et al. modelled P diffusion and activation and compared that to experiments using laser anneal or furnace anneal [117].

Device simulation studies have been undertaken for a variety of devices including GeOI MOSFETs [118], double-gate PMOSFETs [119], and GeOI Tunnel-FETs [120]. Finally, Hellings et al. discussed Ge device simulation model parameters for carrier generation/recombination, mobility, and interface traps [121]. They calibrated models to measurements, which they used to make device predictions.

7. Conclusions

As stated at the beginning of this paper, Si is facing competition from other semiconductor materials that may one day replace it in the channel of the FET device. With the billions of handheld portable electronic devices globally, scaling power consumption can directly reduce the global demand for energy. Power consumption control for handheld devices and other mobile information communication technology systems is the fastest, cheapest, and cleanest way to address energy usage issues. Microprocessors today are based on Si, but as technology evolves, higher carrier mobility materials will be needed to replace it. In simple terms, higher electron and hole mobilities could lead to performance gain or power saving in digital applications. High carrier mobility materials can enable increased integrated circuit functionality or reduced power consumption by delivering a fixed drive current and circuit speed at a reduced power supply voltage, therefore enabling standby and dynamic power reduction. Considering how large the handheld portable consumer electronics market has become, the impact could be very wide-reaching. Most major semiconductor manufacturing companies and, moreover, the top semiconductor sales leaders in the high-end microprocessor market take high carrier mobility materials very seriously. A scan of high-profile device conferences or electron device literature can yield high-mobility material studies from major semiconductor manufacturers [122–124].

Ge is a prime high-mobility channel material candidate. The major challenges for integration can be grouped under the heading of substrates and integration, gate dielectrics, and access resistance. At this moment in time the Ge FET device landscape comprises thin-body substrates or structures that are epitaxially grown or bonded onto Si handle wafers, high-k on GeO_2 interfacial layers for gate dielectric, and implanted dopants source/drains in combination with advanced annealing techniques, followed by optimised contact layers. In terms of devices, Ge thin-bodies have been scaled down to 20 nm thick, and the signs are encouraging. At this point in time it is difficult to directly compare Si and Ge FET performance purely because Si FETs are more scaled than the present state-of-the-art Ge FET devices. Almost all dimensions in Ge FETs are a technology

or two older than the best Si devices, so the comparison is hardly fair. However, there is a lot of exciting work on this material currently ongoing, and these authors continue to watch the developments with great interest.

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