TÜBİTAK

Turkish Journal of Physics

http://journals.tubitak.gov.tr/physics/

Invited Review Article

Turk J Phys
(2014) 38: 375 – 390
© TÜBİTAK
doi:10.3906/fiz-1404-20

Self-assembled nanocrystalline ZnO thin film transistor performance optimization for high speed applications

Burhan BAYRAKTAROĞLU*, Kevin LEEDY
Air Force Research Laboratory, Sensors Directorate, AFRL/RYDD Wright Patterson AFB, Ohio, USA

Received: 25.04.2014 • **Accepted:** 29.06.2014 • **Published Online:** 10.11.2014 • **Printed:** 28.11.2014

Abstract: ZnO nanocrystals grown at relatively low temperatures using various vacuum deposition techniques can yield semiconducting thin films of self-assembled nanocolumns 20–50 nm in diameter. Such films are suitable for the fabrication of high speed and transparent thin film transistors (TFTs). Unlike amorphous TFTs, the performance of ZnO transistors depends both on the crystal quality of nanocrystals and the electrical properties of boundary layers between them. We investigated the use of radio frequency sputtering, atomic layer deposition, and pulsed laser deposition techniques to fabricate self-assembled nanocrystalline thin films and determined the influence of deposition conditions on the performance of transistors. Device design and fabrication parameters were also optimized to demonstrate TFTs with high current density and high speed performance comparable to single crystalline-based transistors.

Key words: Self-assembly, thin film transistors, nanocrystalline, nanocolumns, ZnO, atomic layer deposition, pulsed layer deposition

1. Introduction

Thin film electronics is a highly specialized segment of electronics technology providing solutions for mostly disposable, flexible, or large area products. Some of the distinguishing features of this branch of electronics are the low cost and low temperature manufacturing requirements for all components and their integration on a variety of substrates. The product market for this technology has not been highly visible in the past, but with the introduction of flat panel displays for computers, flat panel television monitors, and the touch screen displays of modern cellular telephones, the product market has sharply increased over the last 10 years. Pixel control of modern TV displays, for example, requires the use of millions of transistors fabricated over an area that is measured in square meters. An even larger product manufacturing base exists if radio frequency identification, thin film solar cell [1], and medical applications are also considered.

As is the case with conventional electronics, transistors lie at the core of thin film electronics. Thin film transistors (TFTs) are some of the earliest solid state electronic components to be developed [2,3], but their evolution did not keep up with transistors fabricated on single crystal substrates. In the past, TFT performance requirements were low, since they were mostly used in disposable, low cost products. These requirements could be addressed with the use of amorphous silicon (a-Si) or organic semiconductors [4]. Compared to single crystal counterparts, these semiconductors provide much lower switching speeds or amplification gains. Polycrystalline Si (poly-Si) [5] has been used in some cases to increase speed at the expense of higher temperature processing.

*Correspondence: burhan.bayraktaroglu@us.af.mil

The control of grain boundary charges is also a concern as it impacts the threshold voltage uniformity [6–9] and hot-carrier induced degradation [10].

Recently, advanced amorphous TFTs became possible with the use of transition metal oxide semiconductors. These types of devices can provide higher electron mobility, low temperature processing, and optical transparency [11,12]. Comprehensive reviews of the status of amorphous transparent TFTs were recently provided [13–15]. ZnO, as a simple binary compound, offers many attractive electronic properties [16]. It has relatively high electron mobility and velocity [17–20] and exhibits strong field induced charge accumulation at its surface [21]. The bonding in ZnO and similar oxide semiconductors is strongly ionic and the states near the conduction band minimum arise almost completely from cation (zinc) s-orbitals. This is in strong contrast to covalent or near covalent semiconductors such as Si and GaAs, where *sp*-bonding is sensitive to both bond angle and bond length disorder that easily generates localized states (traps). In oxide semiconductors, the nearly spherical and relatively large empty zinc cation orbitals that form the conduction band result in electron transport that is largely unaffected by bond angle or bond length disorder and disorder does not result in localized states [22]. It is therefore expected that the amorphous thin film electronic properties can be quite similar to their single crystal counterparts and this has been shown to be true at least for moderately doped ZnO:Ga,In films [23]. Thin films of ZnO are regarded to be polycrystalline rather than amorphous. However, the crystal sizes are extremely small (20–50 nm) and they can spontaneously self-assemble to provide uniform thin films [24–26].

Although most ZnO thin films prepared in vacuum deposition systems exhibit similarly arranged nanocolumnar structures, the performance characteristics of TFTs made from these films can be drastically different. In addition to the quality of crystals within nanocolumns, we must consider the effect of grain boundaries between them. Columns of nanocrystalline ZnO (nc-ZnO) form closely packed arrangements in self-aligned nc-ZnO thin films so that boundaries between nanocolumns are parallel to each other and perpendicular to the growth surface. The electrical current from source to drain flows across these boundaries in the channel. Therefore, the transistor performance can be influenced by the potential barriers that may exist at such interfaces.

In this study, we have investigated the impact of thin film properties on transistor performance by preparing films of equal thickness and correlating the electrical performance to film deposition and postdeposition annealing parameters. Film deposition techniques included RF (radio frequency) sputtering, pulsed laser deposition (PLD), and atomic layer deposition (ALD) across growth temperature ranges from room temperature to 400 °C. Some wafers were annealed in air after deposition at temperatures up to 600 °C. Films were analyzed using X-ray diffraction, ellipsometry, atomic force microscope (AFM), scanning electron microscope (SEM), and transmission electron microscope (TEM). Transistors were fabricated using various gate insulators and gate lengths and electrical performance was determined up to microwave frequencies.

2. Thin film deposition and characterization

2.1. Thin film deposition

PLD nc-ZnO films were deposited in a Neocera Pioneer 180 pulsed laser deposition system with a base pressure of 2.67×10^{-5} Pa. A KrF excimer laser (Lambda Physik COMPex Pro 110, 248 nm wavelength, 10 ns pulse duration) operated at 30 Hz with an energy density of 2.6 J/cm^2 at the target. ZnO films were deposited on 7.62 cm diameter substrates with a deposition temperature of 25 °C to 400 °C, oxygen partial pressure of 1–100 mTorr, and substrate-to-target distance of 9.5 cm. The target was a 50 mm diameter, 6 mm thick

sintered 99.999% pure ZnO ceramic disk. The target and substrate were rotated and the focused beam was scanned across the target during deposition.

Sputtered ZnO thin films were prepared using a Denton Vacuum Discovery RF confocal configured magnetron sputtering system with a base vacuum of 2×10^{-5} Pa and using a 99.999% pure ZnO target. A mass flow regulated Ar sputtering pressure of 4 mTorr and 100 W forward power was held constant, resulting in a nominal deposition rate of 0.1 nm/s. A 150 mm diameter water cooled substrate holder was used without external heating for all of the depositions.

ALD ZnO films were prepared in a Cambridge Nanotech Fiji F200 ALD system at 250 °C. ZnO depositions used diethylzinc and water as the zinc and oxygen source, respectively, yielding a growth rate of 1 Å/cycle. Argon was used as a precursor carrier gas and purge gas.

Various gate insulators, including SiO_2, Al_2O_3, and HfO_2, were used in this study. SiO_2 films were grown in a PlasmaTherm 790 plasma-enhanced chemical vapor deposition (PECVD) system at 250 °C. A N_2O/silane ratio of 5.6/1 at 120 Pa yielded a deposition rate of 46 nm/min. Al_2O_3 and HfO_2 films were prepared in a Cambridge Nanotech Fiji F200 ALD system at 250 °C. Al_2O_3 depositions used trimethylaluminum and water as the aluminum and oxygen source, respectively, yielding a growth rate of 0.9 Å/cycle. The HfO_2 depositions used tetrakis(dimethylamido)hafnium(IV) as the hafnium source and a remote radio frequency 300 W O_2 plasma as the oxygen source, yielding a growth rate of 1 Å/cycle. Argon was used as a precursor carrier gas and plasma purge gas.

Since PLD-grown nc-ZnO thin films have shown the most promise in achieving higher performance TFTs, we have focused on the influence of PLD film deposition and postdeposition processing conditions on the transistor performance. There are many growth parameters that influence the film properties. These include substrate temperature, ambient pressure and gas, laser energy density, pulse frequency, laser scan speed, and target-to-substrate distance. Some of these parameters that primarily influence the growth rate and film uniformity were first optimized to achieve uniform and reproducible films. These parameters were mostly related to laser beam density and scanning and they were fixed at the parameter values described above. Typical film thickness uniformity is shown in Figure 1. The growth parameters that influenced the electrical properties were growth temperature and gas pressure. The most influential postgrowth process parameter was the annealing temperature. Films were subjected to annealing in ceramic ovens up to 600 °C in a filtered clean room air.

2.2. Thin film characterization

The ZnO crystal structure was determined with 2Θ-ω scans using a PANalytical X'Pert Pro MRD X-ray diffractometer. Film morphologies were analyzed with an FEI DB235 SEM and a JEOL 4000EX TEM operating at 400 kV. Surface roughness was measured with a Veeco Dimension 3000 AFM. Film thickness and refractive index were measured with a Horiba Jobin Yvon UVISEL spectroscopic ellipsometer.

3. Transistor fabrication

Devices for low frequency characterization were fabricated on p-type Si wafers. The gate lengths, L_G, varied from 2 to 25 μm. High speed devices were fabricated on high resistivity Si substrates (>2000 ohm cm) to minimize capacitive parasitics of the substrate. Gate lengths for these devices varied from 1.2 μm to 3 μm. A bottom-gate configuration was used for all transistors, where the gate contact was fabricated first directly on the substrate. As shown in Figure 2, the gate contact was covered with the gate insulator and 50 nm thick nc-ZnO films were produced conformably over the gate insulator. The gate contact consisted of evaporated Ni/Au

films with 5 nm and 150 nm thicknesses, respectively. Au was preferred for a gate contact because of its high conductivity and featureless surface morphology. Nonalloyed ohmic contacts were fabricated on nc-ZnO films using lift-off techniques and evaporated Ti/Au metal films (20 nm/350 nm). ZnO layers outside the device area were removed using wet chemical etching in diluted HCl (1% by volume) at room temperature while protecting

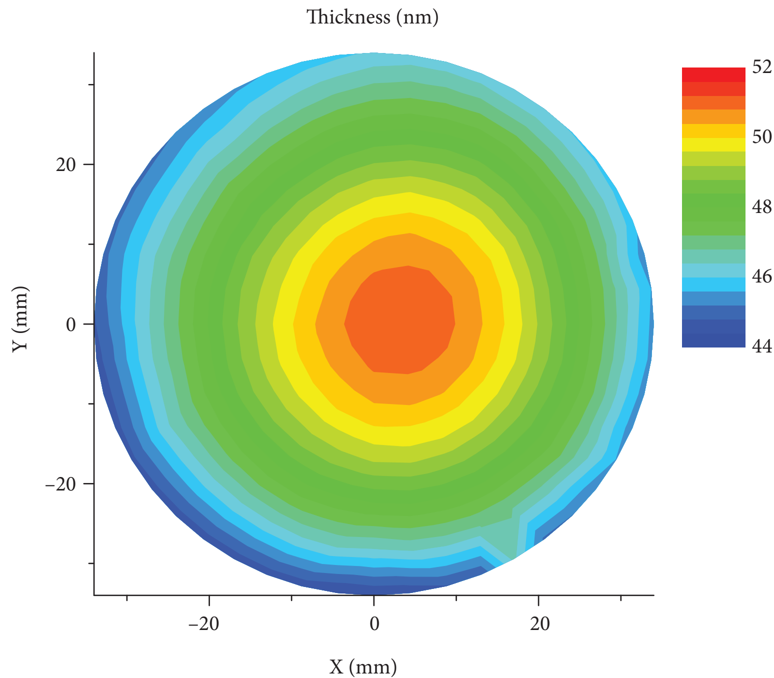

Figure 1. PLD ZnO thickness uniformity on 7.62 cm diameter substrate measured by 169 point ellipsometry map. Average thickness is 47.5 nm with 1.9 nm 1σ.

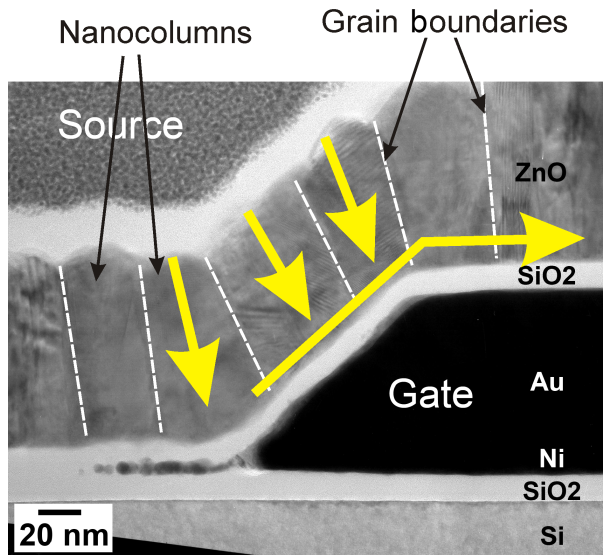

Figure 2. Schematic drawing imposed on TEM image of the transistor section between the source and gate contacts showing the self-aligned ZnO nanocolumns and the expected current flow path.

the active device area with a layer of photoresist. The ZnO etch rate was 5 nm/s. The source and drain contacts overlap the gate contact by 0.5–1.0 μm. The gate length is defined as the distance between the source and drain contacts. No intentional surface passivation was applied to the free surface of the nc- ZnO film.

As shown in Figure 2, ZnO nanocolumns self-assemble over the gate metal in such a way that the columns and the grain boundaries are always perpendicular to the growth surface. The electron current flows from the source contact into nanocolumns toward the gate insulator interface. When the gate bias is higher than the threshold voltage, band bending at the interface allows the formation of a conductive channel. Potential barriers at grain boundaries are also lowered by the gate potential [27–30] and the current flow proceeds perpendicular to nanocolumns toward the drain contact.

4. Thin film analysis

Cross-sectional TEM images of nc-ZnO films indicate that the ZnO is composed of densely packed, columnar-shaped grains extending through the thickness of the film, as shown in Figures 3a–3d. The nanocolumnar grain diameters were between 20 and 50 nm. As will be discussed below, the grain size depended on film growth parameters such as substrate temperature and postdeposition annealing. However, all films exhibited self-assembly of nanocolumns and this feature was also found to be independent of the surface on which the films were grown (i.e. surface agnostic growth). PLD films grown on Al_2O_3 and HfO_2 gate insulators, shown in Figures 3c and 3d, shared similar morphologies with slightly larger grains on HfO_2. While PLD ZnO films were uniformly dense, sputtered ZnO films (Figure 3b) displayed a bimodal growth with a 10 nm partially voided nucleation layer followed by fully dense ZnO. Although lower mobility of adsorbing ZnO due to room temperature deposition might be attributed to the voided layer, no such voiding was observed in PLD grown films at room temperature.

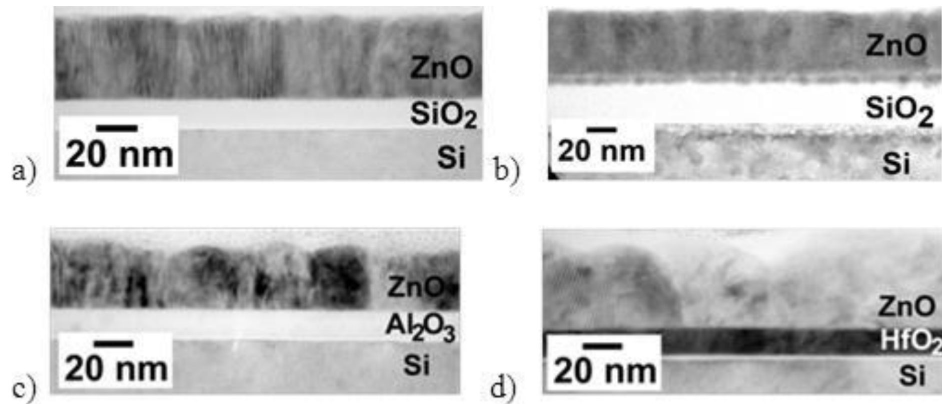

Figure 3. Cross-sectional TEM image of a) PLD ZnO on SiO_2/Si, b) sputtered ZnO on SiO_2/Si, c) PLD ZnO on Al_2O_3/Si, and d) PLD ZnO on HfO_2/Si.

X-ray diffraction scans of ZnO films deposited on SiO_2, Al_2O_3, and HfO_2 gate dielectrics exhibited the typical hexagonal wurtzite structure with a preferred (002) orientation, consistent with other studies of PLD ZnO films [31–34]. PLD and sputtered ZnO scans in Figure 4 show higher quality crystals of PLD films, as indicated by peak width and height. Full width at half maximum (FWHM) values for as-deposited PLD films were 0.38°, compared to 1.25° for sputtered ZnO. PLD ZnO films also showed minor components of (100) and (101) lattice planes. For the optimized PLD ZnO at 200 °C, the as-deposited 2Θ (002) position was 34.416°,

compared to 34.421° from the JCPDS #36-1451 powder diffraction file. The sputtered ZnO (002) peak was at 34.25°, indicating a strained lattice.

4.1. Influence of growth temperature

At deposition temperatures of <75 °C, grains exhibited a more disordered arrangement, as shown in Figure 5. In films deposited from 100 °C to 400 °C, more columnar grain structure and consistent diffraction contrast was observed with increasing temperature. Also with increasing deposition temperature up to 400 °C, the intensities of the ZnO (002) peak increased and FWHM values of the ZnO (002) peak decreased, indicating improved film crystallinity. Progressively higher ZnO (002) peak intensities were obtained from ZnO films deposited on HfO_2, SiO_2, and Al_2O_3, respectively. Further details on XRD results are given elsewhere [35].

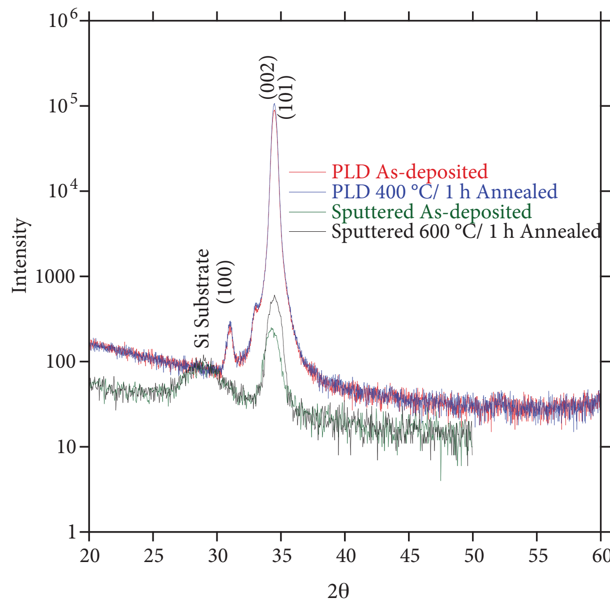

Figure 4. X-ray diffraction patterns of PLD ZnO thin films deposited at 200 °C and after 400 °C/1 h air annealing and sputtered ZnO films deposited at 25 °C and after 600 °C/1 h air annealing.

Calculated ZnO grain sizes from AFM images were 25 to 27 nm for 100 °C, 200 °C, and 300 °C as-deposited films shown in Figures 6a–6d. Films deposited at 400 °C had 31 nm grains. The RMS surface roughness of ZnO films deposited on all gate dielectrics was 0.8 nm, as measured by AFM. The RMS roughness is similar to other reported values of ZnO deposited by PLD [36,37]. Sputtered ZnO had an as-deposited RMS roughness of 1.25 nm. The measured surface roughness of the underlying dielectric material was approximately 0.2 nm regardless of film composition, deposition technique, or deposition temperature. This smooth surface was necessary for ordered ZnO grain growth and produced a well-defined dielectric-ZnO interface, which was essential for device performance.

4.2. Postgrowth annealing

All films displayed grain growth and crystal refinement upon postdeposition annealing in ambient air. However, RMS roughness also increased: 0.8 nm to 2.9 nm for PLD ZnO and 1.25 nm to 2.0 nm for sputtered ZnO. Increased roughness occurred as the coalesced grains developed more pronounced domed surfaces and clearly

defined triple points. The FWHM of (002) showed no appreciable change for PLD ZnO and decreased to 1.05° for sputtered ZnO. The rocking curve FWHM of (002) PLD ZnO decreased from 2.869° to 2.764°. As evidenced in Figures 6e–6h, ZnO grain sizes after a 1 h 600 °C anneal increased to an average of 56 nm for all films. Numerous studies have observed improved physical vapor deposited ZnO film properties with postdeposition annealing, including enlarged grain sizes, narrower FWHM values, and reduced strain [38–40].

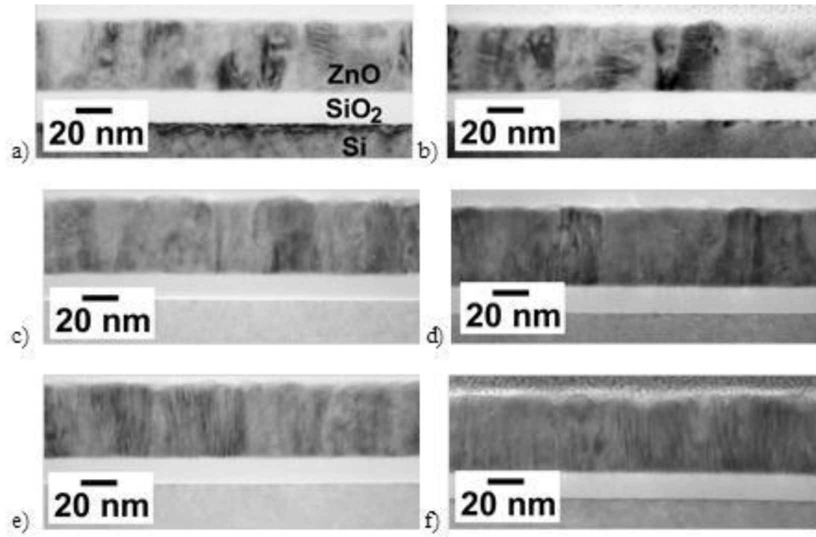

Figure 5. Cross-sectional TEM images of PLD ZnO thin films deposited on 20 nm SiO_2/Si at a) 25 °C, b) 75 °C, c) 100 °C, d) 200 °C, e) 300 °C, and f) 400 °C.

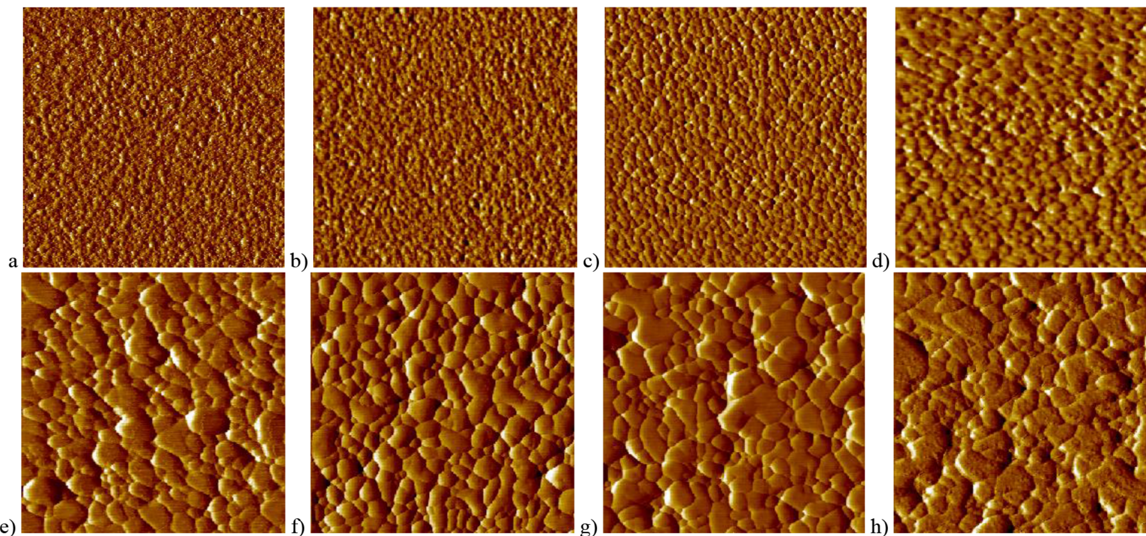

Figure 6. AFM of PLD ZnO deposited at a) 100 °C, b) 200 °C, c) 300 °C, and d) 400 °C and the same films after 600 °C/1 h air annealing in e), f), g), and h). Images are 1 μm × 1 μm.

5. Thin film transistors

The nc-ZnO TFT characteristics depend strongly on the quality and the structure of nanocrystals that make up the active device region. As shown schematically in Figure 2, the electron current flows from source to drain

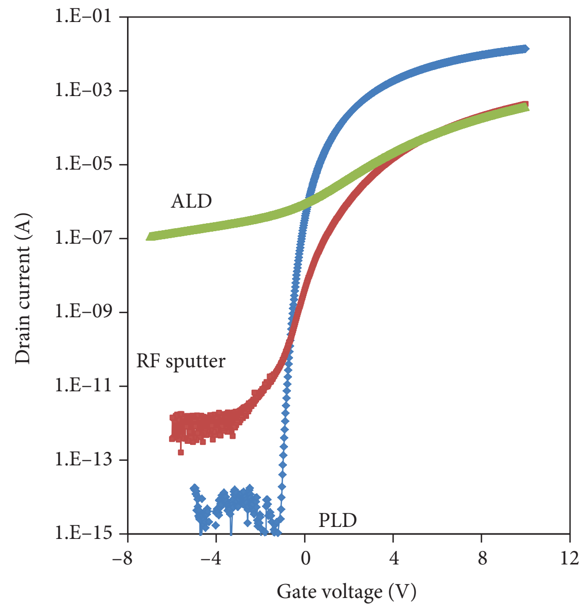

Figure 7. Transfer characteristics of nc-ZnO TFTs prepared by PLD-, ALD-, and sputter-deposited films.

in the conductive channel induced by the gate voltage. The current behavior can be described effectively using fully depleted SOI transistor models [41] because of strong similarities. In the absence of grain boundaries, drain current is influenced by the interface state density, the electron mobility, and the impurity levels in the crystal. For nc-ZnO TFTs, the additional influence of the potential barriers at the grain boundaries must be included [27–30]. The drain current is therefore a sensitive device parameter that can be used to assess the quality of nc-ZnO thin films. A significant increase in this parameter value for a set gate voltage requires the reduction of the effects of grain boundaries, improvements in nanocrystalline ZnO electrical properties (mobility, defects, doping, etc.), as well as a reduction of interface state density.

The transfer characteristics of nc-ZnO TFTs fabricated using 3 different growth methods are shown in Figure 7. Identical device processing conditions were applied to all devices, including postgrowth annealing at 400 °C in air for 1 h. All devices showed normally-off mode of operation with positive threshold voltages (V_{th}). In all other respects, devices were significantly different from each other. The current on/off ratios were 5×10^{12}, 5×10^{8}, and 4×10^{3} for PLD-, sputter-, and ALD-grown ZnO, respectively. The major factor contributing to such a wide difference in the current on/off ratios was the residual conductivity of the ALD and sputtered films. The source of background conductivity can be oxygen deficiency or unintentional doping by impurities in the chamber. The other contributing factor is the on-current level, which was more than an order of magnitude higher for PLD films than the others. The cause of higher on-current can be the quality of nanocrystals, reduction in grain boundary charge, or lower interface state density for PLD-grown films. Low interface state density of PLD films can also be inferred from the low subthreshold voltage swing value of 74 mV/decade, which corresponds to a total interface charge density of 2.51×10^{11} cm^{-2} using the expression developed by Roland et al. [42]. Sputtered and ALD films produced approximately 15× and 35× higher interface charge densities, respectively.

One of the distinguishing features of nc-ZnO TFTs (compared to amorphous or single crystal FETs) is the extended turn-on region of the transfer characteristics. This can be seen as a “soft shoulder” region between the exponential and the square-law regions of the transfer characteristics of all 3 TFTs in Figure 7.

Modeling studies of both poly-Si and nc-ZnO have shown that grain boundary charges are primarily responsible for the increased threshold voltage and the extended turn-on region [6–9,28,30]. This effect can be also observed in transconductance efficiency (g_m/I_D) versus I_D characteristics, where g_m is the transconductance and I_D is the drain current. Transconductance efficiency is a measure of how efficiently current is converted into transconductance and is often used in the analysis of analog devices operating near threshold voltage regions [43,44]. As shown in Figure 8a, PLD TFTs produce flat and near ideal transconductance efficiency at low drain current values where I_D increases exponentially with gate voltage below V_{th}. Near ideal transconductance efficiency is mostly due to a low interface state density. At high drain current values, the slope of the line is roughly –1/2. Between the exponential (below V_{th}) and the high current (much above V_{th}) regimes, in the current range of about 10^{-6} to 10^{-3} A, the line slope is approximately –1/4. This region, which corresponds to "weak accumulation" conditions, is usually much smaller in single crystal Si MOSFETs [44]. Compared to PLD TFTs, sputter and ALD TFTs have much lower g_m efficiency and even wider weak accumulation regions. This can be explained by the presence of much higher interface and grain boundary charges in these types of films. The nanocrystalline quality can be assessed by the field effect (FE) mobility extracted from the transfer characteristics. The mobility values extracted at $V_D = 0.1$ V are shown in Figure 8b. It is clear that the FE mobility is significantly higher with PLD films than the others. Although higher mobility values have been reported with sputtered films [45,46], in our experiments, PLD films consistently produced significantly higher mobility values consistent with prior published data [47,48].

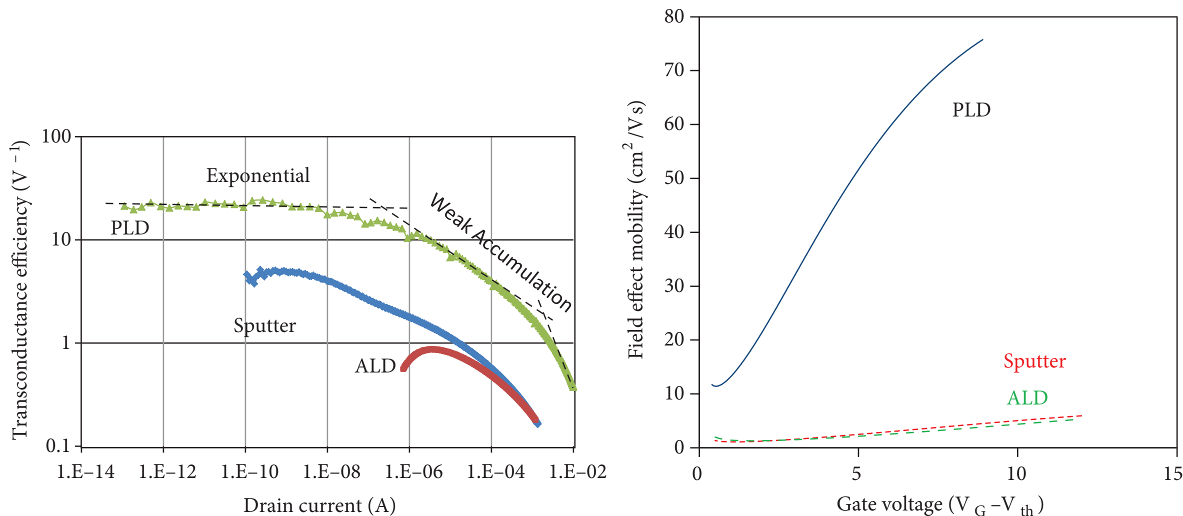

Figure 8. a) Transconductance efficiency dependence on drain current, b) field effect mobility of TFTs with nc-ZnO films deposited by PLD, ALD, and sputtering.

5.1. Performance optimization

We have undertaken several transistor optimization studies, concentrating mostly on improving the quality of thin films. These studies included the growth of films at different temperatures and different pressures, as well as postdeposition annealing. Figure 9 shows the influence of postgrowth annealing temperature on the transistor on-current (also known as current density) values as a function of gate lengths for all 3 types of films. The current density dependence on gate length was almost identical for all as-grown films, but the actual values varied significantly between the film types. ALD films had the lowest current density values. As-grown PLD films have shown 18× and 45× higher current densities than as-grown sputter and ALD film,

respectively. Postgrowth annealing in air increased the current density by a factor of 2 for each 100 °C increase in annealing temperature for sputtered films. ALD films showed more significant improvement ($8.8\times$) at the 350 °C annealing temperature, but the rate of improvement was less at higher temperatures. No improvement was observed between 500 °C and 600 °C for ALD films. The current density also increased with annealing for PLD films, but the rate of increase was much less compared to other films. As discussed above, the postgrowth annealing has a significant impact on grain boundaries by reducing their density. In the case of ALD and sputtered films, annealing can also reduce oxygen deficiency of as-grown films and improve crystal quality. Postgrowth annealing has a similar effect on nc-ZnO films as laser annealing has on poly-Si thin films [49–51]. The highest current density obtained was 800 mA/mm for 2 μm gate length PLD ZnO devices. Assuming that the current density dependence on gate length holds for even shorter gate lengths, we can expect higher than 1 A/mm current density for 1 μm gate length devices.

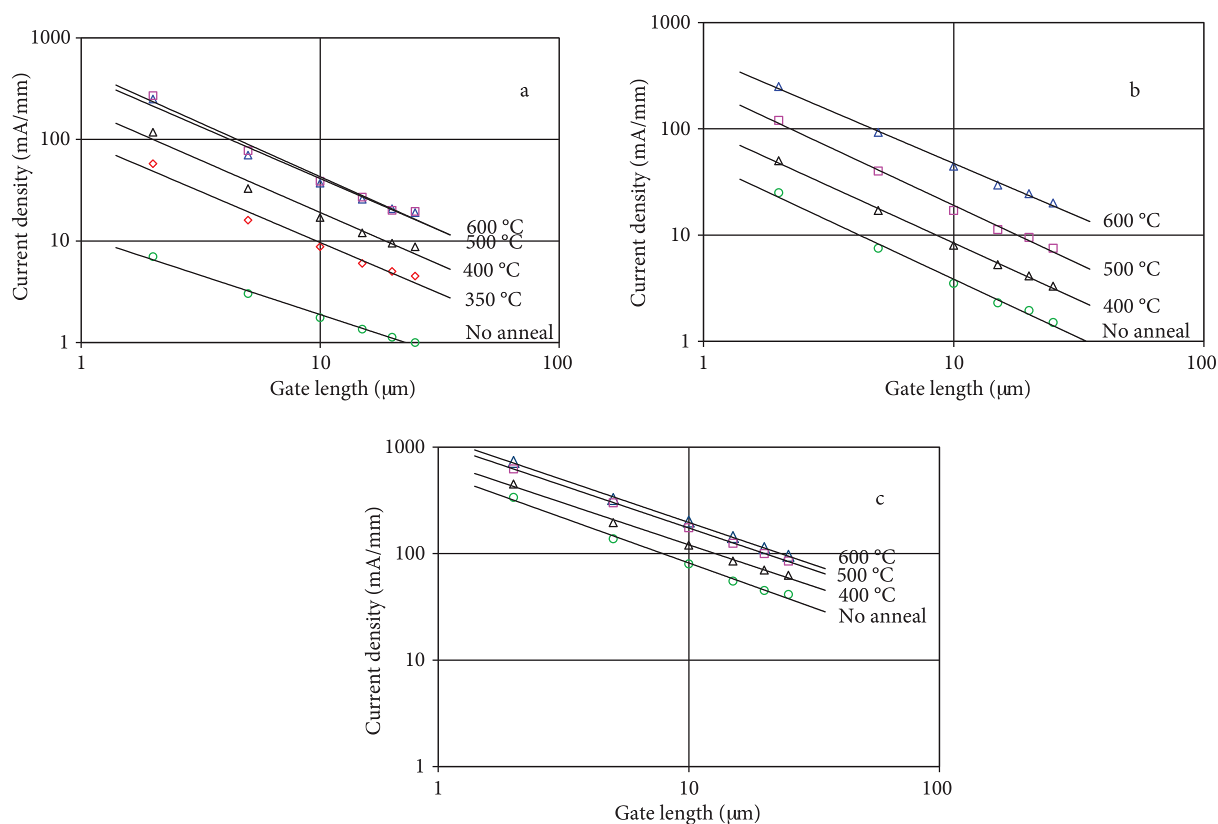

Figure 9. Drain current density dependence on gate length for devices fabricated using a) ALD, b) sputter, and c) PLD deposition techniques.

Since PLD-grown films produced significantly better films, further optimization efforts were concentrated on these films. Figure 10 shows the influence of substrate temperature during film growth on the device transfer characteristics and the drain current density. The growth temperature had only minimal influence on the interface state density, as indicated by almost identical subthreshold voltage swing characteristics. The impact on grain boundary charge density is also minimal, as indicated by almost constant threshold voltage change (as shown in the inset of Figure 10a). The on/off ratio values, however, had nonlinear growth temperature dependence. Since the off-state current values were almost identical, the on/off ratio variations were mostly due to on-state current values. This was further studied by testing the current density as a function of growth

temperature for various gate length devices. As shown in Figure 10b, the current density increases with growth temperature up to 200 °C and then decreases slightly. Based on the above observations, we postulate that the main influence of the growth temperature is on the nanocrystal quality, which reaches a maximum at 200 °C growth conditions.

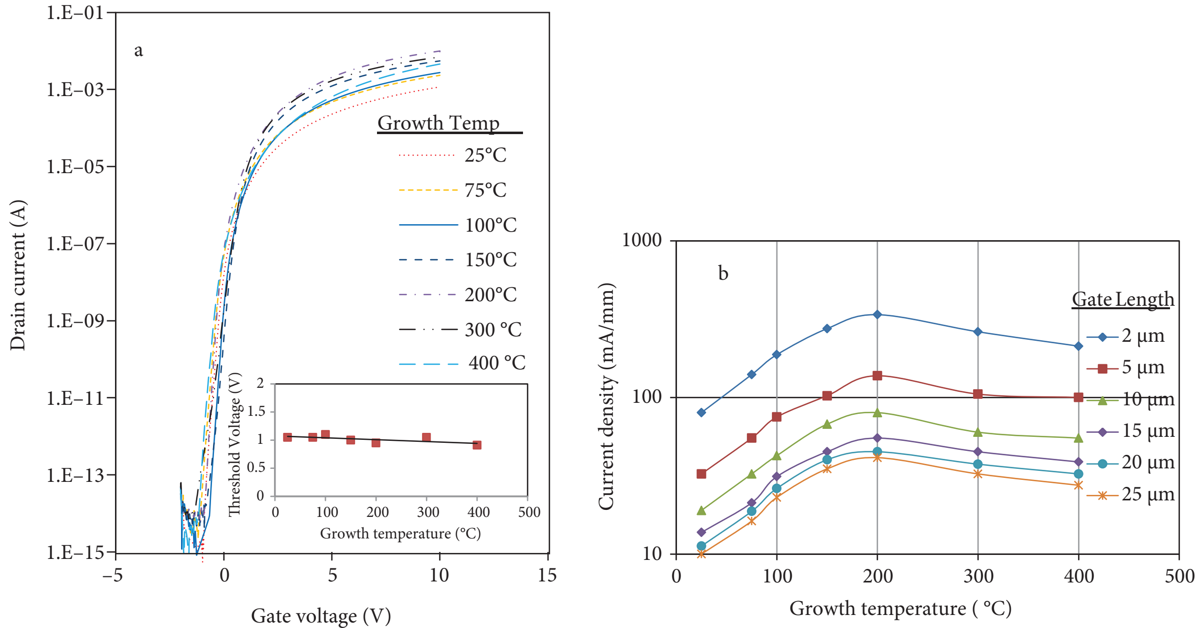

Figure 10. The effect of growth temperature on the a) transfer characteristics and b) drain current density of PLD nc-ZnO TFTs. The transistor size was $W_D = 400$ μm for all tests and $L_G = 5$ μm for a).

The effect of oxygen pressure during growth on current density is shown in Figure 11. The current density is maintained at its highest level at a low pressure level up to 10 mTorr. At higher pressures, the current density decreases logarithmically. We interpret the decrease to be due to the increased oxygen related trap density at grain boundaries. This is consistent with the results obtained with doped nc-ZnO thin films, which showed lower grain boundary potential barriers due to a reduction of metal vacancies for films grown at lower or no oxygen atmospheres [52,53].

Typical common-source I–V characteristics of nc-ZnO TFTs fabricated on SiO_2, HfO_2, and Al_2O_3 gate insulators are shown in Figure 12. The ZnO films were grown at 200 °C and devices were fabricated in the same fabrication batch for direct comparison of results. All devices showed hysteresis-free operation and positive threshold voltages of 1.5 ± 0.6 V. As expected, higher dielectric constants of Al_2O_3 and HfO_2 compared to SiO_2 resulted in higher drain currents for the same gate voltage (i.e. higher transconductance) and flatter current characteristics in the saturation region. The influence of the gate insulator on device transconductance is shown in Figure 13. The same reciprocal dependence of transconductance on gate length was obtained for these insulators in the gate length range of $L_G = 2$–25 μm. This indicates that the number of charge states at the insulator–ZnO interface is low and such charges do not heavily influence the device operation and provide a wider range of gate insulator options for transistor performance optimization.

5.2. High speed transistors

Thin film transistors are mostly used in circuits that do not require high speed operation [4] because of electron mobility limitations. However, with the demonstrated high electron mobility and the anticipated high electron

velocity [19], ZnO-based TFTs have a greater potential for high speed circuit applications than amorphous thin film transistors. Recently, devices capable of small-signal amplification at microwave frequencies were demonstrated using relatively long gate lengths of 1.2–3 μm [47,54].

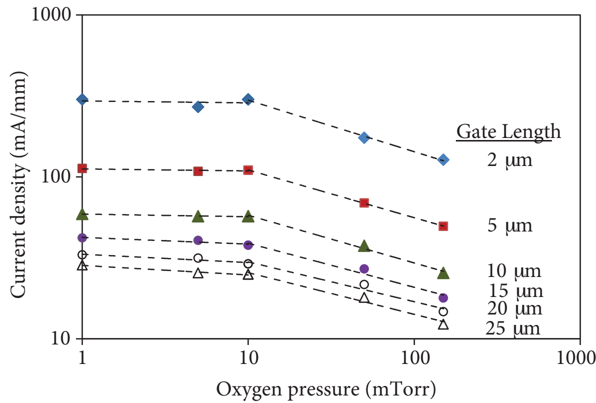

Figure 11. Drain current density dependence on oxygen pressure during deposition of PLD nc-ZnO thin films.

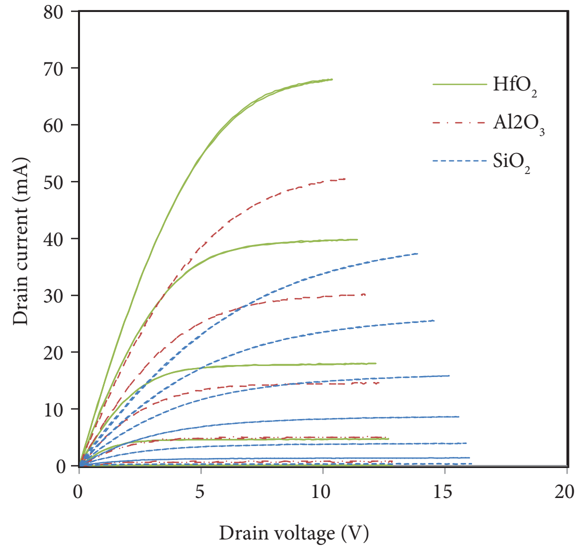

Figure 12. I-V characteristics of nc-ZnO TFTs with various gate insulators. Gate insulator thickness = 30 nm, L_G = 5 μm, W_G = 400 μm, V_G = 2 V/step.

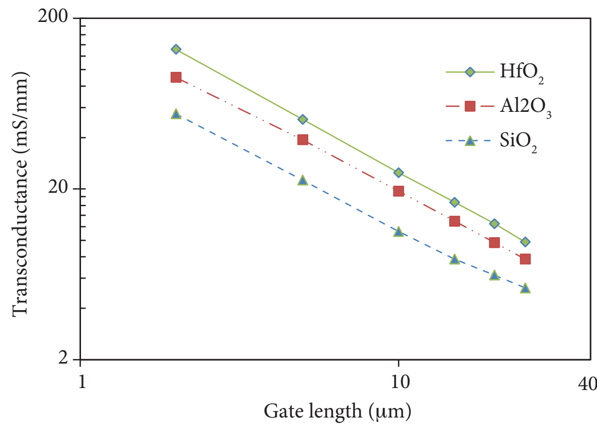

Figure 13. Transconductance dependence on gate length for 3 different gate insulators. V_D = 12 V, V_G = 10 V.

In the design of high speed transistors, several parasitic device elements must be minimized in addition to shrinking the gate length. The most prominent parasitic elements that degrade the high frequency operation of a bottom-gated TFT are the gate resistance and the capacitance between gate and source/drain contacts. The gate resistance can be lowered by the use of thick, high conductivity metals such as Au or Cu. However, as shown in the cross-sectional drawing of Figure 2, thick gate metal produces nonplanar topography for the bottom-gate transistors. It is important that the gate insulator and the ZnO thin film are produced conformably over the gate contact.

The parasitic capacitance resulting from the overlap of source/drain contacts over the gate can be reduced in several ways. The first is to minimize the overlap by careful alignment of these contacts and reduction of the

actual gate length to as close to the source-drain spacing as possible (i.e. self-aligned contacts). The second is to employ a thicker gate insulator in the regions where the contacts overlap and use thinner gate insulator under the actual channel region. This approach requires the use of gate insulators with 2 different thicknesses over the gate contact, as shown in Figure 14. Again, such an approach results in nonplanar surfaces over which the ZnO thin film is produced. However, nc-ZnO films fabricated by PLD have shown that such topological variations can be readily overcome.

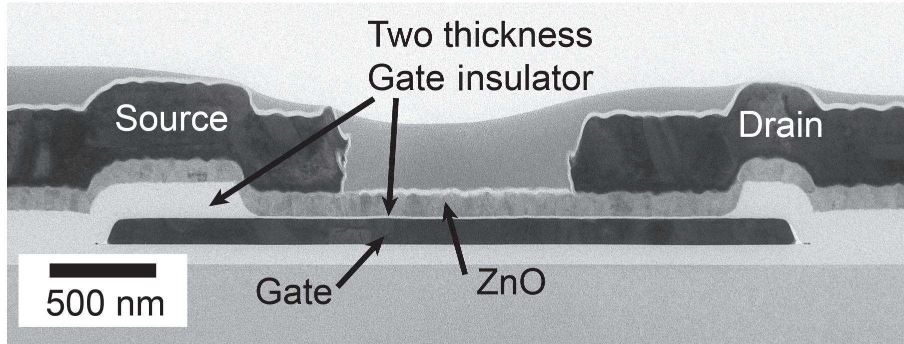

Figure 14. TEM image showing the use of thick gate insulator to reduce parasitic capacitance in high speed TFTs.

The high speed potential of nc-ZnO thin film transistors was examined in a series of designs fabricated on high resistivity Si substrates (>2000 ohm cm). The gate contact was Ni/Au (5 nm/150 nm) to ensure low gate resistance. The gate insulator was 30 nm thick PECVD SiO_2. From the measured s-parameters, the maximum available gain and current gain ($|h_{21}|^2$) values were determined as shown in Figure 15. Both gain characteristics showed –6 dB/octave slopes with cut-off frequencies f_T of 2.9 GHz and f_{max} of 10 GHz for devices with L_G = 1.2 μm and W_G = 2 × 50 μm. To our knowledge, this is the highest frequency operation obtained with any oxide thin film transistor technology. Based on small-signal device models extracted from the measured s-parameters, we expect f_{max} > 60 GHz for devices with L_G = 0.2 μm.

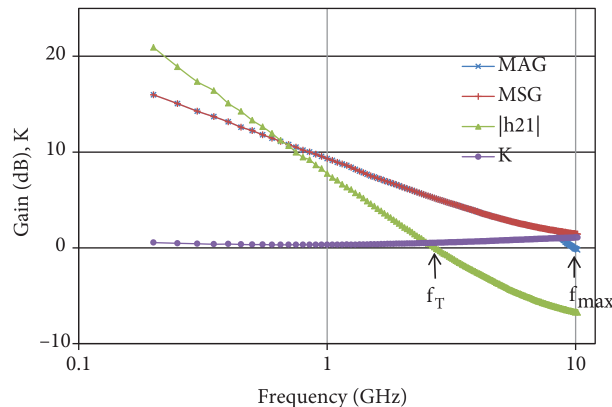

Figure 15. Small signal microwave characteristics of nc- ZnO TFT with L_G = 1.2 μm and W_G = 2 × 50 μm. Devices were biased at V_G = 6 V, V_D = 11 V.

6. Conclusions

Nanocolumns of ZnO with 20–50 nm diameters self-assemble during growth in various vacuum deposition techniques to yield closely packed thin films that are suitable for transistor fabrication. We have studied the

properties of such films grown by PLD, ALD, and RF sputtering techniques over several types of substrates. Although structurally all films had similar characteristics, the electrical performance of transistors were drastically different. The identified factors that explain some of these differences were the grain boundary charges, the nanocrystal quality and doping level, and the interface state density. It was found that postgrowth annealing in air significantly improved transistor performance by physically modifying the grain boundaries and increasing the nanocrystal sizes. A systematic study of PLD film deposition conditions were undertaken to correlate film properties to transistor performance. The optimum performance was obtained with films deposited at 200 °C substrate temperature and 10 mTorr oxygen pressure. Current density values as high as 800 mA/mm were demonstrated with 2 μm gate length devices. Finally, it was shown that optimized films can be used to fabricate very high speed transistors with cut-off frequencies as high as 10 GHz.

Acknowledgments

The authors thank J Brown and A Reed for AFM and XRD analyses, respectively.

References

[1] Poortmans, J.; Arkhipov, V. *Thin Film Solar Cells: Fabrication, Characterization and Applications*; Wiley: West Sussex, England, 2006.

[2] Lilienfield, J. E. US Patent 1900018, 1933.

[3] Heil, O. Brit. Pat. BP 439457, 1935.

[4] Kagan, C. R.; Andry, P. *Thin Film Transistors*; Marcel Dekker Publishing: New York, NY, USA, 2003.

[5] Sameshima, T. *ECS Trans.* **2010**, *33*, 183–191.

[6] Farmakis, F. V.; Brini, J.; Kamarinos, G.; Angelis, C. T.; Dimitriadis, C. A.; Miyasaka, M.; Ouisse, T. *Solid State Electron.* **2000**, *44*, 913–916.

[7] Kimura, M.; Inoue, S.; Shimoda, T.; Eguchi, T. *J. Appl. Phys.* **2001**, *89*, 596–600.

[8] Kimura, M.; Dimitriadis, C. A. *IEEE Trans. Elec. Dev.* **2011**, *58*, 1748–1751.

[9] Ho, C. H.; Panagopoulos, G.; Roy, K. *IEEE Trans. Electron Dev.* **2012**, *59*, 2396– 2402.

[10] Dimitriadis, C. A.; Kimura, M.; Miyasaka, M.; Inoue, S.; Farmakis, F. V.; Brini, J.; Kamarinos, G. *Solid State Electron.* **2000**, *44*, 2045–2051.

[11] Kamiya, T.; Nomura, K.; Hosono, H. *J. Disp. Technol.* **2009**, *5*, 273–288.

[12] Hosono, H. *Thin Solid Films* **2007,** *515*, 6000–6014.

[13] Kamiya, T.; Nomura, K.; Hosono, H. *Sci. Technol. Adv. Mater.* **2010**, *11*, 044305.

[14] Park, J. S.; Maeng, W. J.; Kim, H. S.; Park, J. S. *Thin Solid Films* **2012**, *520*, 1679–1693.

[15] Fortunato, E.; Barquinha, P.; Martins, R. *Adv. Mater.* **2012**, *24*, 2945–2986.

[16] Look, D. C. *Mater. Sci. Eng. B* **2001**, *80*, 383–387.

[17] Özgür, Ü.; Alivov, Y. I.; Liu, C.; Teke, A.; Reshchikov, M. A.; Doğan, S.; Avrutin, V.; Cho, S. J.; Morkoç, H. *J. Appl. Phys.* **2005**, *98*, 041301.

[18] Makinoa, T.; Segawa, Y. *Appl. Phys. Lett.* **2005**, *87*, 022101.

[19] Albrecht, J.; Ruden, P. P.; Limpijumnong, S.; Lambrecht, W. R.; Brennan, K. F. *J. Appl. Phys.* **1999**, *86*, 6864–6867.

[20] Janotti, A.; Van de Walle, C. G. *Rep. Prog. Phys.* **2009**, *72*, 126501.

[21] Eger, D.; Many, A.; Golstein, Y. *Phys. Lett.* **1975**, *55a*, 197–198.

[22] Hosono, H. J. *Non-Crystal. Solids* **2006**, *352*, 851–858.

[23] Nomura, K.; Ohta, H.; Takagi, A.; Kamiya, T.; Hirano, M.; Hosono, H. *Nature* **2004**, *32*, 488–492.

[24] Bayraktaroglu, B.; Leedy, K. In *Conference Proceedings: 11th IEEE International Conference on Nanotechnology*, Portland, OR, USA, 15–18 August 2011; Morris, J. E., Ed.; Institute of Electrical and Electronics Engineers: New York, NY, USA, pp. 1450–1455.

[25] Lee, J. H.; Ahn, C. H.; Hwang, S.; Woo, C. H.; Park, J. S.; Cho, H. K.; Lee, J. Y. *Thin Solid Films* **2011**, *519*, 6801–6805.

[26] Bayraktaroglu, B; Leedy, K. In *Nanoelectronic Device Applications Handbook*; Morris, J. E.; Iniewski ,K., Eds. CRC Press: Boca Raton, FL, USA, 2013, pp. 677–691.

[27] Ming, Z. Y.; Gang, H. Y.; Xia, L. A.; Qing, W. *Chinese Phys. B* **2009**, *18*, 3966–3969.

[28] Yoon, Y.; Lin, J.; Pearton, S.; Guo, J. *J. Appl. Phys.* **2007**, *101*, 024301.

[29] Hossain, F. M.; Nishii, J.; Takagi, S.; Sugihara, T.; Ohtomo, A.; Fukumura, T.; Koinuma, H.; Ohno, H.; Kawasaki, M. *Physica E* **2004**, *21*, 911–915.

[30] Hossain, F. M.; Nishii, J.; Takagi, S.; Ohtomo, A.; Fukumura, T.; Fujioka, H.; Ohno, H.; Koinuma, H.; Kawasaki, M. *J. Appl. Phys.* **2003**, *94*, 7768–7777.

[31] Bentes, L.; Ayouchi, R.; Santos, C.; Schwarz, R.; Sanguino, P.; Conde, O.; Peres, M.; Monteiro, T.; Teodoro, O. *Superlattice Microst.* **2007**, *42*, 152–157.

[32] Amirhaghi, S.; Craciun, V.; Craciun, D.; Elders, J.; Boyd, I. W. *Microelectronics Engineering* **1994**, *25*, 321–326.

[33] Han, L.; Mei, F.; Liu, C.; Pedro, C.; Alves, E. *Physica E* **2008**, *40*, 699–704.

[34] Yu, C. F.; Sung, C. W.; Chen, S. H.; Sun, S. J. *Appl. Surface Sci.* **2009**, *256*, 792–796.

[35] Bayraktaroglu, B.; Leedy, K.; Neidhard, R. *Mater. Res. Soc. Symp. Proc.* **2010**, *1201*, H09–07.

[36] Amirhaghi, S.; Craciun, V.; Craciun, D.; Elders, J.; Boyd, I. W. *Microelectronics Engineering* **1994**, *25*, 321–326.

[37] Han, L.; Mei, F.; Liu, C.; Pedro, C.; Alves, E. *Physica E* **2008**, *40*, 699–704.

[38] Zhu, B. L.; Zhao, X. Z.; Su, F. H.; Li, G. H.; Wu, X. G.; Wu, J.; Wu, R. *Vacuum* **2010**, *84*, 1280–1286.

[39] Kim, H. W.; Kim, N. H. *Mat. Sci. Semi. Proc.* **2004,** *7*, 1–6.

[40] Wei, X. Q.; Zhang, Z. G.; Liu, M.; Chen, C. S.; Sun, G.; Xue, C. S.; Zhuang, H. Z.; Man, B. Y. *Mat. Chem. Phys.* **2007**, *101*, 285–290.

[41] Chang, S. J.; Cheralathan, M.; Bawedin, M.; Iniguez, B.; Bayraktaroglu, B.; Lee, J. H.; Cristoloveanu, S. *Solid State Electron.* **2013**, *90*, 134–142.

[42] Roland, A.; Richard, J.; Kleider, J. P.; Mencaraglia, D. *J. Electrochem. Soc.* **1993**, *140*, 3679–3683.

[43] Silveira, F.; Flandre, D.; Jespers, P. G. *IEEE J. Solid-St. Circ.* **1996**, *31*, 1314–1319.

[44] Binkley, D. M. *Trade-offs and Optimization in Analog CMOS Designs*; Wiley: West Sussex, England, 2008.

[45] Bae, H. S.; Im, S. *J. Vac. Sci. Technol. B* **2004**, *22*, 1191–1195.

[46] Navamathavan, R.; Choi, C. K.; Yang, E. J.; Lim, J. H.; Hwang, D. K.; Park, S. J. *Solid State Electron.* **2008**, *52*, 813–816.

[47] Bayraktaroglu, B.; Leedy, K.; Neidhard, R. *IEEE Electron Device L.* **2008**, *29*, 1024–1026.

[48] Chang, S. J.; Bawedin, M.; Bayraktaroglu, B.; Lee, J. H.; Cristoloveanu, S. In *IEEE International SOI Conference*, Tempe, AZ, USA, 3–6 October 2011, pp. 11–116.

[49] Armstrong, G. A.; Uppal, S.; Brotherton, S. D.; Ayres, J. R. *IEEE Electron Device L.* **1997**, *18*, 315–318.

[50] Valletta, A.; Bonfiglietti, A.; Rapisarda, M.; Mariucci, L.; Fortunato, G.; Brotherton, S. D. *J. Appl. Phys.* **2007**, *101*, 094502.

[51] Yamasaki, K.; Machida, E.; Horita, M.; Ishikawa, Y.; Uraoka, Y. *Jpn. J. Appl. Phys.,* **2012**, *51*, 03CA03.

[52] Scott, R. C.; Leedy, K.; Bayraktaroglu, B.; Look, D. C.; Zhang, Y. H. *Appl. Phys. Lett.* **2010**, *97*, 072113.

[53] Scott, R. C.; Leedy, K.; Bayraktaroglu, B.; Look, D. C.; Zhang, Y. H. *J. Cryst. Growth* **2011**, *324*, 110–114.

[54] Bayraktaroglu, B.; Leedy, K.; Neidhard, R. *IEEE Electron Device L.* **2009**, *30*, 946–948.