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Effects of annealing temperature on electrical characteristics of sputtered $Al/Al_2O_3/p$-Si (MOS) capacitors

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Abstract: The aim of this study is to investigate annealing effects on the electrical characteristics of aluminum oxide (Al_2O_3) MOS capacitors. Chemical changes after annealing have been characterized using the Fourier transform infrared spectroscopy prior to detailed electrical investigation. The influence of annealing temperature on electrical characteristics has been investigated by capacitance-voltage (C-V) and conductance-voltage (G/ω-V) curves. Effective oxide trap density (N_{ox}), border trap densities (N_{bt}), and interface trap densities (N_{it}) were calculated during the electrical analysis. Remarkable changes in the measurements were observed depending on the annealing temperatures. The obtained results demonstrate that the optimum annealing temperature is 450 °C for the Al_2O_3-based devices.

Key words: $Al/Al_2O_3/p$-Si (MOS) capacitors, annealing effect, interface states, series resistance

1. Introduction

Metal-oxide-semiconductor (MOS) capacitors have crucial significance in microelectronic applications. Initial device characterizations depending on the fabrication process can be easily examined by analysis of the capacitor structure. Several high-k gate dielectrics [1–4] have been extensively studied to replace conventional SiO_2 in order to improve device performance. Among them, Al_2O_3 could be one of the suitable ones owing to its large band gap (8.6 eV), high dielectric constant (8.4), suitable off-set values, and thermal stability with silicon. The performances of MOS-based devices are directly related to parameters during the deposition of dielectric layer, the series resistance (R_s), localized states at oxide (N_{ot} and N_{bt}), semiconductor oxide interface (N_{it}), etc. [5–9]. The annealing process, which should be carefully examined during device fabrication, has been performed after gate dielectric layer deposition to reduce the number of defects and impurities in the film. However, it is difficult to form a perfect dielectric/Si interface since it is hard to eliminate formation of the parasitic phase, e.g., Al/silicate, after the annealing process [10,11]. Also, possible phase transformation from amorphous to crystalline structure should be taken into account due to possible changes in the electrical characteristics of devices [7]. Hence, the specification of the optimum annealing conditions is quite important to fabricate reliable devices. In the present study, we have studied the annealing effects on the electrical characteristics of Al_2O_3 MOS capacitors. The optimum annealing temperature has been also specified. Capacitance-voltage (C-V), capacitance hysteresis, and conductance-voltage (G/ω-V) measurements have been performed, incorporating

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series resistance effects in order to assess the annealing influences on the electrical characteristics of Al_2O_3 MOS devices. In addition, chemical changes after the annealing process have been discussed with Fourier transform infrared (FTIR) spectroscopy prior to electrical characterizations.

2. Experimental details

Al_2O_3 thin film was deposited onto p-type (100) Si wafer with a nominal resistivity of 1– 4 Ωcm, which was cleaned following the standard RCA process, with a radio frequency magnetron sputtering system. A 99.99% pure Al_2O_3 sputtering target of 10.16 cm was used during deposition of the Al_2O_3 layer. The base vacuum degree of the chamber was below 7.5×10^{-4} Pa before the Al_2O_3 layer deposition. Vacuum degree was kept as 1 Pa and argon flow rate was adjusted to be 16 sccm during the film deposition. The sputtering was carried out at 300 W for 7 min. The film thickness was specified to be 115 nm by reflectometer. The usage of the Al_2O_3 as a dielectric layer in X-ray dosimetry will be investigated in further studies after specifying the optimum annealing conditions in this study. Hence, an Al_2O_3 layer of 115 nm was used in this work.

Following the deposition process, the Al_2O_3/Si film was divided into four pieces in order to study annealing effects on device characteristics. One of these pieces was kept as deposited and the others were annealed at 250 °C, 450 °C, and 750 °C in a nitrogen environment for 30 min, respectively. Basic film chemistry and observable influence of the annealing on the chemical characteristics of the Al_2O_3/Si structures by ATR-FTIR measurements were discussed. Following the FTIR measurements, the front or rectifier contacts were performed via 99.95% pure aluminum (Al) depositions by direct current sputtering at 150 W onto film surfaces using a shadow mask having circular dots of 1.00 mm in diameter. Base vacuum degree of the chamber was below 9.5×10^{-4} Pa before the Al deposition. Vacuum degree was kept as 1 Pa and argon flow rate was adjusted to be 16 sccm during the Al deposition. The thickness of the front Al contact was measured to be 500 nm. Following front contact formation, the backsides of the films were also coated with Al with the same deposition parameters for elimination of signal losses. All fabrication processes were performed class-100 clean room laboratories at Bolu Abant İzzet Baysal University, which minimized the possible environmental contamination during sample fabrication. Detailed electrical characterizations and optimum annealing temperature of Al_2O_3-based devices for microelectronics were specified by analyzing the C-V, capacitance hysteresis, and G/ω-V measurements. All electrical measurements were performed at room temperature in a dark environment.

3. Results and discussion

3.1. FTIR analysis of Al_2O_3/Si films

IR absorption spectra of the samples were measured after various annealing temperatures and the measurements are depicted in Figure 1. The observed peaks in IR spectra are numbered in Figure 1 and possible bonds are listed in Table 1 [12–15]. It was observed that multiple oxidation states formed depending on the annealing temperatures. Aluminum oxide was found in amorphous vibrational modes except 565 and 513 cm^{-1} for the as-deposited sample. However, the intensities of these peaks enhanced significantly after 450 °C annealing, which shows more microcrystallinity of the Al_2O_3. The decline of peak intensities after 750 °C annealing temperature may be due to degradation of O-Al-O and Al-O bonds. In other words, oxygen may diffuse from the Al_2O_3 bulk to the interfacial layer during high temperature annealing processes, which may change the interface chemistry [16]. The decline in the peak intensities of Al_2O_3 FTIR spectra after 750 °C annealing may be due to possible structural transformation of the initial interfacial layer to the SiO_x/$AlSiO_x$ layer [17]. The presence of these parasitic phases may significantly degrade the electrical performance of the devices.

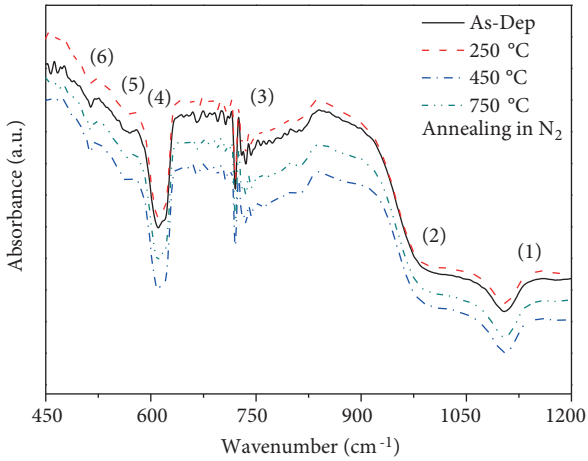

Figure 1. FTIR spectra of Al_2O_3/Si thin films at different annealing temperatures.

Table 1. Peak values corresponding to various vibrational modes in the FTIR spectra of the Al_2O_3/Si structure.

Number	Position (cm^{-1})	Mode type	Chemical bond
1	1101	TO stretching	Si-O
2	985	LO stretching	Al-O
3	739	Condensed tetrahedra stretching	Al-O_4
4	610	TO bending	Al-O_2
5	565	Condensed octahedra stretching	Al-O_6
6	513	Condensed octahedra stretching	Al-O_6

3.2. Annealing-dependent electrical characterization

The annealing influence on electrical capacitance and conductance measurements of Al_2O_3 MOS capacitors are illustrated in Figures 2a and 2b. It was observed that the electrical measurements drastically changed with the annealing temperature. Large flat band voltage shifts on the capacitance curve were observed after 250 °C annealing. Nonstoichiometric and weak bonds may occur after sputtered deposition of the layer. With annealing, these weak bonds, especially in the bulk oxide layer, may be broken and they may act as trap centers where mobile charges can be trapped. Hence, the large negative V_{fb} shift after 250 °C annealing is possibly due to broken weak bonds under the presence of thermal stress. The decreases in the peak intensities after 250 °C annealing temperature in FTIR measurements support this. When the annealing temperature was increased to 450 °C, the V_{fb} treatment was obviously observed. Bond formations occurred at higher temperatures (see intensities from Figure 1); thus, defect densities decreased. A significant reduction in capacitance was observed after 750 °C annealing of the devices. As discussed in FTIR analysis, possible interfacial SiO_x/$AlSiO_x$ layer formation can be observed after high temperature annealing. These parasitic phases enhance the equivalent oxide thickness of the dielectric layer and reduce the equivalent dielectric constant of the materials [7]; thus, the measured capacitances of the devices decrease significantly.

Similar fluctuations were observed for the conductance curves. One of the basic differences is that the peak value of the conductance curves continuously decreases with increasing annealing temperature. The observed decreases in the conductance indicate the reduction of the interface trap densities, which are analyzed in detail

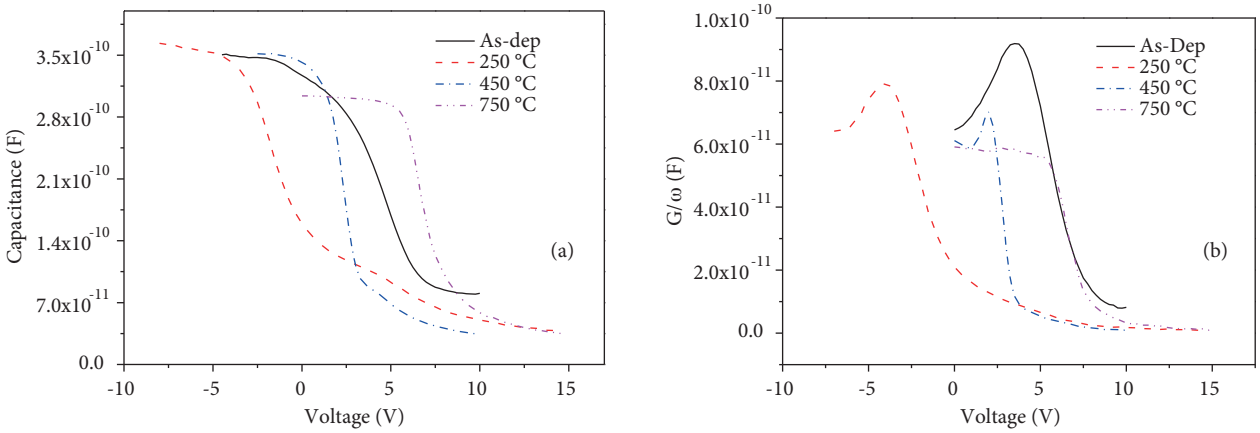

Figure 2. Variations of the a) capacitance and b) conductance curves of the Al_2O_3 MOS devices after different annealing temperatures.

later. In addition, the different shapes of the conductance curves depending on the annealing temperature are basically due to series resistance effects [9].

The presence of the trap sites and trapped charges in the device structure may significantly influence the device performance. Hence, specifications of these trap sites are crucial to fabricate reliable devices for microelectronic systems. These trap sites are basically the effective oxide trap density (N_{ox}), border trap density (N_{bt}), and interface trap density (N_{it}), and the trap site locations can be seen in Figure 3. The N_{ox} values depending on the annealing temperature are calculated using Eq. (1) [18]:

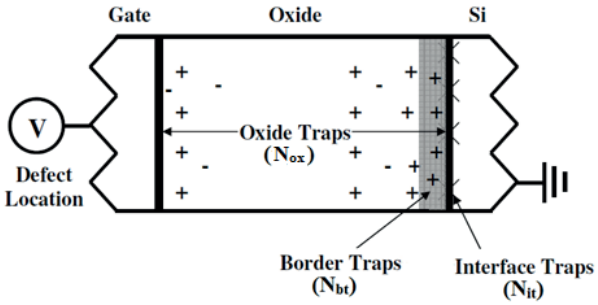

Figure 3. Important defect sites for the MOS structure that may influence electrical characteristics of the device [29].

$$V_{fb} = \phi_{ms} + \frac{Q_{eff}}{C_{ox}} \tag{1}$$

where Q_{eff} (qAN_{ox}) is the effective oxide charge density, ϕ is the work function differences between Si and Al, and C_{ox} ($\varepsilon_{ox}\varepsilon_0 A/d$) is the oxide capacitance value. The calculated N_{ox} values are listed in Table 2. The distribution of N_{ox} values verified the annealing treatment and the possible bond breaking and formation mechanism. The lowest N_{ox} value was obtained at 450 °C annealing temperature. This N_{ox} value is lower than other reported values in the literature [19,20], which is favorable for device applications in microelectronics.

Table 2. Some electrical parameters of Al_2O_3 MOS capacitors after various annealing temperatures.

Ann. tem. (°C)	V_{fb} (V)	N_{ox} ($\times 10^{11}$ cm^{-2})	N_{bt} ($\times 10^{11}$ cm^{-2})	R_s (ΩOhm)	$G_{c,max}$ ($\times 10^{-11}$ F)	C_c ($\times 10^{-10}$ F)	N_{it} ($\times 10^{11}$ eV^{-1} cm^{-2})
As-Dep	2.37	7.47	7.63	112	5.58	2.18	2.59
250	–2.63	12.3	3.89	77	4.29	2.37	2.29
450	1.60	4.31	2.19	80	4.41	2.25	2.15
750	6.25	23.4	2.09	82	1.68	1.65	0.58

Moreover, the capacitance hysteresis was measured and is given in Figure 4 to calculate N_{bt}. It was observed that the flat band shift in capacitance hysteresis ($\Delta V_{fb,hys}$) exhibits variations depending on the annealing temperature. The N_{bt} are special oxide traps that can respond to applied voltage frequencies and affect the device performance during operation. Thus, their values should be less than 10^{12} cm^{-2}. The N_{bt} have been calculated to assess the oxide quality using Eq. (2) from the flat band shift ($\Delta V_{fb,hys}$) in the capacitance hysteresis:

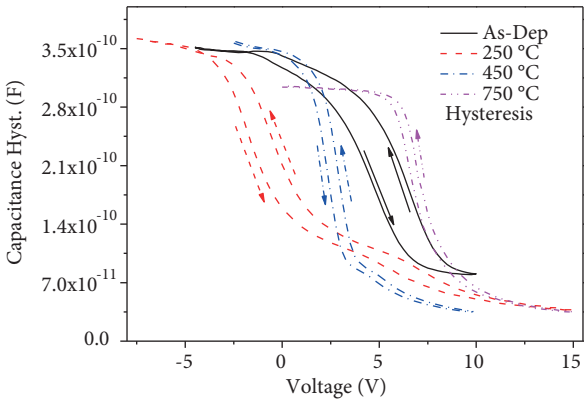

Figure 4. The capacitance hysteresis of Al_2O_3 MOS capacitors depending on annealing temperatures.

$$N_{bt} = \frac{(C_{ox} \times \Delta V_{fb,hys})}{qA}, \tag{2}$$

where q is the electrical charge and A is the front contact area. The calculated N_{bt} are listed in Table 1. Continuous decline in the N_{bt} values was obtained at higher annealing temperatures. The monotonic decreases in the N_{bt} values indicate the passivation of the dangling bonds and the improvement of the interface oxide quality.

The N_{it} values can be calculated by several methods, such as high-low frequency capacitance [8] and conductance methods [21]. The conductance method is one of the most accurate methods among the other techniques because the conductance signal is a direct measure of the majority carrier and states in the semiconductor band gaps [18]. However, the R_s values have significant effects on the conductance characteristics, e.g., they may mask real device characteristics [21]. Hence, series resistance correction must be performed before the N_{it} calculation. R_s can be calculated using the measured conductance (G_{ma}) and capacitance (C_{ma}) curves in strong accumulation using Eq. (3) [22]:

$$R_s = \frac{G_{ma}}{(G_{ma})^2 + (\omega C_{ma})^2}, \tag{3}$$

where ω is the angular frequency. The calculated R_s values are listed in Table 2. It was observed that the R_s value significantly decreased after 250 °C annealing, and then slightly increased with increasing annealing temperature. Using the obtained R_s values, the capacitance and conductance characteristics were corrected by using Eqs. (4) and (5), respectively [22,23]:

$$C_C = \frac{\left[(G_m)^2 + (\omega C_m)^2\right] C_m}{a^2 + (\omega C_m)^2}, \tag{4}$$

$$G_C = \frac{\left[(G_m)^2 + (\omega C_m)^2\right] a}{a^2 + (\omega C_m)^2}, \tag{5}$$

where $a = (G_m) - \left[(G_m)^2 + (\omega C_m)^2\right] R_s$, C_m is the measured capacitance, and G_m is the measured conductance. The comparisons between measured and corrected capacitance/conductance are shown in Figures 5a and 5b for as-deposited samples and those annealed at 450 °C, respectively. Slight rises were observed in capacitance curves, while the conductance of the device was significantly different after R_s corrections. Using the observed conductance peak, the N_{it} values were calculated via the Hill–Coleman technique [24]. Eq. (6) was used to calculate N_{it}:

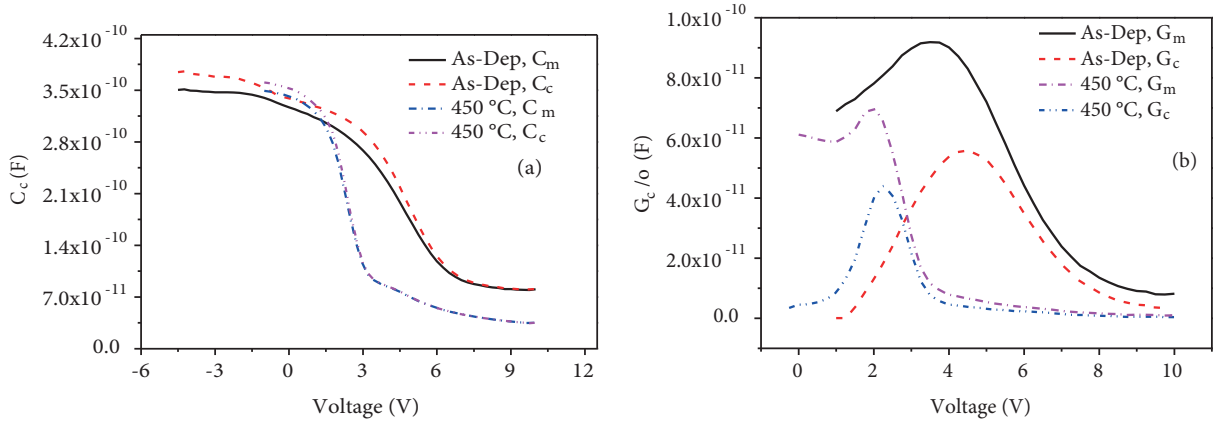

Figure 5. Variations of the corrected and measured a) capacitance and b) conductance for Al_2O_3 MOS capacitors.

$$N_{it} = \frac{2}{Aq} \frac{G_{\max}/\omega}{\left(G_{\max}/\omega C_{ox}\right)^2 + (1 - C/C_{ox})^2} \tag{6}$$

where ω is the angular frequency, G_{max} is the peak values of G/ω-V curves, and C is the capacitance of the MOS capacitors corresponding to G_{max}/ω. The required parameters to calculate N_{it} depending on the annealing temperature and the calculated N_{it} values are tabulated in Table 2. The values of N_{it} continuously decrease with increasing annealing temperatures and the lowest value is in the order of 10^{10} cm^{-2} after 750 °C annealing. Typical values of Al_2O_3/Si interfaces have been found in the order of 10^{12} to 10^{11} cm^{-2} [20,25,26]. It is known that the conversional SiO_2/Si and silicate-based interfaces can reach such low N_{it} values. Hence, such a low N_{it} value after 750 °C annealing points to the formation of the $AlSiO_x$/Si interface (the FTIR

results also support this observation), which increases the equivalent oxide thickness, resulting in reducing the capacitance of the device (see C-V curve after 750 °C annealing in Figure 2a). In other words, besides the decrease in the N_{it} value after 750 °C annealing, the formation of the parasitic interfacial layer degrades the electrical insulation of the device.

4. Conclusion

The annealing influences on the electrical characteristics of an Al_2O_3 MOS capacitor and observable chemical changes after annealing have been discussed. The peak intensities of Al-O bond stretching change with annealing temperatures and the most intense Al-O bonds were found at the annealing temperature of 450 °C. The decreases in the peak intensities after 750 °C annealing temperature may point to changes in the interface chemistry. In addition, annealing significantly modified the C-V and G/ω-V curves. The flat band voltage varied with annealing temperatures, and the oxide capacitance decreased after 750 °C annealing. These variations in the C-V and G/ω-V curves are attributed to generation/breaking of chemical bonds where mobile charges are trapped under annealing stress/treatment. The reduction of the capacitance after 750 °C annealing can be attributed to the formation of the parasitic silicate layer. Owing to these new bond formations, the N_{ox}, N_{bt}, and N_{it} values change with annealing temperatures. It has been reported that the trap sites must be in the order of 10^{10} to 10^{11} cm^{-2} for devices used in microelectronic applications [27,28]. In this study, the distributions of all N_{ox}, N_{bt}, and N_{it} values are in the order of 10^{10} cm^{-2} and no parasitic phase formation was observed for devices annealed at 450 °C. Hence, we may conclude that 450 °C annealing temperature is the optimum one for the fabrication of Al_2O_3-based devices.

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