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Effect of annealing temperature on structural, electrical, and UV sensing characteristics of n-ZnO/p-Si heterojunction photodiodes

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Abstract: The aim of this study is to investigate the influences of annealing temperature on initial device characteristics and their correlations with ultraviolet (UV) radiation sensitivity of n-type zinc oxide/p-silicon (n-ZnO/p-Si) heterojunction photodiodes. Evolutions on the crystalline structure, surface morphology, ideality factor, barrier potential, interface state density, and donor concentration were systematically analyzed during the initial device characterizations before testing the UV sensitivities of the photonic devices. The results demonstrate that the sensitivity of each n-ZnO/p-Si photodiode annealed at various temperatures was linearly correlated with different UV illumination intensities. The devices annealed at 750 °C and 550 °C exhibit more sensitive performance than devices annealed at 150 °C and 350 °C owing to lower dark currents and good oxide quality. However, the presence of an interfacial suboxide or silicate oxide layer significantly decreased the responsivity of the photodiodes annealed at 750 °C. The maximum responsivity value was 126 mA/W for the photodiode annealed at 550 °C. It can be concluded that the photodiode annealed at 550 °C exhibits promising performance for UV sensing applications.

 $\label{eq:keywords: UV photodetector, n-ZnO/p-Si heterojunction, UV sensor, photodiode, annealing temperature, ZnO thin film, optoelectronic$

1. Introduction

A wide-bandgap n-type semiconductor ($\sim 3.1-3.4$ eV) zinc oxide (ZnO) is an attractive material due to some important features such as good electrical and optical behaviors, direct band gap, and large exciton binding energy (60 meV) [1–3]. These features make ZnO an important material for optoelectronic applications, particularly in ultraviolet (UV) sensing applications [4–6]. ZnO has been recognized as a promising material for UV detection, and great efforts have been made to further improve the detection sensitivity of ZnO-based devices [7–9]. Several types of ZnO-based sensor structures such as PN heterojunctions [9], metal-semiconductormetal [10], photoconductors [11], and Schottky photodiodes [5] have been used for UV detection. Among these semiconductor sensor types, the PN junction photodiodes are particularly important compared to others for UV sensing applications owing to their fast response and high recovery speeds [12]. Hence, we have studied the PN heterojunction structure for UV detection applications.

Generation of initial electron-hole (e-h) pairs and current transports of these generated e-h pairs are crucial for efficient UV sensors. Hu et al. [13] reported that formation of Ag nanoparticle improves the photodiode sensitivity due to light scattering of the embedded Ag nanoparticles, which increase the numbers of generated pairs. Ko et al. [14] reported that nanowire formation enhances the UV sensitivity of the photodetectors almost

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three times because the generated e-h pairs can be easily transported to electrodes with lower annihilation. The annihilation of the generated e-h pairs during current transport significantly degrades the photosensitivity of the devices. Choi et al. [15] reported that the argon/oxygen ratio used in the deposition process affects the photosensitivity of the devices due to variations in the junction quality of the devices. On the other hand, Lee et al. [16] reported that the substrate temperature is also effective on the sensitivity of the devices owing to its influence on the structural quality of the ZnO. Large numbers of defect sites exist in film with poor oxide quality, which increases scattering and annihilation of carriers. Hence, the photodiode response is strictly connected to thin film quality. Heat treatments play a significant role to fabricate high-quality devices by improving structural and electrical properties [17]. Heat treatments may change the features of the ZnO layer by decreasing present strains and trap sites. So far, the effects of annealing temperature on the UV sensing properties of ZnO-based photodetectors have not been systematically investigated. Hence, the influences of various annealing temperatures on the structural and electrical characteristics of the n-ZnO/p-Si heterojunction are specified, and their correlations with the UV detection responses of the device are analyzed.

2. Experimental details

A p-type (100) Si wafer of 15.24 cm with 1-2 ohm-cm resistivity was used as a substrate in this study. The Si wafer was cleaned following the standard RCA cleaning process and dried with 6 N pure nitrogen gas. Immediately after cleaning and drying processes, the Si wafer was loaded to the sputtering chamber. During the sputtering deposition a circular ZnO target of 10.16 cm with 99.99% purity was used. The base pressure of the chamber was below 7.5 \times 10⁻⁴ Pa, and sputtering gas pressure was 1.0 Pa. A reactive gas mixture of ultrapure (6 N) Ar and O_2 was used during the sputtering. As oxygen easily reacts with the possible oxygendeficient zinc ions, presence of oxygen during the deposition may promote the deposition of the stoichiometric ZnO structure [18]. Ar flow rate was 16 sccm, while the O_2 flow rate was 1.0 sccm. The substrate was heated to 100 °C before the deposition process. Such low substrate temperature and oxygen concentration during the ZnO deposition were used to eliminate the possible formation of an interfacial SiO_x layer [15,19]. The presputtering was performed for 50 min in order to remove possible contaminations from the target surface. Commercial sputtering was then performed at 300 W for 25 min. After the semiconducting layer deposition, the film thickness was measured as 170 nm via an Angstrom Sun spectroscopic reflectometer. The deposited sample was divided into four pieces. Each piece was annealed at 150 °C, 350 °C, 550 °C, and 750 °C under nitrogen ambient for 30 min, separately. The first annealing temperature was selected for the substrate temperature due to treatment of shallow defect sites and to investigate the electrical performance of devices without changing the crystallinity and microstructure of the ZnO layer. A piece of the annealed sample was also cut to investigate crystallographic and morphologic evolutions of the films by X-ray diffractometry (XRD) and atomic force microscopy (AFM), respectively. The rest of the samples were loaded into the sputtering chamber in order to fabricate front interdigital electrodes onto the n-ZnO surface. Shadow masks were used for the formation of the interdigital electrodes. The interelectrode spacing was 1.0 mm and the active spacing was $1.0 \text{ cm} \times 1.0 \text{ cm}$. Aluminum (Al) deposition was performed at 150 W via direct current sputtering to form front contacts. Following the front contact deposition, the samples were annealed at 150 $^{\circ}$ C for 20 min in a nitrogen environment to reduce possible contact resistance. After that, the whole silicon surface of the samples was coated with silver (Ag) paint. Al and Ag were used as electrode materials to obtain ohmic type contact behavior. A complete schematic structure of the produced n-ZnO/p-Si heterojunction photodiode and some additional details of the interdigital electrode are shown in Figure 1.



Figure 1. Schematic structure of the fabricated n-ZnO/p-Si heterojunction photodiodes.

Electrical capacitance-voltage (C-V) and current-voltage (I-V) measurements of the photodiodes were performed by using a Keithley 4200-SCS in a dark environment. A 60 lumen UV torch having approximately 395 nm wavelength was used as a light source during I-V measurements under UV illumination. The fluxes of UV illumination were calibrated with a HoldPeak lux meter.

3. Results and discussion

Figure 2 shows the XRD pattern of n-ZnO/p-Si (100) film structures annealed at various temperatures. One single ZnO and substrate peaks in the XRD spectra have been observed for all samples. The observed peak in the XRD measurements was indexed with the International Centre for Diffraction Data (ICDD) with Card No: 65-3411. The XRD spectra of the samples reveal that the ZnO thin films exhibit wurtzite structure with single phase along the c-axis as the preferred orientation. Similar highly textured single-phase ZnO film structures have also been reported via a different deposition technique [20]. On the other hand, the intensity of the XRD peak increases up to 750 °C, which demonstrates that high temperature enhances the crystalline quality of the film. Up to a limit, increases in the annealing temperature enhance the surface mobility of the deposited atoms, which provides better crystalline quality of the films [21]. Dang et al. reported that interfacial nonstoichiometric SiO_x or Zn_xSi_yO_z layers can be formed at the ZnO/Si interface when temperatures reach 750 °C or higher [22]. The presence of the interfacial layer may generate additional stress/strains on the film. The decrease in the peak intensity and the shift in the peak position towards lower angles after 750 °C annealing can be attributed to the possible formation of the interfacial layer.

Average grain size (G) values were calculated by the Debye–Scherrer equation:

$$G = \frac{0.9\lambda}{\beta Cos\left(\theta\right)} \quad , \tag{1}$$

where λ is 1.54 Å, β is the full width at half maximum (FWHM) value of the (002) diffraction peak, and θ is half of the peak angle. The calculated *G* values are listed in the Table, gradually increasing from 22.3 to 33.1 nm as the annealing temperature rises. Randomly deposited atoms can be aggregated in a larger cluster with higher thermal energy. Thus, the grain size of the samples increases at high annealing temperatures. These obtained values are better than earlier reported values [23,24]. Similar single-crystal ZnO film deposited at low temperature and a high deposition rate has been reported in the literature [25].

Figures 3a–3d show the AFM images of n-ZnO/p-Si films annealed at various temperatures. It has been observed that the formation of a spherical-like shape becomes more prominent when the annealing temperature



Figure 2. The XRD spectra of n-ZnO/p-Si thin films annealed at various temperatures.

Anneal.	Grain	RMS	I_o	n	ϕ_b	D_{it}	N_d	$\operatorname{Res}(A/W)$
temp. (°C)	size (nm)	value (nm)	(μA)		(eV)	$(\times 10^{11} \text{ eV}^{-1} \text{ cm}^{-2})$	$(\times 10^{15} \text{ cm}^{-3})$	ponsivity
150	22.3	3.47	1260	2.22	0.56	1.82	1.35	0.014
350	31.7	4.10	0.995	2.10	0.74	1.57	5.11	0.071
550	32.4	4.22	0.546	1.84	0.76	1.72	1.34	0.126
750	33.1	4.32	3.760	2.38	0.71	1.53	2.46	0.062

 ${\bf Table.} \ {\rm Some \ structural \ and \ electrical \ parameters \ of \ n-ZnO/p-Si \ heterojunction \ photodiodes.}$

exceeds 350 °C. In addition, the distribution of the individual columnar grains extends upwards (c-axis) with high annealing temperature. The root means square (RMS) surface roughness values are listed in the Table. It has been observed that the RMS values increase with annealing temperature. The observed increases in the RMS values are due to the increases in the grain size [26]. Higher annealing temperatures improve the grain growth, which may also increase the porosity of the films [27]. Although the RMS values are higher than an ideal smooth surface (a few angstroms), they are still in a comparable range for ZnO-based devices used in various applications [2,28,29].

Figure 4a shows the I-V characteristics of the n-ZnO/p-Si heterojunction photodiodes in semilogarithmic scale after annealing at different temperatures. The samples exhibit rectifying behavior. Threshold voltage and reverse bias current change with annealing temperatures. Among the samples, the device annealed at 150 °C does not exhibit the expected I-V curves. A large shift in the threshold voltage and kinks in the I-V curve have been observed for the device annealed at 150 °C. The observed nonidealities indicate poor quality of the n-ZnO/p-Si interface [30]. It is known that during the deposition, atoms are almost randomly sputtering onto the substrate surface. Hence, large numbers of defect sites can be formed [31]. A temperature of 150 °C is possibly not enough to treat these defect sites in the device structure. The I-V curves of the device were considerably changed after annealing at higher temperatures. The threshold voltage approaches 0 V and the reverse bias current increases after 350 °C annealing. It has been reported that mobility increases with increasing grain size [27], and the presence of localized defect sites may act as a leak path. Hence, the rise in the reverse current (dark current) is associated with the crystallization of the ZnO layer. Although the crystallization continues to enhance after 550 °C annealing, the dark current decreases may be related to the improvement of the bulk



Figure 3. AFM pictures of the n-ZnO/p-Si films annealed at a) 150 °C, b) 350 °C, c) 550 °C, d) 750 °C.

oxide quality. On the other hand, further decrease in the dark current after 750 $^{\circ}$ C may be due to formation of the parasitic layer, which may behave like an insulating layer against the current flow.

Moreover, the measured I-V curves of the n-ZnO/p-Si heterojunctions have been analyzed using standard thermionic theory. In this theory, the forward current, which is obtained when the positive voltage is applied to p-Si, can be denoted as follows [32]:

$$I = I_o \left[\exp(\frac{qV}{nkT}) - 1 \right], \tag{2}$$



Figure 4. The a) semilog I vs. V and b) $\ln(I)$ vs. V characteristics of n-ZnO/p-Si heterojunctions photodiodes at various annealing temperatures.

$$I_o = A^* A T^2 \exp(-\frac{q\Phi_b}{kT}),\tag{3}$$

where I_o, q, n, k , and T are the saturation current, electronic charge, ideality factor, Boltzmann constant, and temperature, respectively. In addition, I_o is correlated with the electrode area (A), Richardson constant (A^{*}), and barrier height (ϕ_b). Using the given relations, n can be denoted as [33]:

$$\frac{1}{n} = \frac{kT}{q} \left(\frac{dlnI}{dV}\right) \quad . \tag{4}$$

The *n* values were calculated using the slope of the $\ln(I)$ -V curves. The $\ln(I)$ -V curves are shown in Figure 4b. Using the fit function of data given in Figure 4b for Eqs. (2)–(4), I_o , n, and ϕ_b values were calculated for both samples. These parameters are also listed in the Table. The I_o value for the device annealed at 150 °C was much higher than the expected values due to a large number of surface states. Hence, the I-V curve of the sample annealed at 150 °C cannot be accurately described with Eqs. (2)–(4) [30]. The n value decreased after annealing reached 750 °C because of possible decreases in the surface states' densities [27]. Atoms are randomly deposited and weakly bonded with each other in low temperature deposition processes in the physical vapor deposition methods. Hence, large numbers of dangling and broken bonds, which may act as trap sites, are present in the film structure. With high annealing temperature, the Zn and O atoms gain the required activation energy to complete their bonds. Effective surface oxidation occurs at high annealing temperatures [34], which decrease the surface state densities. On the other hand, the ϕ_b values varied from 0.56 to 0.76 eV depending on the annealing temperatures. The observed rises in n and decreases in ϕ_b values after 750 $^{\circ}$ C annealing are also associated with the formation of the interfacial layer, which degrades the stoichiometric structure of the ZnO/Si interface [23]. However, the obtained n and ϕ_b values are almost as good as or even better than those of n-ZnO/p-Si heterojunction devices reported in previous studies [28,35–37].

Figure 5a shows capacitance vs. voltage curves of the devices at high frequency (1 MHz). Similar to the I-V curve, kinks corresponding to accumulation regions have been observed after 150 °C annealing, indicating



Figure 5. The a) C-V and b) C⁻²-V characteristics of the n-ZnO/p-Si heterojunctions at 1 MHz.

poor oxide and interface quality. The presence of a capacitance peak for the device annealed at 350 °C may be due to series resistance effects. The devices annealed at 550 °C and 750 °C exhibit ideal C-V curves with clear accumulation, depletion, and inversion regimes. However, the decline in capacitance after 750 °C annealing is associated with the presence of the interfacial layer formation. The dielectric constants of the parasitic SiO_x (ε : ~3.9) or Zn-containing silicate (ε : ~6.5) layers are lower than ZnO (ε : ~8.5). The formations of these parasitic layers decrease the equivalent dielectric constant of the devices. Hence, the measured capacitance decreases after 750 °C annealing process [38]. On the other hand, the interface state densities (D_{it}) were calculated using the high frequency capacitance (in Figure 5a) and low frequency capacitance (not shown here) techniques [39]. The calculated D_{it} values are given in the Table. It has been observed that the values of D_{it} varied from 1.82×10^{11} to 1.53×10^{11} eV⁻¹ cm⁻² depending on the annealing temperatures. These values are in the same order as those of a previously published n-ZnO/p-Si interface [28].

Figure 5b shows the inverse square of the capacitance-voltage $(C^{-2}-V)$ relations of the devices in order to investigate donor states (N_d) distribution of the n-ZnO layer. The C^{-2} curves were given for voltage regimes from depletion to inversion where the N_d distribution could be easily analyzed. C^{-2} almost linearly changed with applied voltage except when the device was annealed at 150 °C. The linear $C^{-2}-V$ relations indicate that the dopant concentrations are uniform [35], and the rectifying behavior of devices is associated with the n-ZnO/p-Si interface [40]. The capacitance of the devices can be expressed by using the following expression:

$$C^{2} = \frac{A^{2}qN_{D}N_{A}\varepsilon_{1}\varepsilon_{2}}{2\left(N_{D}\varepsilon_{1} + N_{A}\varepsilon_{2}\right)\left(V_{bi} + V\right)},\tag{5}$$

where A is the area of the device; N_d and N_a (8.0 × 10¹⁵ cm⁻³ calculated from surface resistivity of p-Si used in the process) are the donor density in n-ZnO and acceptor density in p-Si; and ε_1 and ε_2 are the permittivities of the of n-ZnO and p-Si, respectively [35]. The N_d values were calculated from the slopes of the C⁻²-V curves as given in the Table. The N_d values varied from 1.34×10^{15} cm⁻³ to 5.11×10^{15} cm⁻³ depending on the annealing temperatures. These variations may be due to the annealing-induced changes in the crystalline structure and electrochemical changes of the film structures [4].

Figures 6a-6d show the I-V characteristics of n-ZnO/p-Si heterojunction photodiodes under dark and

continuous UV illumination. Remarkable changes have been observed in the reverse current of devices under UV illumination (I_{uv}) as compared to dark current. The operation of the photodiode can be summarized in three steps: 1) First, a large number of e-h pairs is generated by the absorption of incident UV-light. 2) A number of generated e-h pairs, which escape from initial recombination, are then transported by the internal electric field in the depletion region. This step explains why the photocurrent (I_{ph}) becomes distinguishable in reverse bias regions. Under forward bias, the charge separation of the generated carriers cannot be formed. Thus, the generated e-h pairs recombine, which significantly decreases the I_{ph} . 3) Finally, the I_{ph} is obtained by external circuit [41]. In addition, the observed voltage shifts of the I-V characteristics under UV illumination are associated with the I_{ph} , which affects the depletion edge between the n-ZnO and p-Si.

The UV sensitivities of the heterojunction photodiodes were calculated in order to investigate the annealing influences on the device sensitivities. The sensitivity (S) values were calculated at 2 V under various UV fluxes using the following relation [41]:

$$S = \frac{I_{ph}}{I_{dk}} = \frac{I_{uv} - I_{dk}}{I_{dk}} \times 100.$$
 (6)

The UV sensitivities of devices under different flux densities are illustrated in Figure 6e. The S values change almost linearly depending on the UV flux densities for both devices annealed at different temperatures. The device annealed at 350 °C exhibits lower sensitivity, which is related to the high dark current values (see Figure 4a). An evident relation between dark current and sensitivity has been observed. The devices that have low dark currents exhibit high sensitivity, except the device annealed at 150 °C. As mentioned above, the atoms are randomly deposited onto the Si surface, and 150 °C is not enough for the treatment of the possible defect sites. The presence of higher trap sites on the device structure may affect the recombination ratio of the generated e-h pairs and may extend the lifetime of carriers [41]. Thus, these may degrade the device sensitivity.

Moreover, the UV sensitivity of the devices has also been assessed by calculating the responsivity (R) of the photodiodes. The R values of the photodiodes are strictly connected to the incident light wavelength, applied reverse bias, and structural quality of the absorbing layer [42]. The R values of the devices were calculated by using the following relation [9,40]:

$$R = \frac{I_{ph}(A)}{P_{inc}(W)} = \frac{I_{ph}(A)}{E(W/cm^2)A(cm^2)},$$
(7)

where P_{inc} is the incident power of the UV illumination. The calculated R values under UV illumination at 2 V are given in the Table. As expected, the R-values exhibit variations depending on the annealing temperature, and the maximum R-value is obtained to be 126 mA/W for the photodiode annealed at 550 °C. This value is good; it is even better than previously reported R-values in the literature of the same incident UV wavelength for similar n-ZnO/p-Si heterojunction photodiodes [4,43]. However, the obtained R-value should be improved compared to the specialized nanowire structure of ZnO₂-based photodiodes for UV detection [14]. Nevertheless, the device annealed at 550 °C exhibits promising performance for UV sensing applications.

4. Conclusion

The effects of annealing temperatures on initial device characteristics and the UV detection response of n-ZnO/p-Si heterojunction photodiodes have been investigated. Highly textured ZnO layers were deposited on



Figure 6. The I-V curves before and after various UV flux densities of n-ZnO/p-Si heterojunction photodiodes annealed at a) 150 $^{\circ}$ C, b) 350 $^{\circ}$ C, c) 550 $^{\circ}$ C, and d) 750 $^{\circ}$ C; e) sensitivity vs. UV flux curves of the photodiodes.

the Si substrate, and the crystalline structure of the films increased when increasing the annealing temperature up to 750 °C. Further increase of the annealing temperature caused a decline in the peak intensity and a shift of the peak angle, which was possibly due to the formation of the interfacial SiO_x and/or silicate layer. The surface roughness of the films increased from 3.47 to 4.32 nm with increasing annealing temperature. Several factors including the crystalline structure of the ZnO, oxide quality, and formation of the interfacial layer significantly influenced the dark current, I_o, n, ϕ_b, D_{it} , and N_d values of the devices. Furthermore, linear S-UV flux relations were obtained for all devices. However, the devices annealed at 550 °C and 750 °C exhibited more sensitive performance due to lower dark current and good oxide quality. The responsivity of the devices annealed at 750 °C significantly decreased, which was due to the presence of an interfacial SiO_x or silicate oxide layer. The interfacial layers may block some of the photocurrents or decrease the initial photogenerated electron-hole yields due to their higher band gap energy than ZnO. Hence, the maximum *R*-value was obtained to be 126 mA/W for the heterojunction photodiode annealed at 550 °C. It can be concluded that the device annealed at 550 °C exhibits promising performance for UV sensing applications.

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