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Feasibility of the GaInP/InGaAs/GaAs System for Modulation Doped Field-Effect Transistors

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Abstract

Si-doped single $Ga_{0.51}In_{0.49}P$ layers and GaInP/InGaAs/GaAs modulation doped field-effect transistor structures grown by gas source molecular beam epitaxy were characterized in detail through Hall-Effect and Deep Level Transient Spectroscopy techniques. Electrical characterization of the undoped and moderately Si-doped ($N_D = 3x10^{17}$ cm^{-3}) GaInP layers yielded an electron trap with an activation energy of 0.75 eV and a temperature dependent capture cross section with a capture barrier of 0.593 eV showing DX center properties. The trap was not detected in highly Si doped ($N_D = 4x10^{18}$ cm^{-3}) as grown layers suggesting that it is a defect complex including a residual impurity. An anomalous decrease in the free carrier concentration of GaInP was observed after the samples were annealed at temperatures typically used in device processing. While other explanations may be possible, this can be attributed to Si atoms moving from donor to acceptor sites. Very high two-dimensional electron gas density ($2.6x10^{12}$ cm^{-2} at 30 K) was achieved in the lattice matched (x=0) structure. The strained structures were found to be very sensitive to heat treatment and another level with dislocation trap characteristics was detected in these structures. Persistent photoconductivity and a significant reduction in the interface sheet electron density were observed in the strained samples after annealing. This can partly be attributed to the strain relaxation at the heterointerface. With no detectable traps in heavily Si-doped GaInP and with very high two dimensional electron gas densities, GaInP/InGaAs/GaAs seems to be a promising material system for modulation doped field-effect transistor applications.

1. Introduction

AlGaAs/GaAs is an important and widely used material system for electronic and optical device applications. However, the presence of donor related deep traps (DX centers) in Si-doped AlGaAs has been an important problem especially in modulation doped field

effect transistor applications. DX centers cause I-V collapse and persistent photoconductivity (PPC) at low temperatures where device performance is expected to be superior. Recently, $Ga_{0.51}In_{0.49}P$ (hereafter called GaInP), which is lattice matched to GaAs, has received increasing attention to replace AlGaAs in the $Al_xGa_{1-x}As/GaAs$ system. The advantages of GaInP over AlGaAs are well known [1]. It is believed that the DX center density becomes significant at compositions close to the crossover of the direct and indirect conduction bands. The crossover occurs at x=0.37 in $Al_xGa_{1-x}As$, and at x=0.74 in $Ga_xIn_{1-x}P$. While DX center density can be reduced to an acceptable level by using Al mole fractions lower than 0.2 in $Al_xGa_{1-x}As$, low Al mole fraction results in very small conduction band discontinuity and inferior electron confinement at the hetero-interface. On the other hand, at the composition lattice matched to GaAs (x=0.51), GaInP is far from the crossover point with a sufficiently large conduction band discontinuity at the GaInP/GaAs interface. Therefore, DX center density is assumed to be negligible in this material.

Based on the earlier experimental work [2,3] reporting the absence of deep traps in n-doped GaInP, the material has attracted some interest for modulation doped field-effect transistors (MODFETs) [4-6]. However, several studies reported recently indicated the presence of deep levels in GaInP [7-16]. Amor et al.[11] observed PPC in Metalorganic chemical vapor deposition (MOCVD) grown modulation-doped GaInP/GaAs heterostructures, and they related this to a DX-like center. Elhamri et al. [8] observed PPC in MOCVD grown undoped GaInP/GaAs quantum wells, and they attributed it to the photoionization of deep donors in GaInP. Krynicki et al. [9] characterized MOCVD grown, Si doped GaInP/GaAs heterostructures, and observed a level with an ionization energy of 0.435 eV but located 20 meV below the conduction band. They related this level to a DX center. Huang et al. [12] reported two electron traps located 0.28 eV and 0.51 eV below the conduction band in molecular beam epitaxy (MBE) grown GaInP/GaAs heterostructures. They attributed these traps to phosphorous vacancies and related defects and complexes. Kwon et al. [14] investigated the deep traps in undoped and Si-,S-,Se, Te-doped GaInP layers grown on GaAs substrates by liquid phase epitaxy (LPE). They observed similar trap characteristics in undoped and S-doped layers with an activation energy of 0.26 eV, and only S-doped sample exhibited PPC. They attributed the S-related deep level to a DX center. Paloura et al. [15] studied the dopant dependence of the deep levels and the PPC effect in metalorganic molecular beam epitaxy (MOMBE) grown undoped, S-doped and Si-doped GaInP/GaAs heterostructures. The undoped layers were characterized by a trap with an activation energy of 820 to 875 meV which was suppressed by S and Si doping. Doping yielded a new trap at 315 meV which was related to a DX like center. It was also observed that PPC was suppressed only by Si doping.

Conflicting reports and conclusions presented in the literature suggest that more work needs to be done on the investigation of the GaInP and GaInP/GaAs heterostructures. In this paper, we present the results of a detailed study on the characteristics of the traps in Si-doped GaInP and on the transport properties of modulation doped GaInP/InGaAs/GaAs heterostructures with different channel In mole fractions.

2. Growth Procedure

GaInP layers (1 mm thick) at various Si doping levels and GaInP/$In_xGa_{1-x}As$/GaAs modulation doped field effect transistor structures were grown by gas source molecular beam epitaxy at 510°C on superclean semi-insulating GaAs substrates. At this growth temperature, GaInP had a badgap of 1.895 eV which was measured with low-power room temperature photoluminescence. Modulation doped heterostructures are shown in Figure 1.

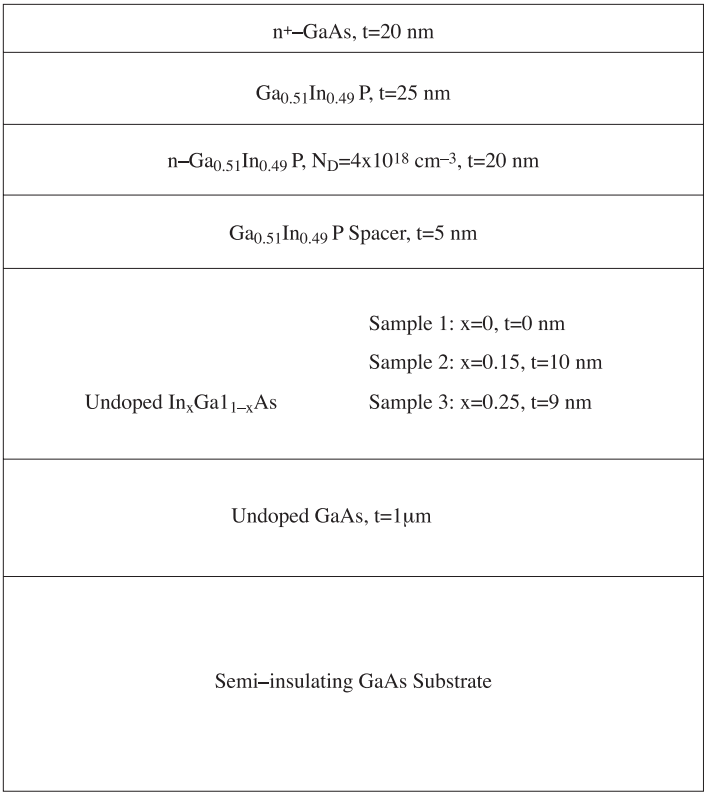

Figure 1. Grown MODFET structures

The thicknesses of the InGaAs layers in the strained structures were chosen to be sufficiently below the theoretical critical thickness. Flux of arsine was 3 sccm, and the flux of phosphine was 7 sccm. The substrate was rotated at 20 rpm during the growth. Run-Vent switching was used to allow fast switching times, and there was no growth interruption at the GaInP/GaAs interface. However, a growth interruption of 1 second was used at the GaAs/GaInP interface in order to ensure that all the arsine was pumped out before switching the phospine in. The growth rates of different layers in the heterostructure were determined by surface profiling on the test layers after a step etch and comparing

the result with that predicted from reflection high energy electron diffraction (RHEED) oscillations. The composition of the InGaAs layer was calibrated by using bulk InGaAs test layers grown on GaAs substrate. RHEED oscillations were used to establish relative fluxes of indium and gallium. The amounts of indium and gallium incorporated into the solid were calculated based on the x-ray mismatch of the bulk InGaAs layer, assuming that the layer was relaxed. Photoluminescence measurements were made on the bulk InGaAs samples in order to corroborate the composition determined by x-ray diffraction. The room temperature photoluminescence spectrum for the bulk $In_{0.1}Ga_{0.9}As$ sample is shown in Figure 2. Silicon cell doping calibration was done by growing staircase structures on n^+-GaAs substrate and measuring the doping profile with an electro-chemical capacitance voltage profiler. The grown layers exhibited mirror-like morphology.X-ray diffraction full width at half maximum (FWHM) values measured on the single GaInP layers were in the range of 20-30 arcsec being comparable to the best values reported in the literature.

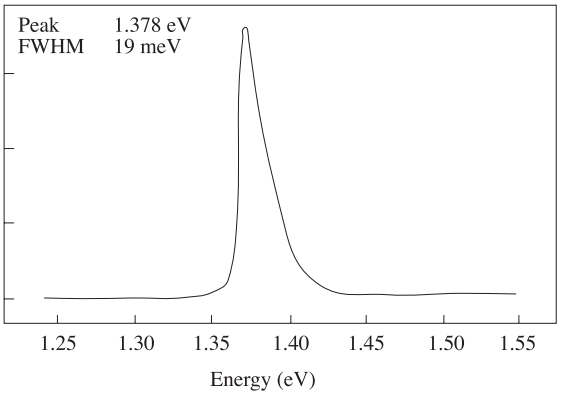

Figure 2. Room temperature photolumunescence spectrum for the bulk $In_{0.1}Ga_{0.9}As$ sample

3. Trap Characterization

In order to investigate the electrical properties of the single GaInP layers, we performed variable temperature (30-300 K) Hall-Effect characterization. Before the Hall-Effect measurements, the samples were mounted on small pieces of microscope slide glass, and the GaAs substrates were removed by etching in a H_2O_2:H_2O:H_3PO_4 solution. Due to the small thickness of the grown layers (1 mm), substrate removal process is quite difficult. However we observed that the measurements strongly reflect the properties of the 2DEG forming at the layer substrate interface, if the substrate was not removed.

The results of the Hall-Effect measurements on a highly doped $Ga_{0.51}In_{0.49}P$ layer ($N_D \approx 4x10^{18}$ cm^{-3}) are presented in Figure 3. The layer did not exhibit any persistent conductivity before and after annealing at 400°C. However, a considerable reduction in the carrier concentration and an increase in the electron mobility was observed after annealing at this temperature for 15 minutes. After 1 minute annealing at 550°C, the

layer became highly resistive, and reliable measurements could not be taken at dark. However, we observed strong PPC with a very large time constant (several minutes).

The characteristics of the traps in as grown and annealed layers were investigated through the deep level transient spectroscopy (DLTS) technique. Schottky diodes were fabricated on the samples by evaporating Au. The measurements on a moderately doped as grown layer ($N_D = 3x10^{17}$ cm^{-3}) yielded only one trap with an activation energy, E_a, of 0.75 eV. The related Arrhenius plot is shown in Figure 4. DLTS peak height of this trap was observed to depend on the temperature suggesting a temperature dependent capture cross section. In order to obtain the capture cross-section, the temperature variation of the trap occupancy given by the ratio of the DLTS peak amplitude to the maximum peak value was used [9,17] and the resultant capture cross section was found by fitting to be

$$\sigma_n(\text{ cm }^2) = 1.3x10^{-12}\exp[-0.593(eV)/kT] \quad (1)$$

with a capture barrier height, E_b, of 0.593 eV. The density of the trap in the as grown layer was $1x10^{14}$ cm^{-3} as calculated from the saturated DLTS peak height for a filling pulse width of 0.05 sec. The thermal ionization energy, E_t, of this trap was determined to be 20 meV from the measured temperature dependence of the carrier concentration obtained through the Hall-Effect measurements. The activation (emission) energy, E_a, obtained from DLTS measurements can be expressed as $E_a = E_b + E_t$. E_a is 0.75 eV and Eb is around 0.6 eV as determined from the DLTS measurements. The difference between E_a and E_b is 0.15 eV which was expected to be equal to the thermal ionization energy determined from the Hall measurements. Such large discrepancies between the values of the thermal ionization energies determined by Hall measurements and those obtained from DLTS measurements are typically observed [18], and they can be attributed to the different temperatures at which these measurements were taken. With such a large capture barrier and small capture cross section, the trap shows characteristics similar to those of DX centers.

No detectable traps were observed on the as grown highly doped ($N_D = 4x10^{18}$ cm^{-3}) sample showing that Si doping is not responsible for the 0.75 eV trap observed in the moderately doped sample. DLTS characterization of the undoped GaInP layers was performed on a lattice matched modulation doped field effect transistor structure (sample 1). DLTS measurements yielded the same trap observed in the moderately doped sample. The DLTS spectrum of this trap is shown in Figure 5.

DLTS measurements on a strained $Ga_{0.51}In_{0.49}P/In_{0.15}Ga_{0.85}As/GaAs$ structure with an channel thicknes of 150 A yielded the spectrum shown in Figure 6. Under low reverse bias, only trap B was observed. This trap yielded characteristics similar to the trap observed in the lattice matched sample. When the reverse bias level was increased, the second trap (A) appeared with DLTS peak intensity dependent on the filling pulse width. The activation energy and the capture cross section of this trap were calculated to be 0.422 eV and $2.8x10^{-17}$, respectively. The DLTS peak height was found to be linearly dependent on the logarithm of the filling pulse width. This characteristic is known to be the fingerprint of traps associated with extended defects such as dislocations. The

results suggest that strain relaxation occurs at the interface even though the InGaAs layer thickness is below the theoretical critical thickness.

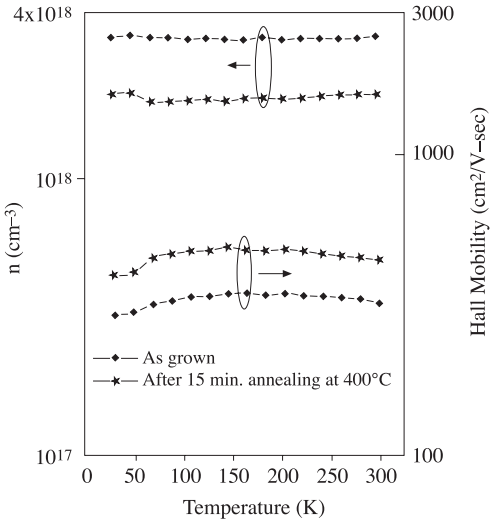

Figure 3. Results of the Hall-Effect measurements on the highly doped single GaInP layer (substrate is removed).

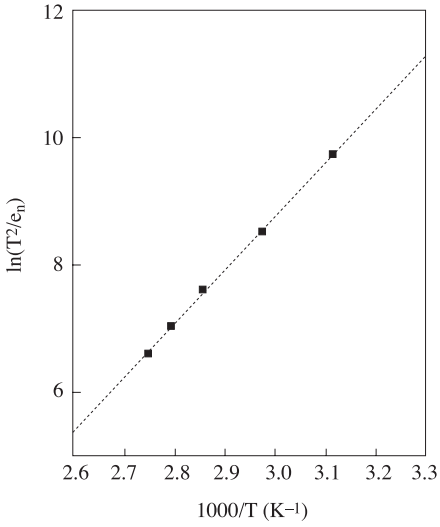

Figure 4. Arrhenius plot of the 0.75 eV deep trap observed in GaInP.

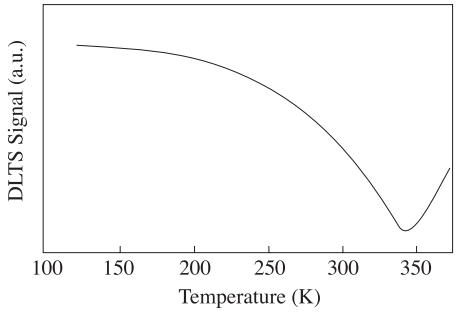

Figure 5. DLTS spectrum of the trap observed in the lattice matched sample.

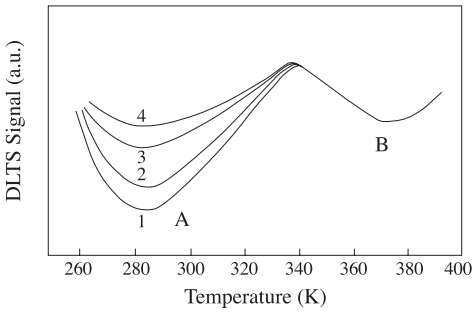

Figure 6. DLTS spectrum of a strained $GaInP/In_{0.15}Ga_{0.85}As/GaAs$ sample with InGaAs channel thickness of 150 $\AA$

In order to investigate the effects of annealing on the trap characteristics, DLTS measurements were repeated after annealing the single GaInP layers at various temperatures. The measurements on the moderately doped ($N_D \approx 3x10^{17}$ cm^{-3}) single GaInP layer yielded trap concentrations of $9x10^{14}$ cm^{-3} and $1.4x10^{15}$ cm^{-3}, corresponding to 15 minute 400°C and 1 minute 550°C annealing cases, respectively. In the as grown layer,

the trap concentration was $1x10^{14}$cm^{-3}. The net doping concentration ($N_D - N_A$) in this layer decreased to $9.6x10^{16}$ cm^{-3} after 550°C annealing. Measurements on the highly doped layer ($N_D = 4x10^{18}$ cm^{-3}) did not yield any trap after400°C annealing. However after 1 minute annealing at 550°C, the 0.75 eV deep trap observed in the undoped and moderately doped layers was also detected in the heavily doped layer with a density of $2.8x10^{14}$ cm^{-3} and the net doping concentration in this layer decreased to $1.4x10^{16}$ cm^{-3}.

4. Transport Properties

After trap characterization, variable temperature Hall-Effect measurements were performed on the GaInP/$In_xGa_{1-x}As$/GaAs MODFET structures (samples 1-3) in order to observe the effects of the channel In mole fraction and annealing on the transport properties of the structures. In order to check the presence of persistent photoconductivity in the samples, the measurements were taken under both dark and after illuminating the sample. The results are presented in Figure 7. Measurements labeled light were taken by cooling the sample to 30 K in dark, illuminating the sample until the light induced change in conductivity was saturated and starting the measurement after the light was turned off. Lattice matched structure (sample 1) and the strained structure with the channel In mole fraction (x) of 0.25 (Sample 3) did not exhibit PPC. Therefore, only the results of the measurements taken in dark are shown in Fig. 7 for these samples. A slight PPC was observed in Sample 2 (x=0.15, channel thickness=100 A). As reported previously [19], stronger PPC was observed in the as grown sample when the channel thickness was increased to 150 A.

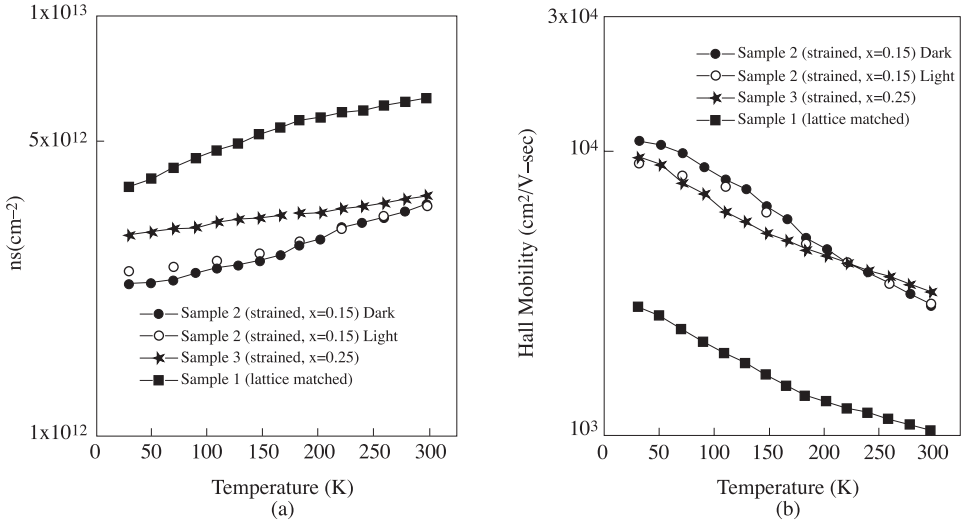

Figure 7. Results of the Hall-Effect measurements on the MODFET structures. (a) Sheet electron density, (b) Hall mobility

When the In mole fraction is increased from 0.15 (sample 2) to 0.25 (sample 3), an

increase in the sheet electron concentration is observed. This is expected due to the larger conduction band discontinuity at the interface of sample 3. However, the increase in the In mole fraction does not seem to improve the low temperature 2DEG mobility. This can be attributed to the larger 2DEG density in sample 3 and stronger intersubband scattering as the electrons occupy the excited subbands[20]. Besides, it has been shown theoretically that both the interface roughness scattering and alloy scattering limited mobilities decrease considerably with increasing 2DEG density [20,21].

Unexpectedly large 2DEG density, and low Hall mobility indicate that the Hall data taken on the lattice matched sample may be affected by the parallel conduction through the doped GaInP layer. In a two layer structure, if $\mu_1 B \ll 1$ and $\mu_2 B \ll 1$ where μ_1 and μ_2 are the carrier mobilities in the layers, the measured sheet carrier concentration and mobility can be expressed as [17]

$$n_s = \frac{(n_1\mu_1 + n_2\mu_2)^2}{n_1\mu_1^2 + n_2\mu_2^2} \tag{2}$$

$$\mu = \frac{n_1\mu_1^2 + n_2\mu_2^2}{n_1\mu_1 + n_2\mu_2} \tag{3}$$

We used the Hall data measured on the single GaInP layer doped to $4x10^{18}$ cm^{-3} and the above equations, and calculated the actual 30 K 2DEG density and the mobility in the lattice matched sample (sample 1) to be $2.62x10^{12}$ cm^{-2} and 3700 cm^2/V-sec, respectively. The actual 2DEG density in this sample is comparable to those in the strained structures and is still quite high which is desirable for MODFET applications.

In order to see the affects of annealing on the MODFET structures, we annealed two different sets of sample 1 (lattice matched) and sample 2 (x=0.15) at 400°C and 550°C. After sample 1 was annealed at 400°C for several minutes, 30 K 2DEG density decreased to $1.3x10^{12}$ cm^{-2} from the as grown value of $3.9x10^{12}$ cm^{-2}, and the 2DEG mobility increased to 8170 from 2800 cm^2/V-sec. A slight light sensitivity was introduced after annealing the sample at this temperature. After sample 2 was annealed at 400°C, a decrease in both 2DEG density and mobility was observed. 2DEG density at 30 K decreased to $1.4x10^{12}$ from $2.45x10^{12}$ cm^{-2} and the 2DEG mobility dropped to 5430 from 9050 cm^2/V-sec. Light sensitivity introduced to sample 2 by annealing at this temperature was much stronger than that introduced to sample 1, and we observed strong PPC in sample 2 after annealing. After the samples were annealed at 550°C, they both became extremely resistive with a very strong PPC.

5. Discussion

The absence of detectable traps and PPC in the highly doped ($N_D = 4x10^{18}$ cm^{-3}) as grown GaInP layer suggests that Si doped GaInP/GaAs modulation doped heterostructures should not suffer from PPC caused by microscopic barriers such as DX centers. Indeed, we did not observe any PPC in as grown lattice matched MODFET structures. Therefore, for MODFET applications, Si doped GaInP seems to be a proper alternative

to Si doped AlGaAs which suffers from DX center related problems at Al mole fractions of interest in device design. However, annealing introduced PPC and the decrease in the carrier concentration in GaInP seem to present a problem in device processing. The DX center like trap with 0.75 eV activation energy observed in undoped and moderately doped layers does not have a relation with Si doping since its concentration is not increased with increasing Si doping. The effect of Si doping on this trap is consistent with the report of Kwon et al. [14] who observed only one DX center-like trap with an activation energy of 0.26 eV in LPE grown GaInP. The authors attributed this trap to S impurity. Based on our results, the increase in the trap concentration by annealing suggests that the trap may be a defect complex consisting of a residual donor atom and a P vacancy. The increase in the trap concentration by annealing may be due to the out-diffusion of phosphorus as proposed by Huang et al. [12]. The reasons behind this anomalous behavior as well as the decrease in the electron concentration are not clear at present. The latter may also be due to Si atoms moving from donor to acceptor sites and the deactivation of the donors.

When the results of our study on the GaInP/$In_xGa_{1-x}As$/GaAs MODFET structures are considered, the decrease in the 2DEG density and the increase in the mobility in the lattice matched structure (x=0) after annealing can be attributed to the reduction in the net donor doping density in the doped GaInP layer. Especially, the increase in the mobility suggests that the anomalous behavior observed after annealing is not due to the diffusion of the dopants to the spacer layer or to the channel.

When compared with the lattice matched structures, the strained structures seem to be more sensitive to heat treatment. The PPC introduced to the samples after 550°C annealing can be explained by the increase in the DX center like 0.75 eV trap density in the doped GaInP layer. However, annealing at temperatures as low as 400°C also introduces PPC to the strained structures, and the 2DEG mobility is significantly degraded. As mentioned above, 400°C annealing does not cause PPC in the heaviliy Si doped GaInP layer. The reason for PPC in the strained structures does not seem to be the 0.75 eV deep trap present in the undoped layer of the structures. Hence, the conductivity of the undoped GaInP layer is much lower than the conductivity of the 2D channel, and the channel electrons are provided by the doped GaInP layer. Therefore, any PPC present in the undoped layer should not be reflected in the Hall meaurements which mostly reflect the properties of the highest conductivity region in the sample. In this case, strain relaxation related dislocations at the interface indicated by deep level A (Figure 6) with interface trap characteristics may be the reason for PPC introduced to strained samples after 400°C annealing. There is a general belief that all of the strain is not relaxed when misfit dislocations form at the interface, and this has been confirmed by annealing experiments showing an increase in the dislocation density with annealing [22]. The question of how the dislocation trap A causes PPC remains somewhat open. It is likely that the linearly arranged character of the traps forms a barrier for electron capture. Therefore, strained GaInP/InGaAs/GaAs structures do not seem to be thermally stable. Similar behavior was observed in AlGaAs/InGaAs/GaAs structures by Yang et al.[23].

6. Conclusion

We performed a detailed investigation of the electrical properties of Si doped single GaInP layers and GaInP/$In_xGa_{1-x}As$/GaAs MODFET structures. Important conclusions of this work are given below;

i. A 0.75 eV deep native trap with DX center like properties is present in GaInP and it causes PPC in samples with low free carrier concentration. Si doping has no apparent effect on the trap concentration. Therefore, Si doped as grown GaInP/GaAs MODFET structures should not suffer from PPC. However, annealing introduced decrease in the free carrier density in GaInP may present a problem in the processing of devices.

ii. Reasonably high 2DEG concentrations and mobilities can be achieved with the GaInP/InGaAs/GaAs modulation-doped heterostructures making this material system promising for MODFET applications. The 2DEG density in the lattice matched GaInP/GaAs heterostructure is comparable to the best values reported for the MODFET structures based on other material systems.

iii. A decrease in the low temperature 2DEG mobility is observed when the carrier concentration is increased above $1x10^{12}$ cm^{-2}. Therefore increasing the In mole fraction in the channel of the strained structures, which also increases the 2DEG density, may not improve the low temperature mobility.

iv. The strained GaInP/InGaAs/GaAs structures are not thermally stable even if the InGaAs layer thickness is sufficiently below the theoretical critical thickness.

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