Tr. J. of Physics
23 (1999) , 789 – 797.

An Investigation of Electrical Properties of Porous Silicon

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Received 01.03.1999

Abstract

In this work, electrical properties of porous silicon structures, formed with electrochemical anodization in HF acid solution under two different current densities, were investigated. In these experiments, Sb doped (111)-oriented n-type silicon samples with 0.006-0.015 Ωcm resistivity was used. Samples were anodized in a solution of 38% HF and 99% C_2H_2OH at 1:1 ratio for 15 minutes. After anodization, the structures that formed at low current density (J=5 mA/cm^2) was compared with structures that formed at high current density (J=30 mA/cm^2). Both structures and electrical properties were investigated

Introduction

Semiconductors have been used extensively in the area of circuit design and construction of electronic devices. Very rapidly changing electronics technology force semiconductor research to obtain much smaller and faster semiconductors. Recently, visible light emission observed from porous silicon (p-Si) structures obtained from a single crystal silicon at room temperature has attracted intense attention and research, the interest partially fuelled by the indirect band gap and the ease with which silicon (Si) can be prepared.

Porous silicon consists of a network of nanometer-sized silicon regions surrounded by void space. In order to obtain p-Si with desired dimensions and working quantity, electrochemical methods were employed. Porous silicon films were first obtained by Uhlir [1] and Turner [2] while studying electropolishing of Si in dilute HF acid solutions. With respect to the experimental conditions during the p-Si preparation, e.g., current density, anodization time, electrolyte concentration, films of different density have been obtained and mean p-Si density has been found to decrease with increasing current density during the forming anodic reaction. Unfortunately, despite research performed over many

years, the electrical and optical properties as well as the formation mechanism remains unknown. The purpose of this work is to investigate both the porous silicon structure and its electrical properties.

Experimental

Formation of The Porous Silicon Structure

In the experiments, Sb doped (111)-oriented, 0.006-0.015 Ωcm resistivity n-type Si was used. Samples of dimension 13×13 mm^2 were kept 15 minutes in $1NH_3+1H_2O_2+4H_2O$ solution for cleaning, then rinsed with deionised water. In order to obtain a uniform current distribution the back side of the samples were coated with ∼600 Å Aluminium layer. Contacts were taken from this aluminium coated surface and placed in front of the Teflon cell as illustrated in Figure 1.

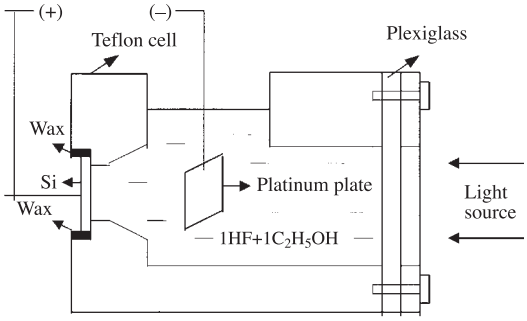


Figure 1. Electrochemical set up

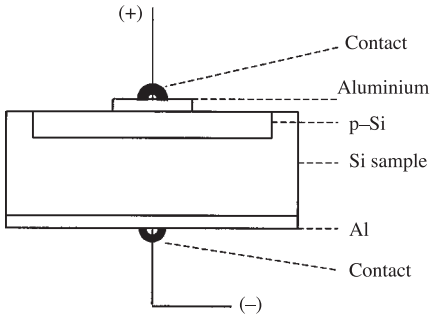


Figure 2. Configuration for the electrical measurements.

Before anodization, in order to get rid of the oxide layer, samples were kept in dilute HF acid solution ($1HF+4H_2O$) for 5 minutes, then were rinsed with deionised water. In the anodization process 38% HF and 99% ethanol solution was used at 1:1 ratio. Anodization was performed at two different current densities, 5 and 30 mA/cm^2, respectively. During anodization a 250 W tungsten light source was placed 15cm away from the samples and a reference electrode, a platinum plate was placed 3 cm away from the sample. Anodization was performed for 15 min. Bubbles were observed during anodization and are believed to be hydrogen gas. After anodization, samples were taken from the Teflon cell and rinsed with ethanol for 2 minutes and dried at room temperature.

Electrical Measurement

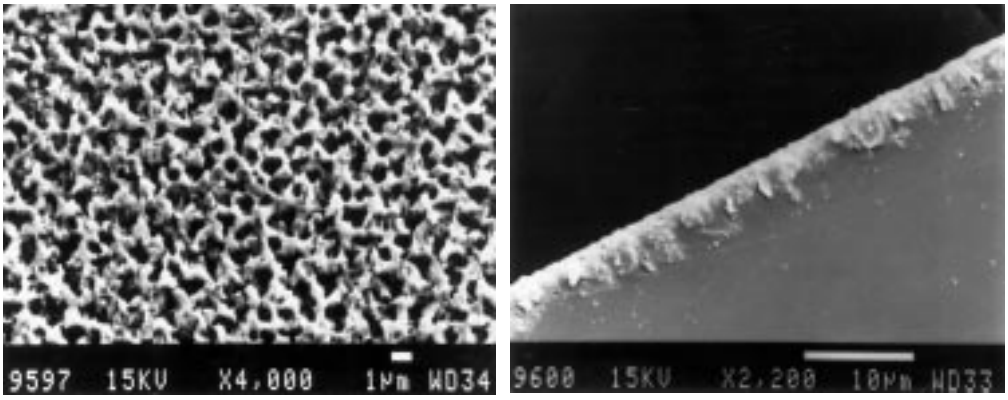
Before the measurements, a 5×5 mm^2 area of the samples were coated with ∼1000 Å layer of aluminium. All electrical measurements were established in a dark room, as shown in Figure 2.

For capacity measurements, a 5 Hz-13 MHz impedance analyser was used. During capacity measurements, the voltage between the two contacts was scanned between -5 V and +5 V and the obtained data was recorded by a x-y recorder. During measurements, frequency was kept at 1MHz. For the current-voltage measurements, two electrometers and a 25 V power supply were used. The voltage was varied from 0 V to the voltage breakdown point of the samples.

Results

Data showed differences between high and low current densities. A porous structure was established at certain current values (5-30 mA/cm^2). For current less than 5 mA/cm^2 and greater than 30 mA/cm^2, a porous structure was not observed, which agrees well with the theory discussed in the literature [1,2,3,4,5,6,7]. In order to form a porous structure there should be holes on the surface of the semiconductor. Therefore, to increase the hole concentration on the surface of n-type Si, the sample was illuminated during anodization (see Refs. [3,5,6]). Experiments performed without illumination showed no porous structure. Results thus indicate that a supply of light is necessary.

During processing it was observed that samples became grey in colour for both low current (5 mA/cm^2) and high current (30 mA/cm^2) for both 15 and 30 minutes anodization time. The resulting structures were photographed by SEM and are shown Figure 3 and 4.



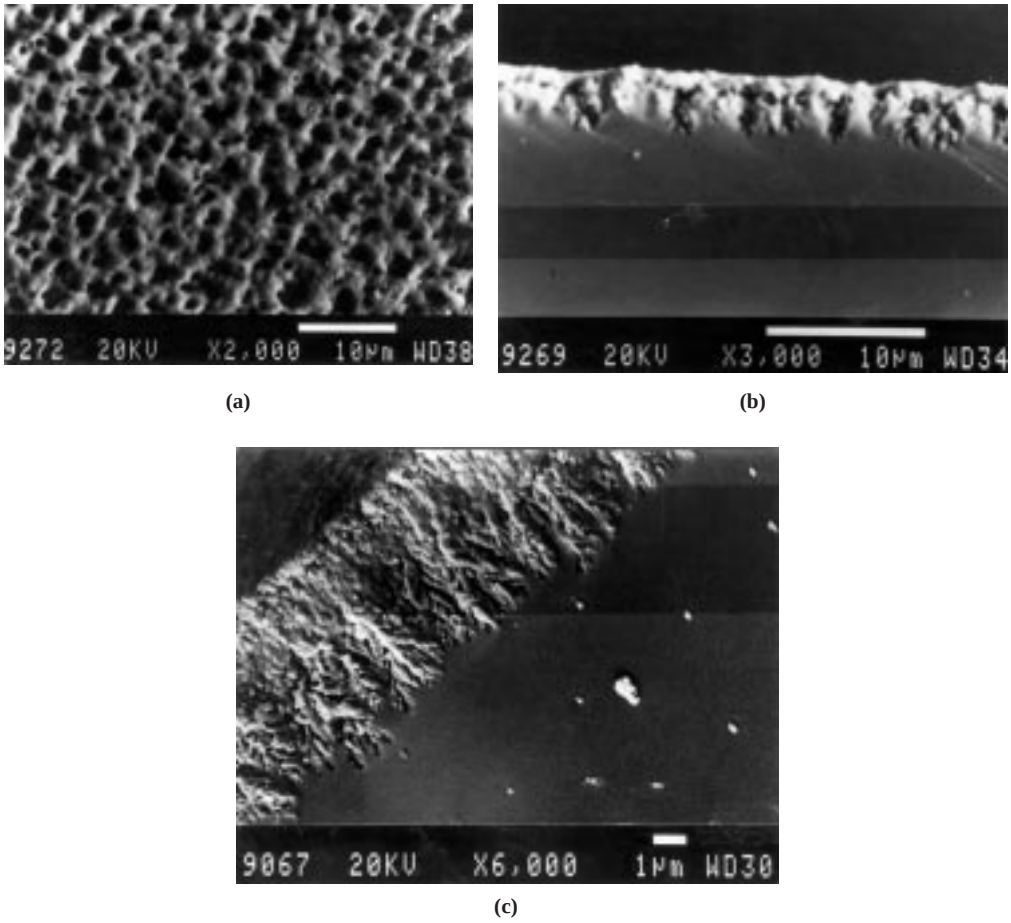
(a) **(b)**

Figure 3. p-Si structure obtained at low current density (5 mA/cm^2). a) surface film, b) cross-section film

From the data in Figures 3a and 4a, the pore radius for 5 mA/cm^2 current has been deduced to be approximately 0.3-0.8 μm, and for 30 mA/cm^2 is approximately 1-3μm. Moreover, the porosity of the sample was calculated to be 40% for low current density and 60% for high current density.

Figures 3b, 4b and 4c show cross-sections of the samples. From these figures it was

observed that porous Si layer thickness is about 4 μm for 15 minutes anodization time. Results are summarised in Table 1. Additionally, the cross-sectioned image of the porous region, Figure 4c, shows branches.



(a) (b)

(c)

Figure 4. p-Si structure obtained at high current density (30 mA/cm^2). a) surface film, b) cross-section film, c) cross-section film for 30 min.

With help of the surface images of the samples (see Figs.3a and 4a), it is seen that with lower current densities the pore diameter show smaller diameters than those associated with higher current densities. Therefore we think that the pore diameter may be increased by increasing the current density. Parkhutik [8] obtained the same results at two different current densities (25 mA/cm^2 and 5 mA/cm^2). With the help of images shown in Figure 3b, 4b and 4c, thickness of the n-Si layer with 30 minutes anodization time has thicker layer, therefore the layer thickness is related with anodization duration. Separately, one

can also see a relationship between the thickness and the pore depth. Since the current prefers the least resistance during the anodization, relation between the pore depth and the layer thickness seems reasonable [3,4,9].

Table 1. Dependence of p-Si structure on current density

Current Density	Porous Diameter	Thickness of Porous Layer	Porosity
5mA/cm^2	0.3-0.8μm	4μm	40%
30mA/cm^2	1-3	4	60%

Table 2. Values obtained from I-V measurements

Sample and Current Density	I_S	n	ϕ_b
5mA/cm^2	1.4-5.5mA/cm^2	25-30	540-570 mV
30mA/cm^2	3.4-5.2	16-22	540-550
Reference Sample	1.1	26	580

Table 3. Values obtained from C-V measurements

Sample and Current Density	N	W
5mA/cm^2	$2x10^{12}$cm^{-3}	54-80μm
30mA/cm^2	$2x10^{13}$	36-44
Reference Sample	$2x10^{11}$	74

Figure 5 illustrates the results obtained from current-voltage measurements. It can be seen that formation of the pores is strongly related with the current-voltage characteristics of the sample. Moreover, calculations show conductivity around 10^{-5} $(\Omega\text{cm})^{-1}$ while the reference sample conductivity is around 10^{-4} $(\Omega\text{cm})^{-1}$. Reference sample dimensions are 13×13 mm^2 and were coated with ∼1000 Å Aluminium on the front and ∼600 Å on the back side. No anodic process had been applied. From literature [6,10,11], it was seen that higher resistivity is a result of carriers trapped at the pore walls.

From the data plotted in Figure 5, the dependence of lnI versus V is plotted in Figure 6. The slope of the curves gives the saturation current density (I_S, in units of mA/cm^2), the ideality factor (n) and the barrier potential (ϕ_b, mV). Their values are given and compared with those of the reference sample in Table 2.

Figure 6 displays the logarithm of the current as a function of the applied voltage. It shows that samples anodised by low current density has a lower ideality factor than the samples anodised by high current density. The present values are not higher than those obtained by Chorin [11] but still high for an ideal diode. These results shows that increasing the current density is a way to obtain an ideal diode. Ideality factor n_{ef} can be explained by the high density of states at the sample interface [11,12]. In the present work, calculated barrier potential of the samples are very close to each other and are not different from value in the literature. Contrarily, saturated current density values are higher than published in [10]. When we apply a forward bias to the metal-semiconductor junction (metal side is positive and semiconductor side is negative), the electron energy levels on the semiconductor side will increase by $e(V_{bi} - V)$, where V_{bi} denotes the built-in voltage and V (Volt) denotes the applied forward bias voltage between metal and semiconductor.

Therefore, the Fermi energy level of the semiconductor should increase by the value of eV as well. Thus, barrier height for the electrons passing from semiconductor to metal will be decreased by eV. As a result, current flow from semiconductor to metal will increased by exp (eV/kT) and the electrons will face different barrier heights at different voltage values. This barrier height is small comparison to kT but has a high saturation current density [10].

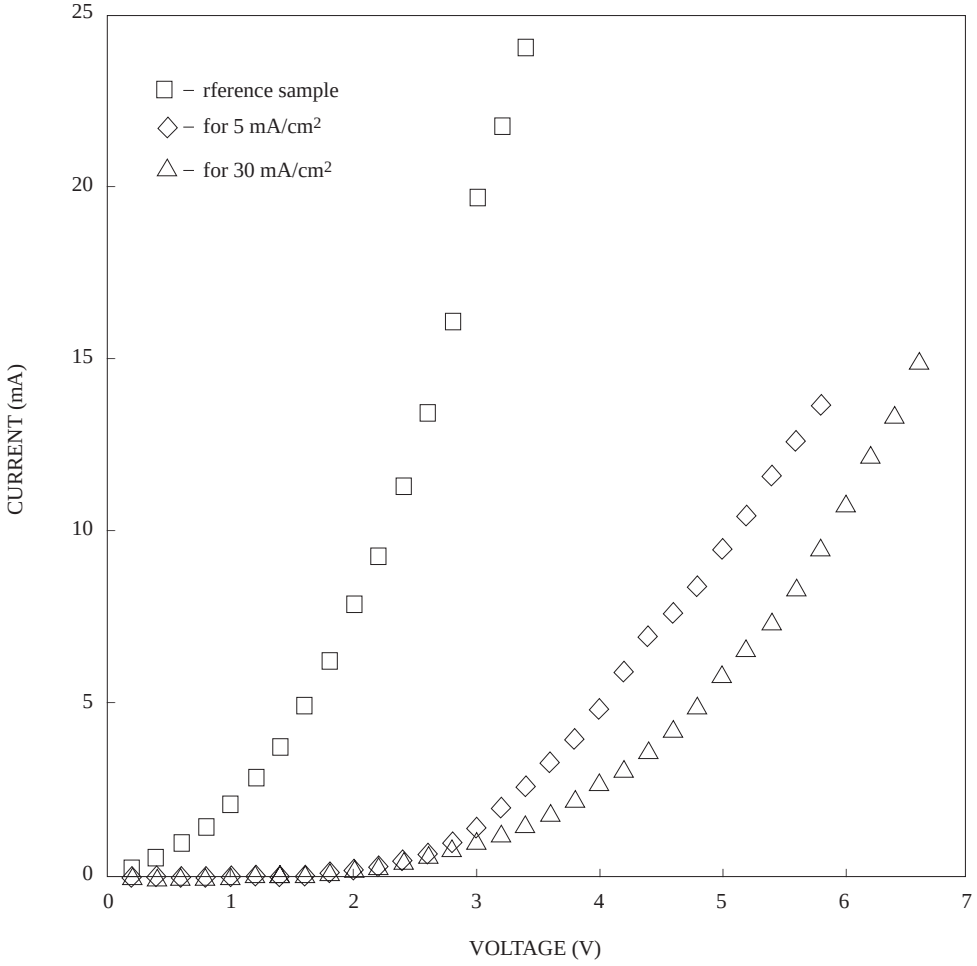


Figure 5. I-V characteristic

C-V measurements were made and are plotted in Figure 7 as graphs of $1/C^2$ versus V (Volt). Due to nonlinearity of the slopes, calculations are made in the selected voltage range of 1-3 V. The built-in potential is obtained from the intersection of the $f(V)=1/C^2$ plot with the abscissa. By using the slope of the curves and necessary equations the

effective carrier density, N (cm^{-3}) and width of the depletion layer, W (μm) is calculated. Results are given Table 3. The results of the reference sample also can be found at Table 3.

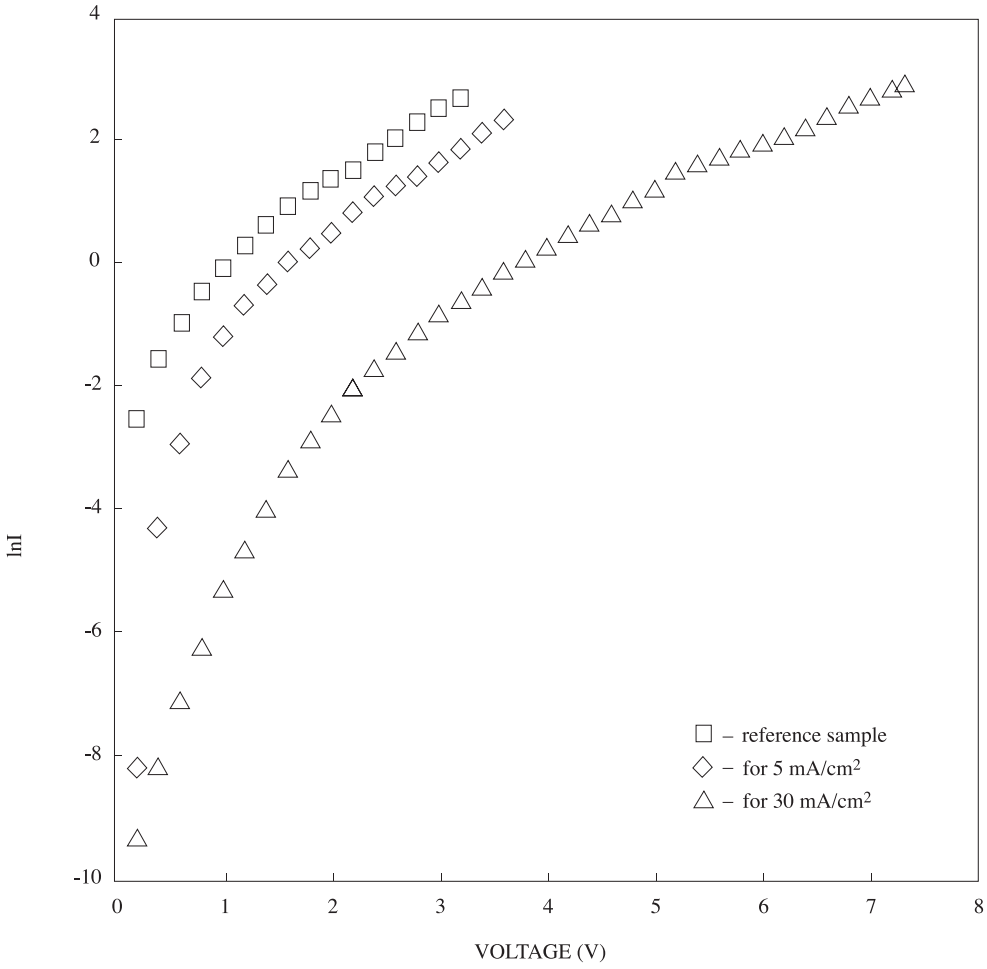


Figure 6. lnI versus V graphic

According to capacitance-voltage measurements, drawing $1/C^2$ versus V does not give a straight line (see Figure 7). This means that the depletion layer and the barrier height are not constant and so the carrier concentration will not be constant at the depletion layer. From the results shown in Table 3, it can be seen that by increasing the current density, the depletion layer becomes smaller and the carrier concentration increases. This phenomena can be explained by not only the diffusion mechanism but also the tunnelling mechanism [10,11,12,13].

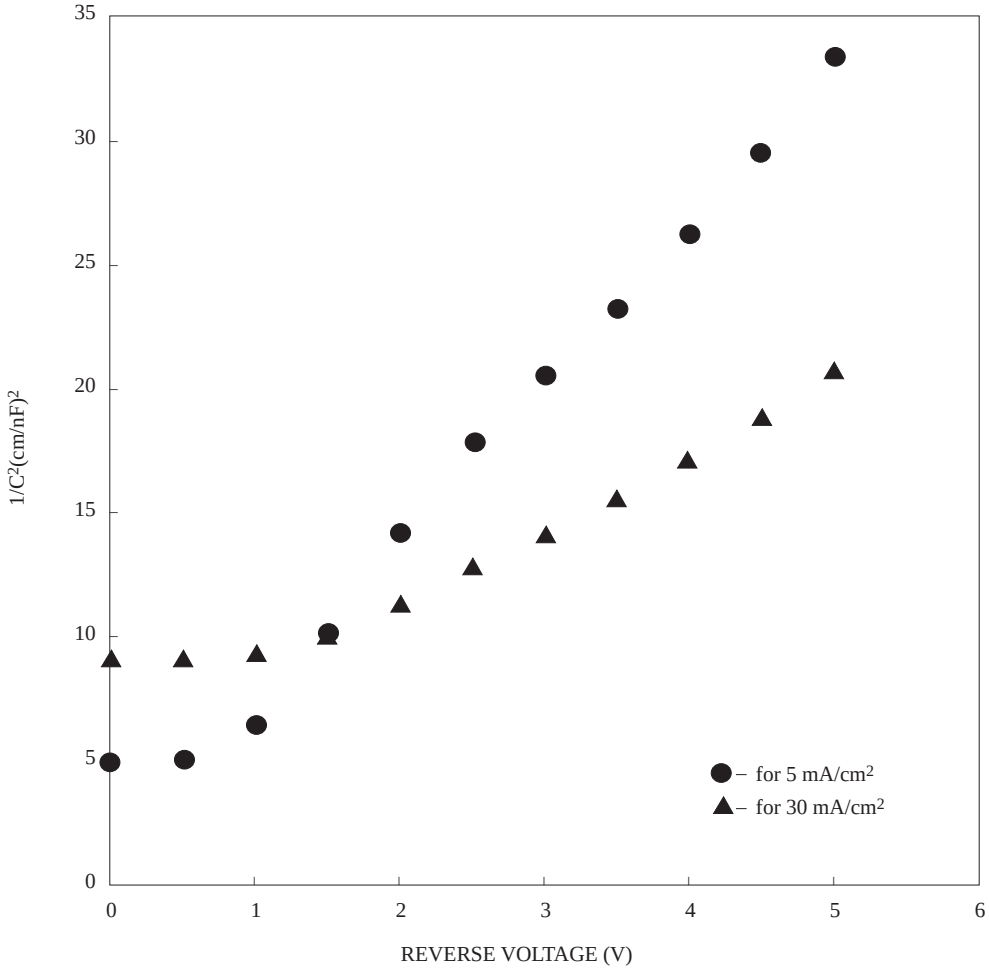


Figure 7. C-V characteristic

Conclusion

As a result, comparing the electrical measurement results with literature it can be seen that (for n-type porous Si) both pore radius and concentration grows by increasing the current density. Layer thickness increases with anodization time and during the formation of the porous layer the reaction grows in the direction of the thickness. In addition, the transport mechanism can be explained by both diffusion and tunnelling mechanisms. Moreover, it can be stated that the structure acts like a Schottky diode for both current densities. It is thought that p-type Si might be investigated using TEM.

Acknowledgment

This work was partially supported by The Research Fund of The University of İstanbul, prowect number: T-224/050396

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